EIGHTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

March 5 - 8, 2017

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Session 6

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BiTS Burn-in & Test Strategies Workshop 2017

Session 6
Jason Mroczkowski
Session Chair

BiTS Workshop 2017 Schedule

Frontier Day

Tuesday March 7 - 1:30 pm

Making Contact

"High Current Final Test Contactor Development"

Thiha Shwe, Hisashi Ata – Texas Instruments

Kenichi Sato – Yokowo

"Customers Are the New Team Member for Board to Board Connectors"

Derek Biggs – Plastronics

"WLCSP Contacting Technologies for 0.2 mm Pitch and Below"

Valts Treibergs - Xcerra Corporation

"Coming to terms with Burn-In sockets"

James Tong - Texas Instruments

BiTS 2017 Burn-in & Test Strategies Workshop

High Current Final Test Contactor Development

Thiha Shwe
Texas Instruments

Hisashi Ata
Texas Instruments

Kenichi Sato
Yokowo Co., Ltd

BiTS Workshop
March 5 - 8, 2017

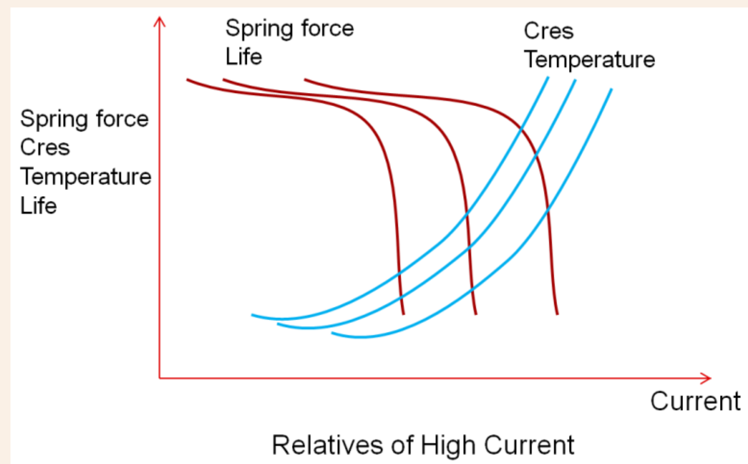
yokowo

Overview

- Background
- Problem statement
- Challenges and solutions
- New Current Carrying Capability (CCC) measurement methods
- Simulation of probe temperature rise
- Pin temperature rise studies
- Summary

Background

- To accommodate smaller pitch devices, size of the pogo pin becomes smaller
- Complex test applications to measure
  - ➢ Low RDSon and High current testing on the same device pin
  - ➢ Under different test temperature
- To develop a pin with
  - ➢ Small pitch
  - ➢ Higher CCC
  - ➢ Low Cres
  - ➢ Tri-Temp
  - ➢ Reliability

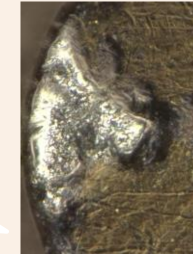


Problem Statement

- Issues due to high current:
  - Depressed pins
  - Burnt pins
  - Burnt springs
  - Discolored barrels
  - Spring force reduction

High maintenance, low Yield and low throughput

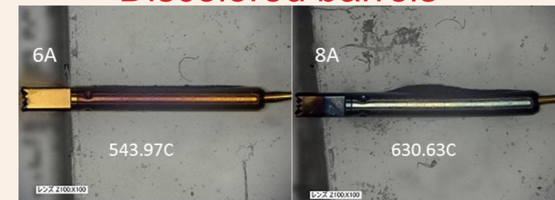
Melting tip



Depressed string

- Correlation between pin CCC and actual device testing
  - **Pin Spec:** ISMI (International Sematech Manufacturing Initiative) and Temperature rise methods use **Continuous Current**
  - **At Test:** Various **Pulse Current**

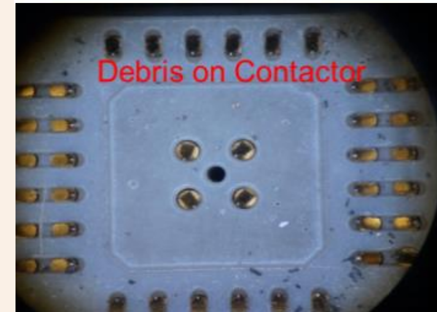
Discolored barrels



Challenges and Solutions

- Dual Pogo strategy
  - Electrical and mechanical redundancy
  - Reduce pin's Cres and Sharing current

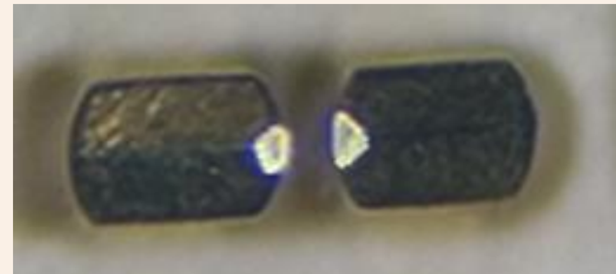
- Debris, foreign material
  - Debris cause high contact Resistance between pin and device
  - The higher the Resistance, the higher the Power ➔ the higher the Energy



Challenges and Solutions

- Alignment
  - ➢ Having good contact between DUT and pin is important ➔ improving device guide, handler alignment,… are essential
- Test program robustness
  - ➢ Optimum current I-range and clamping
- Pin tip worn out
  - ➢ Worn out tip result high Cres
  - ➢ Pin tip shape and material

Worn Out Tip

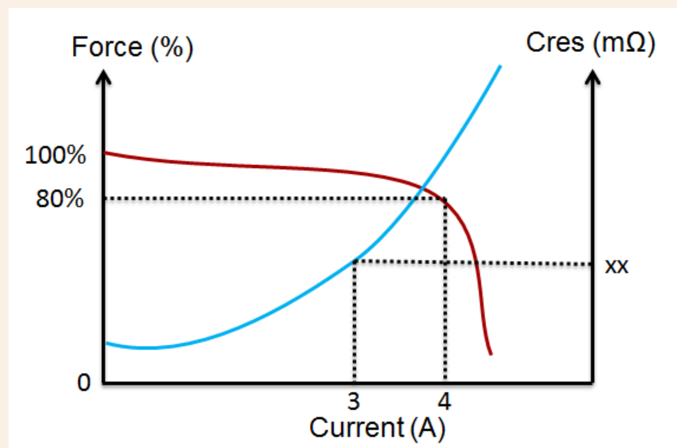


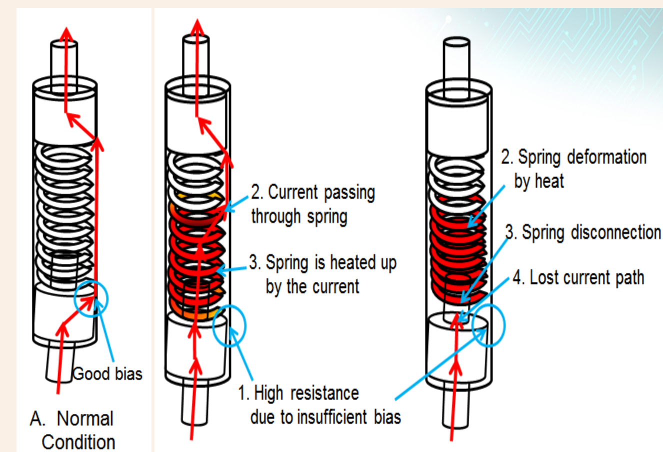
New Current Carrying Capability (CCC) Measurement Methods

- Force/Cres reduction method
- Pin life vs. CCC
- Test temperature vs. CCC
- Mechanical, Electrical, and Thermal Stress test (METS CCC Test)

Force/Cres Reduction Method

- Modified ISMI Method ➔ Measure and monitor not only force, but also Cres
- Set Cres limits at maximum xx mΩ
- Why does Cres increase, but force stays within the 20% reduction ➔ Biasing?

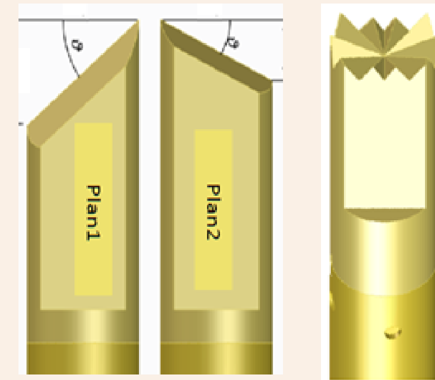




Pin Life vs. CCC

- CCC decreases along with increasing insertions
- Aged pin's Cres becomes unstable → causing low CCC
- Reliable contact at DUT side and maintaining internal contact resistant are essential

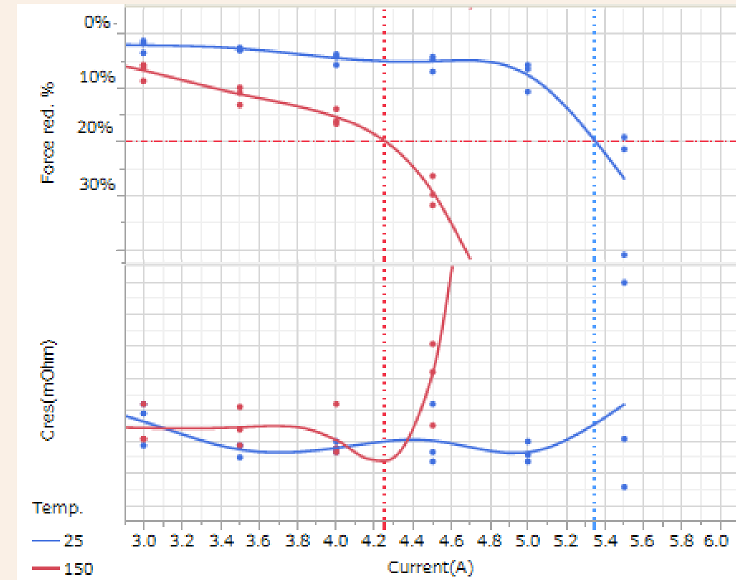
Test Condition	Modified ISMI	
	CCC (A)	CRES (mΩ)
Initial	4	54
250K Insertions	4	62
500K Insertions	3.5	66
750K Insertions	2.5	69
1M Insertions	2	73



Test Temperature vs. CCC

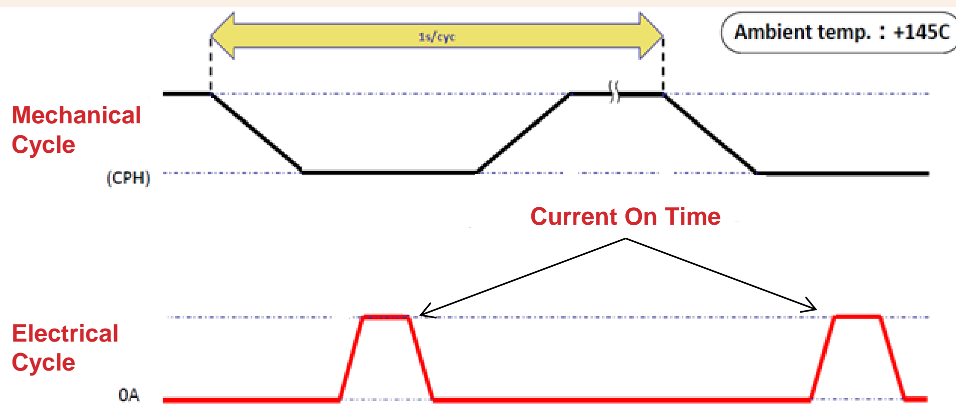
- Pin CCC dramatically reduces while testing under high temperature
- Pin's Cres increases at higher temperature
- Thermal stresses significantly affect the structural strength and stability of the pin

Pogo Pin Under High Temperature

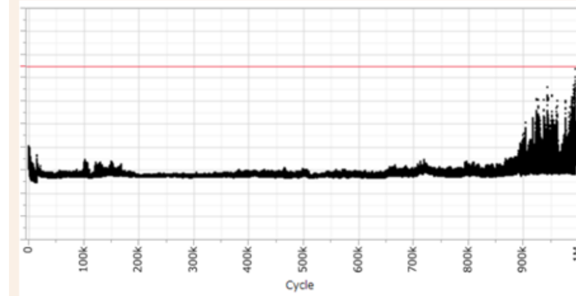


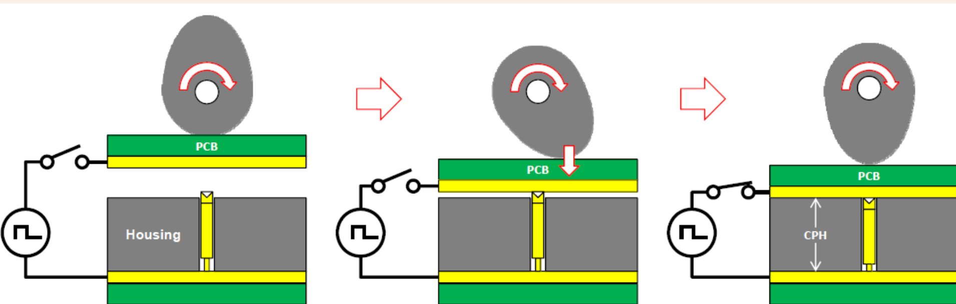
METS CCC Test

- Test Procedure: Apply Mechanical, Electrical, and Thermal Stress on the same setup.

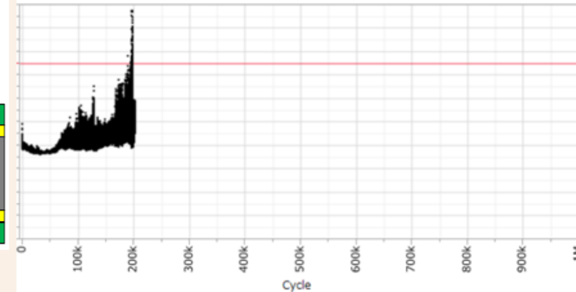


Test result under room temperature





Test result under 145°C



Simulation of Probe Temperature Rise

- Temperature is one of the KEY factor
  - Ambient temperature
  - Joule heating by Current
- Probe performance is changed by various Current condition
  - Better understanding about behavior of Electrical / Thermal load under various current condition is essential
  - ISMI CCC Specification does not cover for all actual test condition

Pin Temperature Rise Studies: Choosing the Most Severe Test

- Various current conditions are expected in actual test
  - 1x (A) 80ms On / 300ms OFF
  - 2x (A) 80ms On / 300ms OFF
  - 6x (A) 10ms On / 300ms OFF
  - And so on …
- Probe surface temperature is good to understand about Electrical / Thermal load

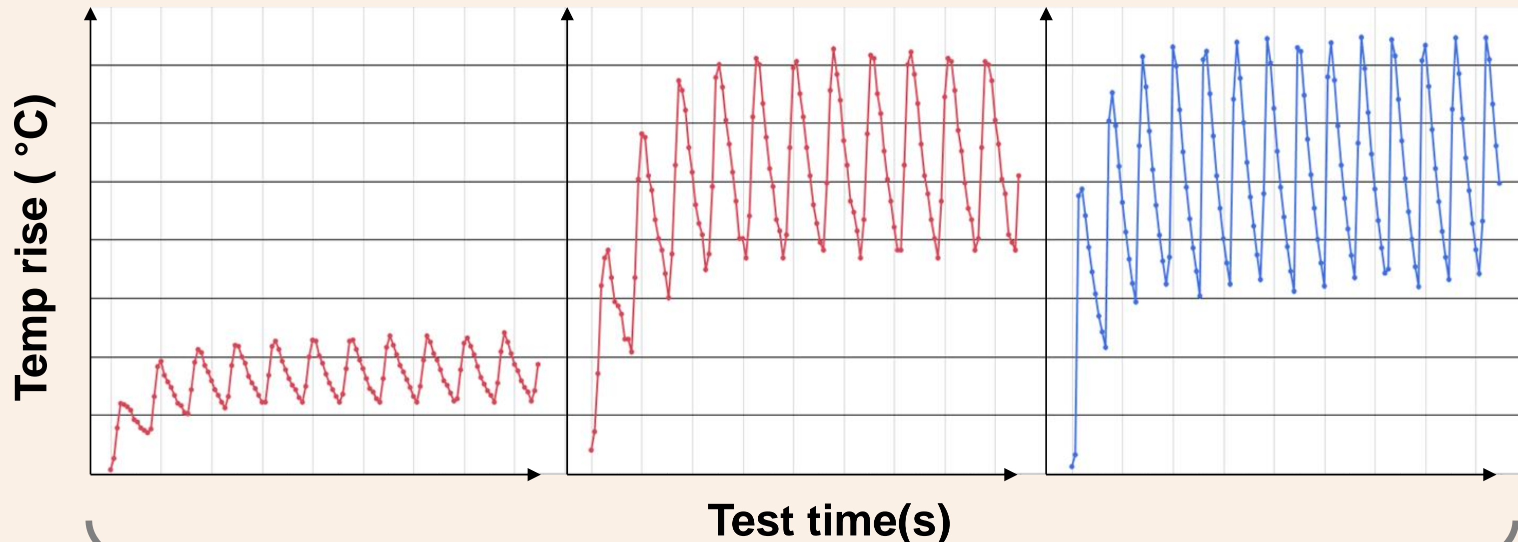
Measurement Setup for Probe Surface Temperature

- Infrared Camera is used
- At Room temperature No housing around DUT
- Various pulse current conditions

Temperature Rise by Pulse Current Conditions

At Room Temperature

1x(A) 80msOn **2x (A) 80msOn** **6x (A) 10msOn**



Different conditions but similar results

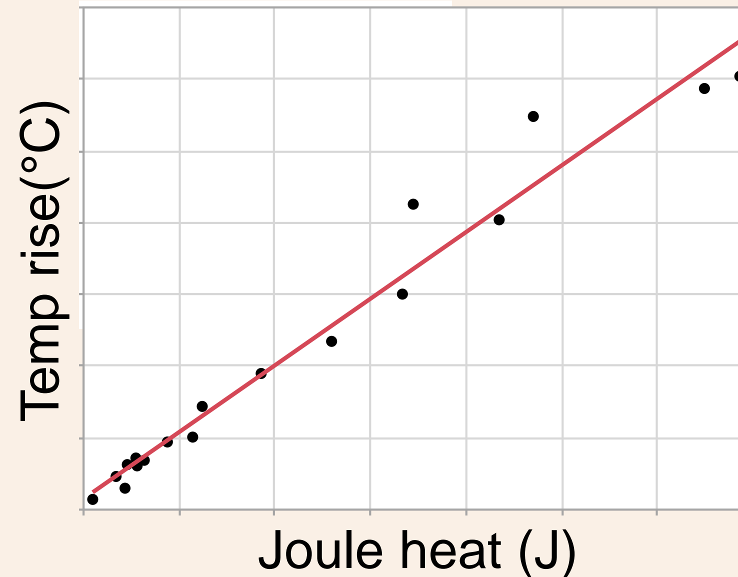
(Same off time applied to all conditions)

Temperature Rise by Joule Heat

- Probe temperature rise is determined by Joule heating
  - Joule heating equation

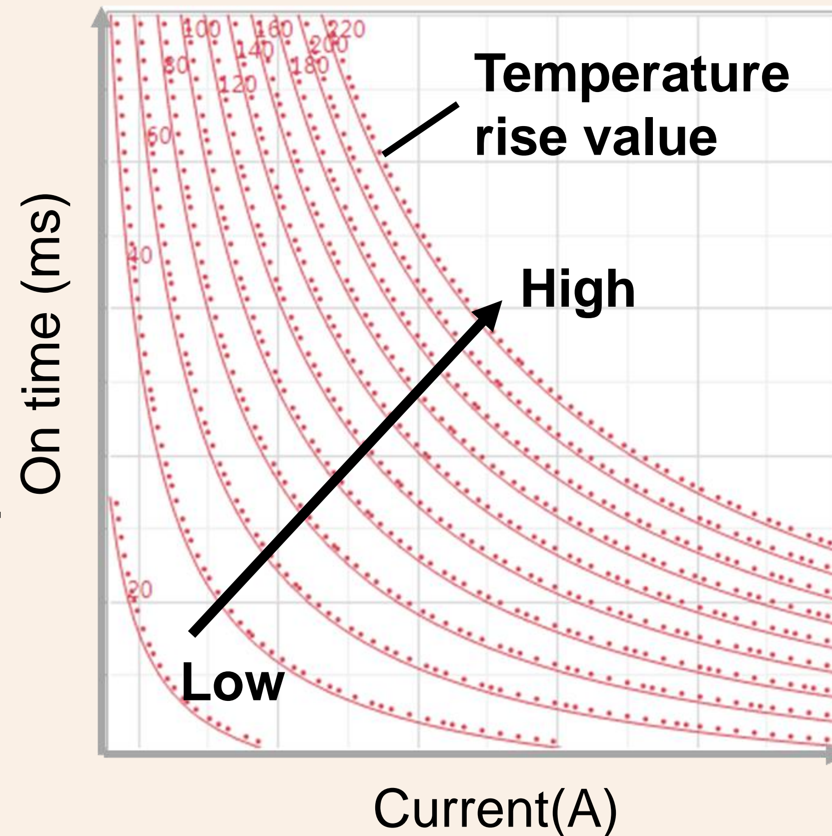
$$Q = RI^2t$$

- 18 different test conditions to simulate



Temperature Rise Contour Map

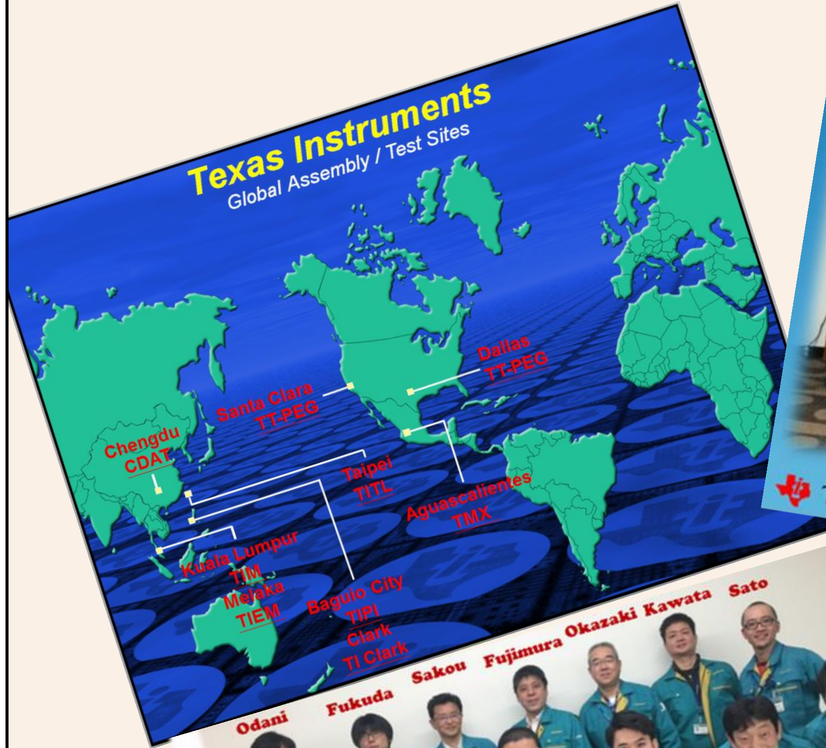
- Based on DOE, temperature rise map is created
- Same temperature rise value on different conditions is observed



Summary

- Utilizing METS (Mechanical, Electrical and Thermal Stress) CCC test data to develop high current probe
- Maintaining low Cres is important
- CCC of the pin varies with ambient temperature, Joule heat and pin life (insertions)

Acknowledgements



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