EIGHTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop ™

March 5 - 8, 2017

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Session 5

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BiTS 2017
Burn-in & Test Strategies Workshop

Session 5

Rahima Mohammed
Session Chair

BiTS Workshop 2017 Schedule

Frontier Day

Tuesday March 7 - 10:30 am

Heating Up

"Process Improvements to Increase Burn-In Yield and Quality"

Jeanette Linn, Rich Karr - Texas Instruments

"Device Characterization Over Temperature at the Board Level"

Barry Johnson - inTEST Thermal Solutions

"Qualifying A Process For Higher Burn-In Voltage Application"

Krishna Mohan Chavali - Globalfoundries US Inc

"Coming Challenges and Opportunities for MEMS Testing Supply Chain"

Wendy Chen - KYEC

BiTS Burn-in & Test Strategies Workshop 2017

Qualifying A Process For Higher Burn-In Voltage Application

Krishna Mohan Chavali
GLOBALFOUNDRIES

BiTS Workshop
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ABSTRACT

- More often foundry customers push for higher Burn-in Voltages or "Over Drive" (OD) conditions.
- As Gate voltages scale down below 1V, its critical to Characterize for OD voltages, for sub-micron nodes.
- OD BI also reduces the wafer, module level screening and production burn-in before shipment of products.
- Detailed scheme of qualifying a product for Higher BI / Over Drive Voltage application.

INTRODUCTION

- Typical BI voltage is **1.1V to 1.3V** for Qualifications.
- Products (APU/GPUs) with > 87.6K ~ 110K POH field life also call for "Over Drive Voltages". * POH - Power On Hours
- What are critical reliability considerations to be evaluated ?
- What are the Reliability mechanisms to include ?
  - Ex: FEOL/BEOL (Front and Back End of Line)
- Additional Circuit/Product evaluations to be done ?

Assumptions & Limitations

- For device level assessments use appropriate models for that technology node, as they will vary.
- BI voltage determined here is not to screen out EFR fails.
- BI voltage to be high enough to increase random failures,
- Also to be low enough not to cause main population fallout.
- Life time requirements in this procedure to be adjusted depending on acceleration factors and for that node.

RELIABILITY CONSIDERATIONS

Reliability considerations are mainly:

1) **Device Level / Intrinsic Reliability.**
2) **Circuit Level / Product Reliability.**

1) Device Level Reliability considerations:

- **Parasitic Bipolar turn-on for (NMOS/PMOS)**
- **BTI (Bias Temperature Instability)**
- **TDDB (Time Dependent Dielectric Breakdown)**
- **HCI (Hot Carrier Integrity)**
- **EM (Electro-migration)**
- **Device Latch Up**

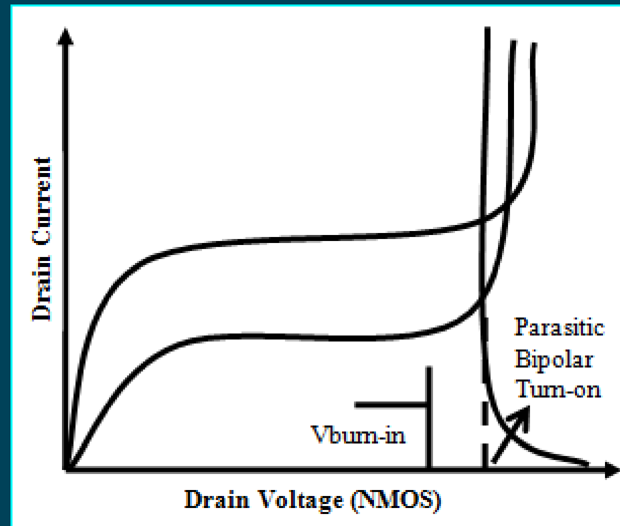
RELIABILITY CONSIDERATIONS - 2

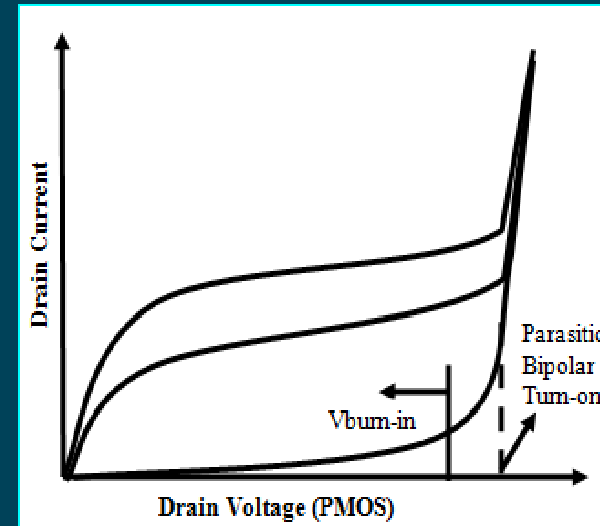
2) **Circuit Level Reliability Considerations:**

- Circuit Level Reliability Evaluation Results
- Package Reliability Evaluation Results.
- Local / Joules' heating
- Latchup – Package Level.
- Dynamic High-Voltage Stress Test Evaluation

Device Level Reliability Considerations

Parasitic Bipolar turn-on: N/P MOS





Output Characteristics of Transistor. Maximum Vburn-in allowed is indicated.

- Check for both NMOS and PMOS devices.
- Over Drive / BI Voltage < transistor Turn-On.

Bias Temperature Instability (BTI) Life Time

- BTI is prominent at higher temperatures (recent nodes).
- The BTI Life Time margin and its impact to be considered:
  - For both NMOS, PMOS &
  - Also for all Gate (thin, IG, thick) voltages.
- **SRAMs:** Impacts Vmin, shift, RWM (Read Write Margin).
- **Logic:** Impacts Speed & Fmax degradation additionally.

TDDB Life Time

- FEOL (Front End of Life) TDDB Life Time margin to be checked before setting the Over drive voltage.
- BEOL (Back End of Life) TDDB margin also to be checked, as the designers maximize the Metal layer routings and current densities.

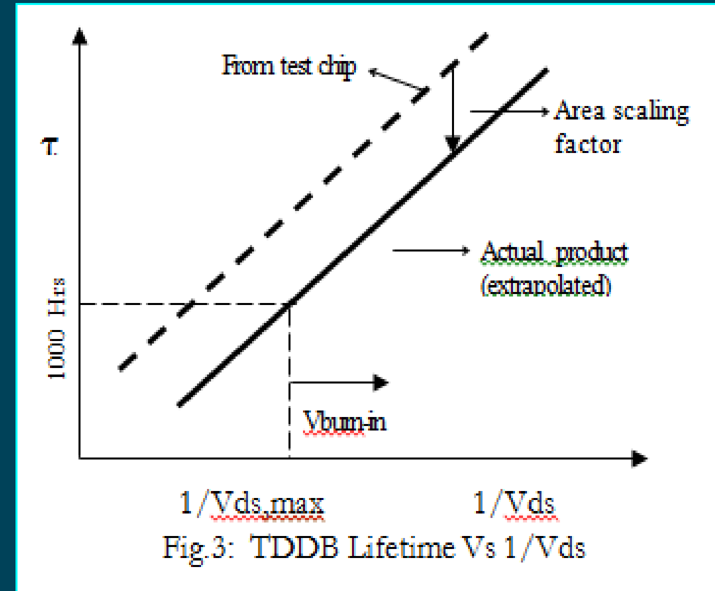


Fig.3: TDDB Lifetime Vs 1/Vds

FEOL & BEOL TDDB Life Time:

Maximum Vburn-in allowed is indicated.

Hot Carrier Integrity (HCI) Life Time

- Mainly driven by "Hot Carriers".
- Prominent at low temperatures.
- HCI Life Time to be checked for Products that need Low Temperature Operation (LTOL).
- Some product Quals need LTOL Test. Ex: AEC/Aero/Space.

Vburn-in < 1 / Vds,max

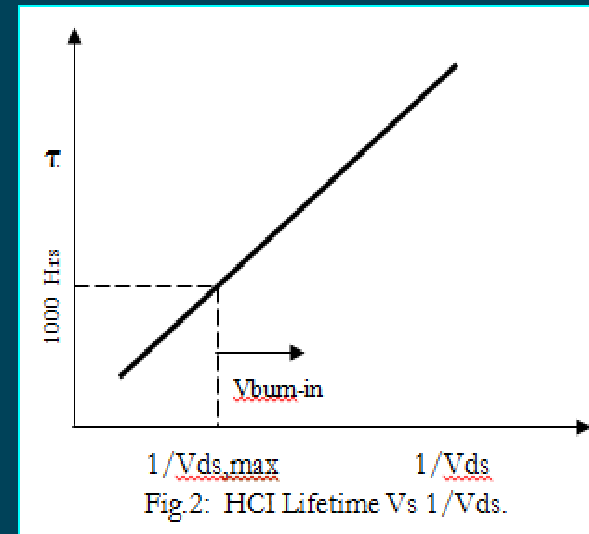


Fig.2: HCI Lifetime Vs 1/Vds.

HCI Life Time: Maximum allowed Vburn-in is indicated.

Electro-migration: EM Life Time

- EM Life time at Tburn-in to be checked.
- Designers must take into account Tj burn-in at actual elevated temperature and at rated current density.
- Extrapolate EM lifetime for such increased temperature and current densities.

Black's equation: $ttf = \frac{a}{i^n}\exp(\frac{Ea}{kT})$

where, a and Ea are technology dependent,

k is Boltzmann's constant,

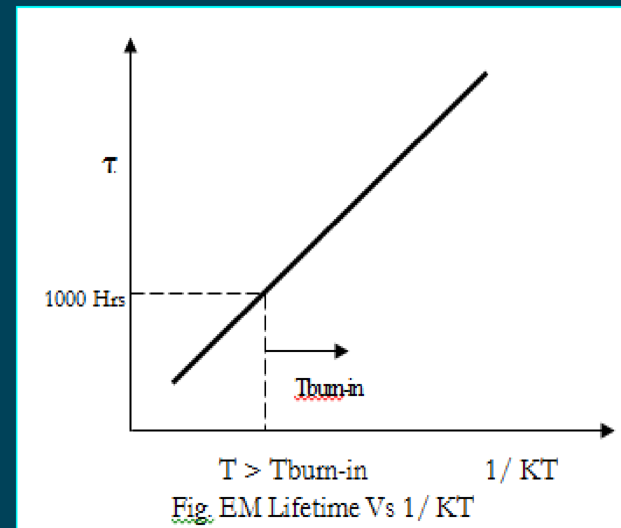


Fig. EM Lifetime Vs 1/ KT

EM Life Time: Maximum Vburn-in allowed to be lower as indicated.

Latchup: Device Level

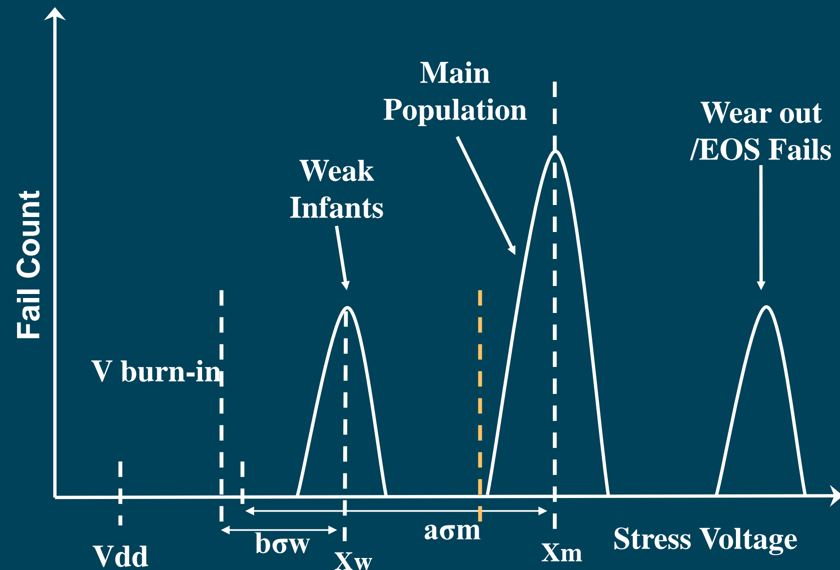
Though the package type other considerations allow higher voltage, the device might Latch up / Snap Back during BI.

- The device **Latch up and Snap Back** should be checked.
- The devices should be checked for **intrinsic latch-up** robustness at Vburn-in at rated Tburn-in.
  - Done by triggering 4-stripe PNPN structures @Tburn-in.
- Device Trigger voltage must be >> Vburn-in.

Circuit Level Reliability Considerations

Check the SSV & OD Range

- The "Safe Screen Voltage" (SSV) to be setup for that technology node / product.
- To have clear idea of what's the Vdd range and where are the boundaries.
- OD BI voltage should be:
  - Slightly higher than SSV.
  - Able to screen weak infants.
  - Just below main population.



Mean of Main Population kill voltage	:	X_m
Mean of Weak Infant population kill voltage	:	X_w
Standard deviation of Main Population Vkill	:	σ_m
Weak Infant population kill voltage Std. Dev	:	σ_w

Circuit Level Reliability Evaluations

LIMITATIONS ON THERMAL & VOLTAGE ACCELERATIONS

Points to consider on Thermal and Voltage acceleration Factors for OD BI:

Junction Temperature: The junction temperature at BI is a function of both thermal as well as voltage conditions used:

$$T_j = T_a + (P_d \times \theta_{ja})$$

where Ta is the Ambient Temperature. (°C)
Pd is the Power Dissipation = V x I (W)
θja is the Thermal Resistivity of packaging (°C/W)

Hence the voltage and thermal accelerations are so selected that:

Device Tjstress at OD BI not exceed design specs of the DUT/Circuit.

Package Reliability Evaluations

Package level considerations to be checked:

- Package Type: Wire Bond or Flip Chip/Laminated

  Package Thermal << Solder bumps rated melting temp.

  - @183-190C for some Solder/Ag/Sn compositions.

- Encapsulation Type: Plastic, Ceramic
  - For some QFPs $T_{glassivation}$ @ 160-190°C
  - The BI conditions should not exceed those specs.

- Others: BI System PSU's, BIBs & Sockets' Specs.

Local / Joules' Heating

Points to be considered for higher BI:

- Chip's Joules heating at BI Voltage and temperature.
- Wafer level Higher BI data could be good reference.
- But consider IR drops & self heating for package level BI.
- Circuits with VCO's/RO's: KIV self and local heating.
- The stress voltage should not push the chip into thermal runaway mode during BI.

Latchup: Package Level

- Do package level Latch up test at 25C & 125C.
- Check limits on OVS and OCS at high temp.

  (Over Voltage & Over Current Stress)
- Check leakage currents and limits at:
  - Individual and across pin groups at package level.
- Check BIBs & BI Oven for any Over-shoot and Undershoot currents that exceed the LU limits.

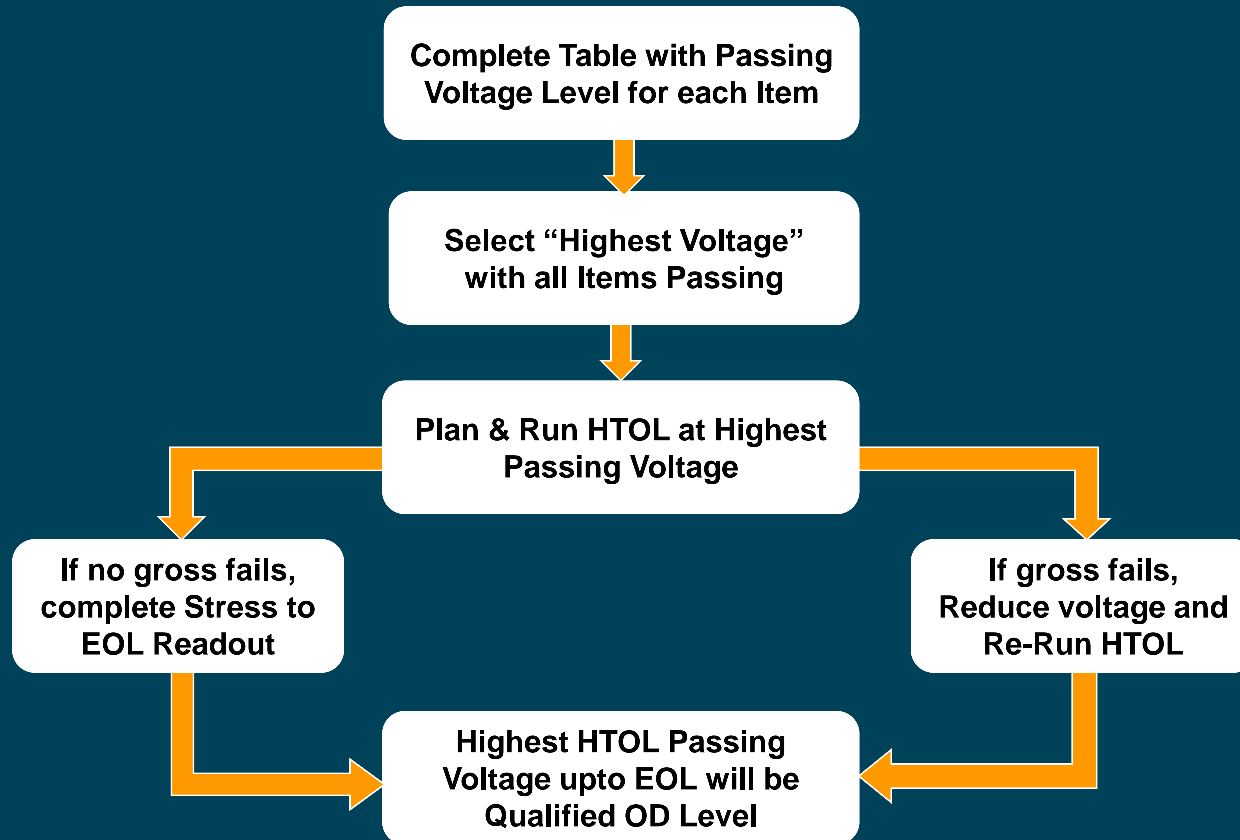
Consolidation of Reliability Considerations

REL Items Table: Device & Circuit

After doing the Reliability assessments, compile all the results in to a table:

Check Item	Sub	1.1xVdd	1.2xVdd	1.3xVdd	1.4xVdd	1.5xVdd	1.6xVdd
Bi-Polar Turn On Voltage	NMOS						X
	PMOS						
BTI Lifetime	NMOS					X	X
	PMOS						X
HCI Lifetime	NMOS						X
	PMOS					X	X
TDDB Lifetime	FEOL						
	BEOL					X	X
EM Lifetime	BEOL						X
Latchup	Device						
	Package						X
Thermal Acceleration	Tjstress					X	X
JH & Package	Tjstress					X	X
HTOL @ OD Voltage	@HSV					X	X

HTOL @ Higher BI/OD Voltage



Key Learnings On OD Quals

- Maturity of Process, Circuit Design and test programs.
- Design margin fails might appear at early tape-out / design verification stages → Difficult to separate
- If OD voltage is too high, extrinsic fails will appear mixed with intrinsic fails even in ELFR stage.
- Keep sort yield pareto to separate major killers
- Best to implement OD BI after:
  - Product design & process are mature and stable.
  - Baseline pass the process and product Quals.