BiTS 2017

Heating Up - Burn-in & Thermal Test



Burn-in & Test Strategies Workshop

www.bitsworkshop.org

March 5-8, 2017

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Session 5 Rahima Mohammed	BiTS Workshop 2017 Schedule			
	Frontier Day			
Session Chair	Tuesday March 7 - 10:30 am			
<u>Heating Up</u>				
"Process Improvements to Increase Burn-In Yield and Quality"				
Jeanette Linn, Rich Karr - Texas Instruments				
"Device Characterization Over Temperature at the Board Level"				
Barry Johnson - inTEST Thermal Solutions				
"Qualifying A Process For Higher Burn-In Voltage Application"				
Krishna Mohan Chavali - Globalfoundries US Inc				
"Coming Challenges and Opportunities for MEMS				
Testing Supply Chain"				
	Wendy Chen - KYEC			
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Device Characterization Over Temperature at the Board Level

Barry Johnson inTEST Thermal Solutions



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Contents

- Temperature IC characterization methods
- Isolating temperature to component level
- Reaching & maintaining DUT temperature
- Establishing a test environment
- Handling moisture
- Other thermal system considerations
- Pros and cons of temperature methods



Semiconductor device characterization over temperature at the board level

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Two Scenarios





Temperature characterization on load board Troubleshooting temperature related problems to device level



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The Vanilla Temperature Chamber

- Slow response: 2 to 5°C/min
- Frost free with purge
- Cannot isolate individual comps
- Signal integrity, test equip is not near DUT





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Temperature Forcing

Fast: 18°C/sec

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- Dry, frost-free environment
- Signal integrity improved
- Temperature confined to a more contained "region"



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Direct Contact Conductive Conditioning

- Isolate to component level
- Fast transition times: 40°C/min
- Small & conducive to lab environments
- Handles IC power fluctuations well





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Thermal Bridge

- IC Package defines the X, Y area
- Board topology defines Z height & shape
- If test socket used, socket will define height and shape
- Thermal performance at DUT varies with different ThermoBridge designs



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Thermal Resistance

- f(Volume, Dimensions, Material)
- Expressed in °C/W
- Example:
 - Thermal bridge Resistance of 0.5°C/W
 - If the DUT dissipates 20W, there will be a 10°C delta across bridge
 - Therefore system needs to generate -65°C at Thermal head to achieve -55°C at DUT



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Response – Dissipation vs Capacity





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Minimizing Transitions Fastest way to set point is to drive temperature beyond and use DUT Control 180 150 120 Set point 90 **Thermal Head** 60 °C 30 DUT 0 -30 -60 0 50 100 150 200 250 300 350 Seconds Semiconductor device characterization over temperature at the board level 15 rn-in & Test Strategie

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Session 5 Presentation 2

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Other Considerations

- System capacity must exceed broader temperature range than test requirements
 - Provides faster ramp rates
 - Handles heat dissipation
- When going below ambient, frost will be an issue
- Junction temp using thermal diode requires an ideality factor close to 1.0



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The Test Environment

- Frost free setup
- Independent adjustable flow, top and bottom
- Thermal collar around head as barrier to ambient







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Temperature Method Comparison

	Thermal Chamber	Air Temperature Forcing	Direct Contact Temperature Forcing
Relative system response to achieve set temperature	Slow: 2-5°C/min	Fastest: 18°C/sec	Fast: 40°C/min
Thermal capacity to bring DUT to specified temperature	Yes	Yes	Yes
Ability to isolate temperature to DUT	Weak	Moderate	Strong
Handles IC power fluctuations	Weak	Moderate	Strong
Signal integrity	Weak	Strong	Strong
Frost elimination	Yes	Yes	Yes
Flexibility	Strong	Moderate	Weak
Footprint	Large	Moderate	Small



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Summary

- What method of temperature delivery is best
- Determine if DUT needs isolation from surrounding components
- Will system capacity handle power dissipation of DUT (Delta T)
- Where is temperature being measured (case, internal)



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