EIGHTEENTH ANNUAL
BiTS
TM
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 5
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Session 5

Rahima Mohammed
Session Chair

BiTS Workshop 2017 Schedule

Frontier Day

Tuesday March 7 - 10:30 am

Heating Up

"Process Improvements to Increase Burn-In Yield and Quality"

Jeanette Linn, Rich Karr - Texas Instruments

"Device Characterization Over Temperature at the Board Level"

Barry Johnson - inTEST Thermal Solutions

"Qualifying A Process For Higher Burn-In Voltage Application"

Krishna Mohan Chavali - Globalfoundries US Inc

"Coming Challenges and Opportunities for MEMS Testing Supply Chain"

Wendy Chen - KYEC

Process Improvements to Increase Burn-In Yield and Quality

Jeanette Linn and Rich Karr
Texas Instruments

BiTS Workshop
March 5 - 8, 2017

Table Contents

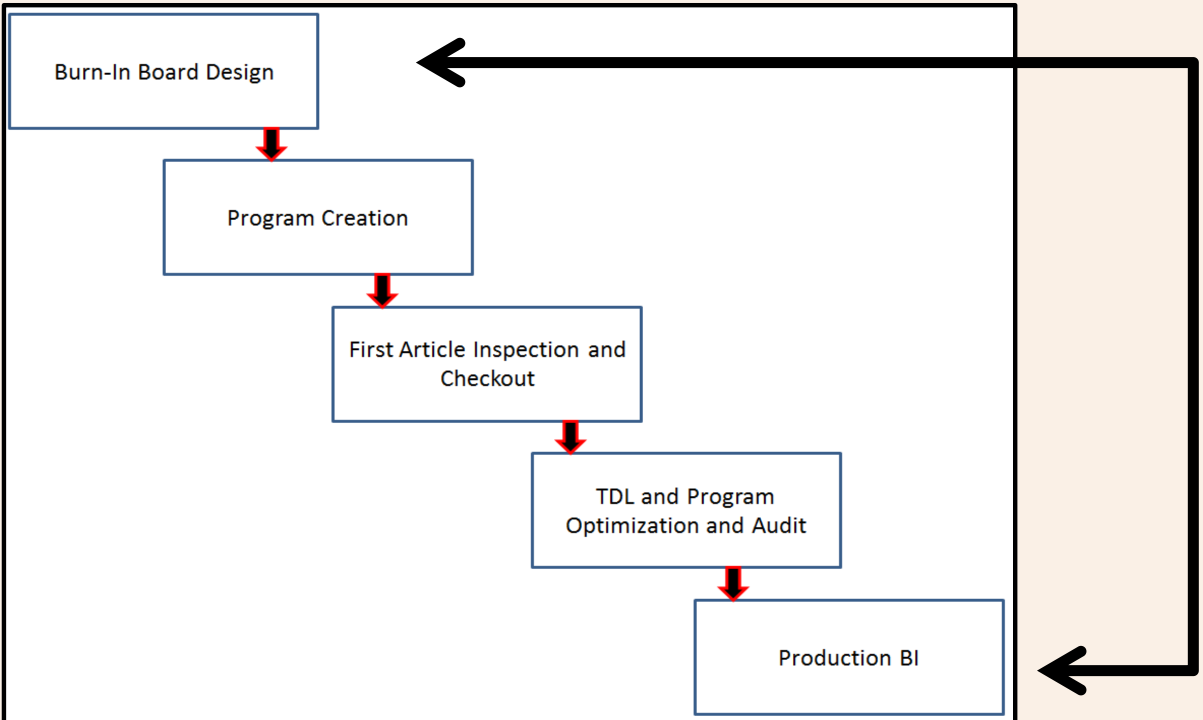
- Problem Statement
- Burn-In (BI) Development Lifecycle
- Burn-In Board (BIB) Design and Verification
- BI Program Creation and Audit
- Volume Manufacturing Issues
- Results

Problem Statement

- The challenge of identifying truly defective devices while preserving high yield and throughput during a new BI platform bring up, resulted in a call-to-action for root cause analysis and process improvement implementation.
- The high levels of undesired scrap were non-value added as the devices were not actually defective, but were instead failing the monitored burn-in insertion due to BI program and hardware instability issues.
- **Increased cost without improved quality!!**

BI DEVELOPMENT LIFECYCLE

BI Development Lifecycle



Quality improvement is dependent on all subsystems including, BIB, BI programs, oven operating system, oven hardware, and production processes.

BI BOARD DESIGN AND VERIFICATION

BIB Design Standardization

- Creation of centralized and standardized BIB design tools and requirements.
- Standardized BIB design template was created.

CUSTOMER INFORMATION			
Engineer Contact	Jeanette Linn	EDGE PCB DWG Title	PWA,Oven,BIB,SN1508017
Phone Number:	Phone number	PCB Manufacturer	IMakeBIBs
Email:	email	PCB EDGE #	1234567
Business Unit (SBE)	SBE	PCB EDGE # Rev.	A
Business Unit (LBE)	LBE	PCB EDGE ECR #	1234567

DEVICE INFORMATION			
Device Name	Device A	Device Pin Count	156
Device Alias	MoneyMaker	Package Type	AAA
Min Temperature	25	Socket Manufacturer	SuperSocket
Max Temperature	125	Socket Part #:	Socket123
Sockets Per Board	28	Burn-In Oven Manufacturer:	BI Oven Maker
No. of Socket Rows	4		
No. of Socket Columns	7	Burn-In Oven Used:	BI Oven

Color	Item
Yellow	DUT Pin Out
Orange	Resource Allocation and Conditions: I/O Assignments, Clock Connections, Monitoring Signals, Driver Termination
Green	Socket Information: Socket Diagram
Blue	Device Specific Requirements: Device Packaging Drawings, Device Schematic
Lavender	BOM
Red	Miscellaneous Information: Additional instructions the user wants to provide to vendor

BIB Vendor Requirements

- All vendors must use the same design tool
- Design tool has standard PCB templates for different BI ovens.
  - Keep out areas, Maximum height restrictions, etc.
- Library of TI approved parts and components
- This resulted in improved quality, and also enabled supplier comparison on performance and cost.

First Article Inspection

- Implemented FAI checklist based on lessons learned.

BI Hardware Verification		
Item	**Proceedure**	**Status / Results**
Socket Visual Inspection	Open socket, actuate contacts, inspect contacts	
	Inspect heater and sensor wires, also sensor button	
	Open and close heat sink, verify stress relief for wiring	
BIB Visual Inspection	Ensure all componenets are soldered on well	
	Ensure no electrical component is the highest point on the top or bottom of the BIB	
	Ensure the board does not flex when being loaded	
Device Socket Seating	Ensure that device seats in socket properly, inspect witness marks	
Empty BIB Power Up Checkout	Measure power supply voltage levels, check supply current readback for leakage	
Empty BIB Driver signal checkout	Scope clock and driver signals at both side of the socket isolation resistor	
	Check scope sync and expeted data signals	
Single Unit BIB Power Up Checkout	Measure power supply voltage levels, check device current readings	
	Scope clock and driver signals at both side of the socket isolation resistor	
	Compare expected data to device output	
Single Unit Socket Mapping Verification	Move 1 unit to all socket locations to verify the BIB mapping is correct.	
Fully Populated BIB Power Up Checkout	Measure power supply voltage levels, check device current readings	
	Collect detailed scope pictures of all the BIB supplies to ensure no drooping, overshoot, or noise etc for the entire BI flow all vectors.	
	Scope clock and driver signals at both side of the socket isolation resistor	
Debug / Checkout all delivered TDL (Fully Populated BIB)	Get all delivered TDL to pass robustly at all socket locations.	
	Collect scope pictures of each TDL. Need to include the cricital pins for that TDL.	
Power and Thermal Characterization	Complete power and thermal characterization with split lot material to ensure no issues are encoutered across process. Split lot material should pass production FT1. Yield team to select devices to ensure device process is well represented. Recommended minimum 3 parts per split. -- Run the entire BI program including all TDL at the maximum temperature and voltage expected (example production BI conditions). -- Run the entire BI program including all TDL at the minimum temperature and voltage (example lowest DPSE voltage leg): -- Ideally, run fully populated BIB with all hot parts at the maximum BI conditions --BI program exectution does not need to be the full duration program, it can be a reduced duration. Example 2 minutes per pattern. Note: Soak step needs to be the full duration. --Voltage, current, and temperature data should be measured at the maximum frequency allowable by the oven or OpAmp (ABTS). Note: For MCC oven can use the dutgraph tool to record measurements every 30ms. **Key Care Abouts/Concerns:** **What is the maximum current drawn by cold, nom, and hot units for each BIB supply throughout the BI program? --Does this match the power model well? Is there any unexpectedly high current? **If running a BIB fully populated with the hottest parts, will the board shutdown due to current starvation? --If yes, need to implement FT1 power sorting / BIB shredding	

BI PROGRAM CREATION, OPTIMIZATION, AND AUDIT

BI Program Creation

- BI program template and standardization of programs helped to reduce errors and allow data comparison across different devices. It also helped improve independent program audit quality.
- Pre-check step or checkout program required to run before production BI, including minimum good yield requirements.

BI Program Audit

- A formal BI program audit methodology was established.
- An expert auditor team was formed.
- The BI Program Audit Checklist was defined for different program release milestones.

BI Program Milestones

Item	Qual Start Requirement	Program Uprev Release Requirement	Applicable Y/N	Proceedure
BI Program Audit Checklist Completion	YES	YES		Ensure all checklist items were completed / followed.
BI Hardware Checklist Completion	YES	NO		Ensure all checklist items were completed / followed.
TDL Checklist Completion	YES	If new TDL, YES, else NO		Ensure all checklist items were completed / followed.
BI Yield Check	YES	NO		Yield check using tuned BIB, all TDL passing, run on split lot material that passes FT1 production flow. If less than 99%, what are the actions to increase the yield? Need to also review all BI logs collected to date including FAI checkout, LA qual, qual, production, etc to see if there are any yield issues that need to be addressed. Please provide link to data analysis.
Power Char	YES	NO		Please refer to the cell link for details. MCC can use DUTGraphTool ABTS can use OpAmp output to observe device current and voltage.
Thermal Char	YES	NO		Complete thermal characterization using split lot material to ensure no thermal issues. Optimize the thermal control to minimize temperature overshoot / undershoot.
BI Start / Offload	YES	NO		Confirm all BI locations on all BIBs are passing, if not, repair or mask off. Run 4 fully populated BIBs for 24 hours. If ABTS need to run baords in both zone 0/1, side by side. Analyze BI yield to be sure 100% passing BI results. Analyze all ATE pre to post BI shift for potential issues
Burn In Uprev Checkout	NO	YES		Run minimum 1 fully populated BIBs for production duration. Analyze BI yield to be sure 100% passing BI results.
Documentation	NO	NO		Did you confirm your BIB spec is uploaded onto hardware design documentation website? Is it correct and matching the BIB design and actual BIBs?
	YES	NO		Complete the scope work including: Supply power up, supply power down, supply noise, device clocks, TDL functionality Ensure you have all scope work is labled and posted to Twiki/Sharepoint. Please provide the link to the scope work. -
	YES	YES		Documentation page: Do you have documentation posted for testplan, BIB hardware, TDL status, BI program information, BI program conditions, thermal and power char, lessons learned, and labled scope work? Example page is linked. Please ensure all sections are included and documented.
	YES	YES		All BI Programs need to be uploaded to test program archive site.
Full team audit, PE + BI audit team to audit everything	YES	NO		BI Audit team + device PE team to perform thorough review of all BI documentation and results.
BI audit team only	NO	YES		BI Audit team to review / audit all checklists and documentation completed by the BI engineer.

BI Program Audit Checklist

BI Program Audit Checklist			
BI Platform	**Power Supply / Voltages**	**Yes or No**	**Comments / Links to Data**
All	What is your power up / power down sequence? Does it match to the device datasheet requirements? --> Please be sure to double check this for each program release to make sure nothing was accidentally changed.	Yes	Power up sequence does match the defined Apps/ datasheet order. However, there is a known high power mode on VDDSHV* supplies that is being debuged by the team.
All	Does your device require to be in reset or any other pin ties during power supply ramp?? If yes, supply scope pictures with tie pins controlled correctly during device power up and down.	Yes	PORz = L is required during device power ramp. We do have the pull down on this pin as well as driving L on the POR vector that is executed before and during supply ramp up and down. Collected the supply power response on power down that shows the low power state during device power down.
All	Do you have scope pictures to show you have a controled power up / power down? Did you confirm that there are no under or overshoots present. Please provide the link to the scope work.	Yes	Detailed scope work is completed and posted here:
All	Did you check to ensure your PS voltages are correct for BI? I.e. Do they match the PDK BI voltage spec for your device? Think EFR vs. HTOL vs. DPSE. Please provide the link.	Yes	DPSE is using Vmax conditions. Confirmed Vmax voltage levels with PE team and yield team member. Vmax = Vnom + 5%.
Oven A	Did you check to ensure your checkout program voltages are correct? Example DPSE and HTOL cannot use EFR checkout program. This is to avoid over voltage stress for any duration.	Yes	Yes, checkout program created with DPSE voltage levels
All	Did you check to ensure that your driver VIH does not exceed your IO power supply voltage? Please provide programmed value.	Yes	VIH = 1.79v and 3.0v. VDDSHV = 3.465v and vdds18 = 1.89v
All	Did you check to ensure your VIH drivers level is correct for all pins connected to oven drivers?	Yes	There are 2 VIH levels, only 1 pin is 1.8v level. All olthers are 3.3v level.
All	Check to make sure your regulators are linked. Want all supplies to shut down if any supply shuts down.	Yes	Regulators are linked
All	Power Supply Clamps: Are your supply clamps set based on the device requirements / power char, not the maximum oven capability?	No	Since split lot characterization is not completed, current clamps are not well defined, many supplies do not allow for maximum current, but are not optimized yet. Material used for DPSE is nominal / not split lot

TDL Audit Checklist

TDL BI Requirements			
Item	**Applicable Y/N**	**Proceedure**	**Status / Results**
No Include Files		TDL must be standalone. No include files are allowed.	
Scan Blocks		TDL cannot contain any scan blocks. Serial scan data must be unrolled.	
Block Repeats		TDL cannot contain any block repeats.	
Matched Loops		TDL cannot contain any matched loops (commented out or not)	
Die ID Requirement		Die ID TDL must have continuous output (128 Bits).	
Clocks must be toggled		Device clocks must be toggled to prevent asymmetric aging.	
BI TDL		PE to analyze BI TDL to ensure it fits within the PE / BI test requirements	
TDL ATE Checkout		TDL Shall be checked out on the ATE , before BI Conversion	
TDL Strobes		TDL must have at least 1 H and 1 L strobe to ensure no stuck state (010 or 101)	
TDL Strobes		TDL must not strobe any 'additional' pins. The only strobes should be on the MBI pins. PBIST TDL can also strobe the pbist_done signal.	

Test Description Language was created by TI in 1980 and is still the primary format for handing off test patterns from design to product engineering.

VOLUME MANUFACTURING

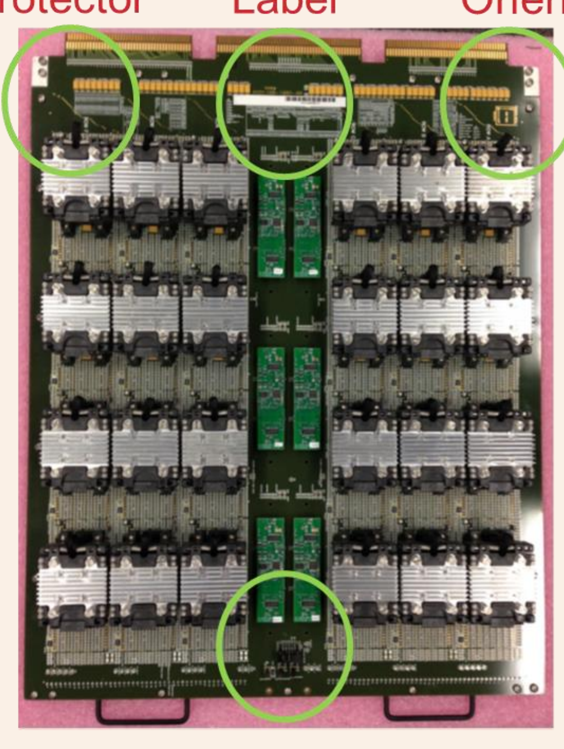
Standard BIB Template Features

Topside

Protector

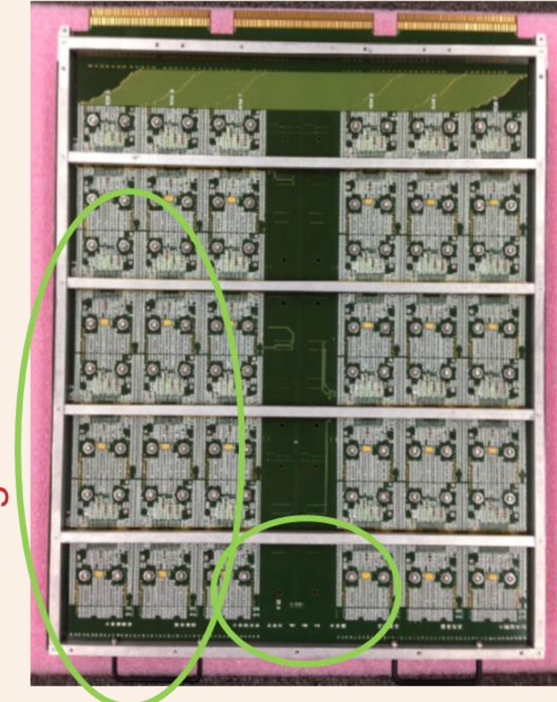
Label

Package Orientation



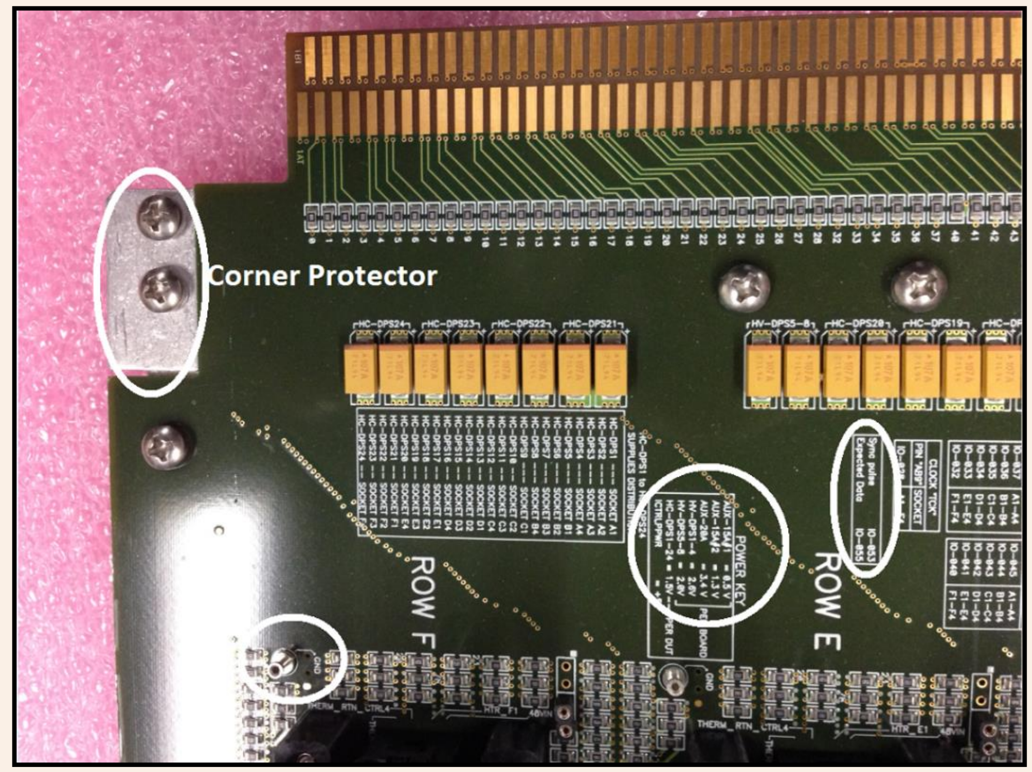
Bottomside

BIB Edge & Frame

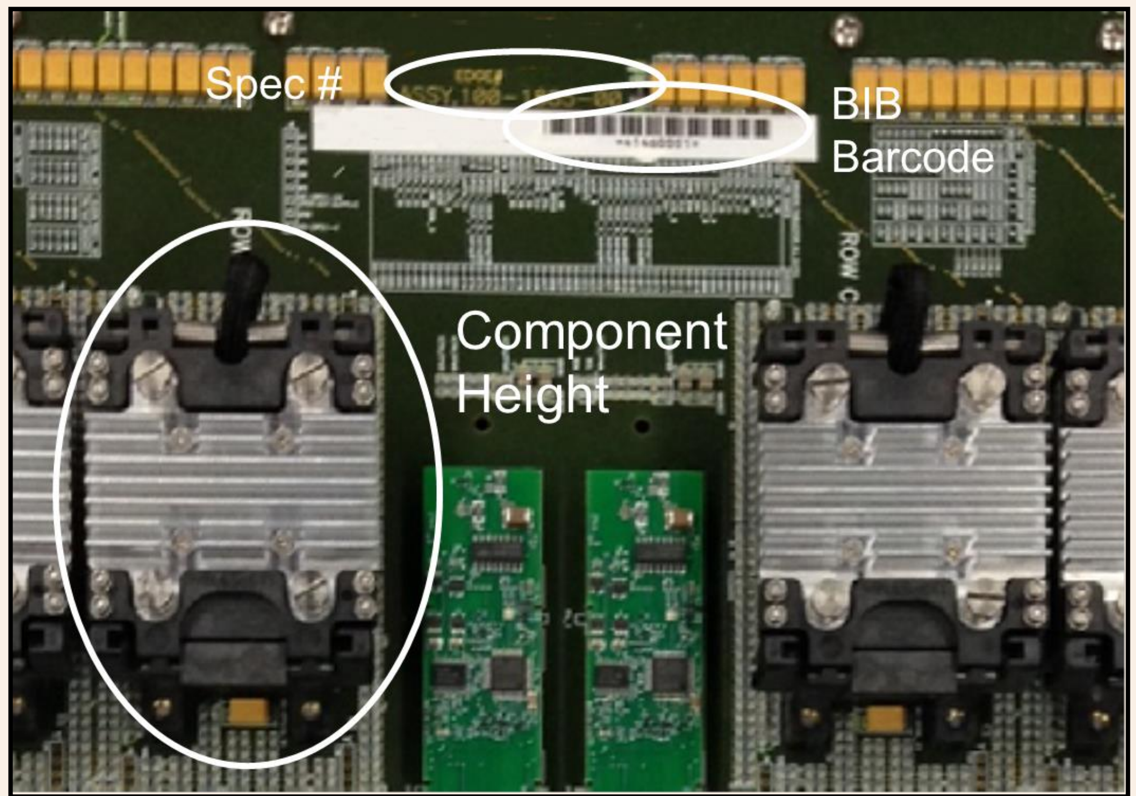


BIB/Socket Stiffeners

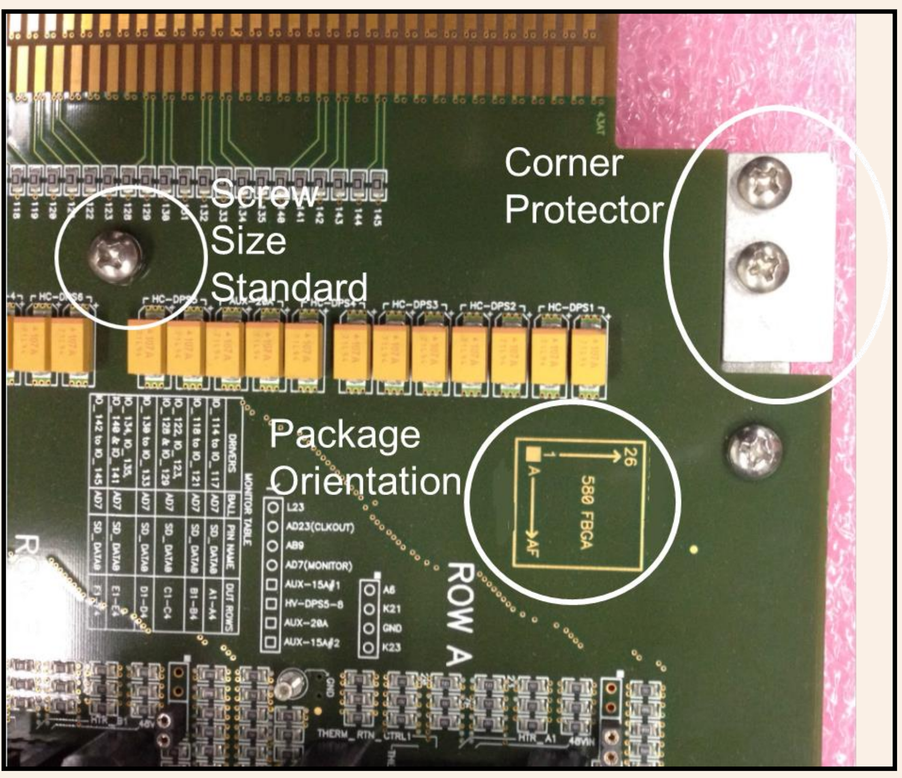
Standard BIB Template Features



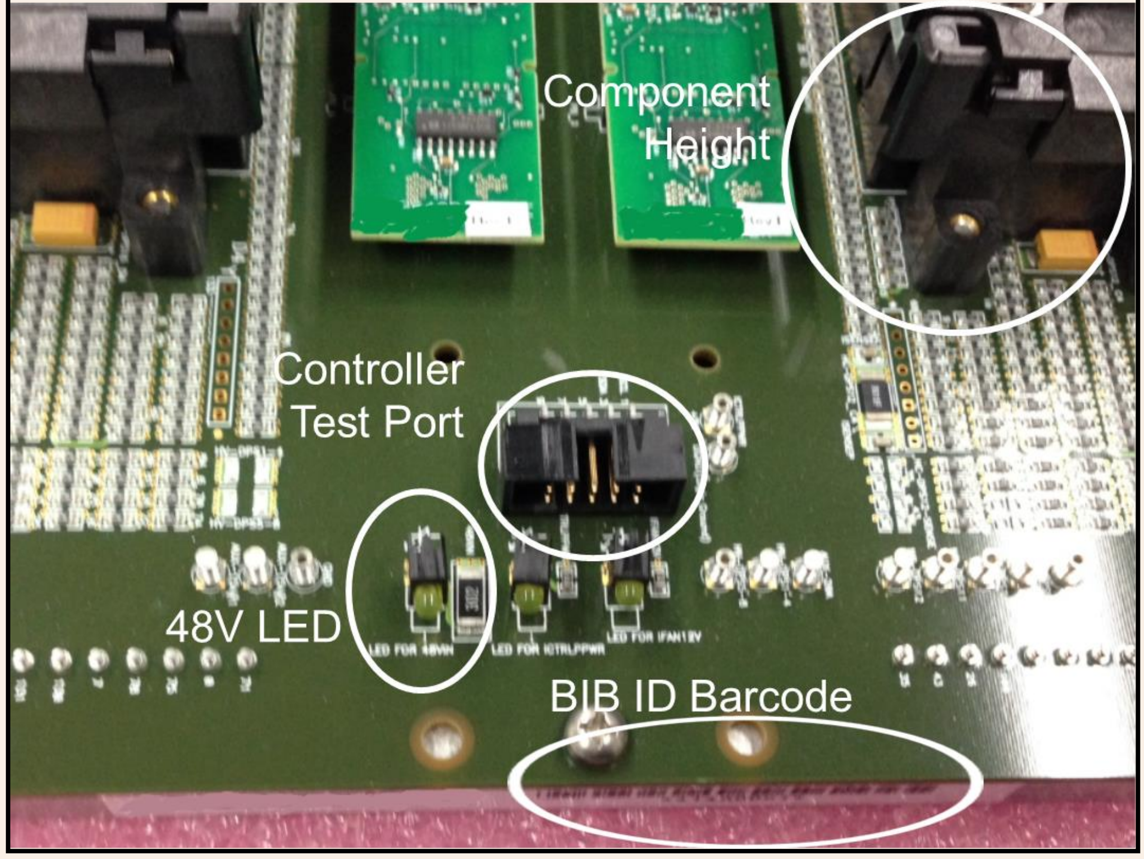
Standard BIB Template Features



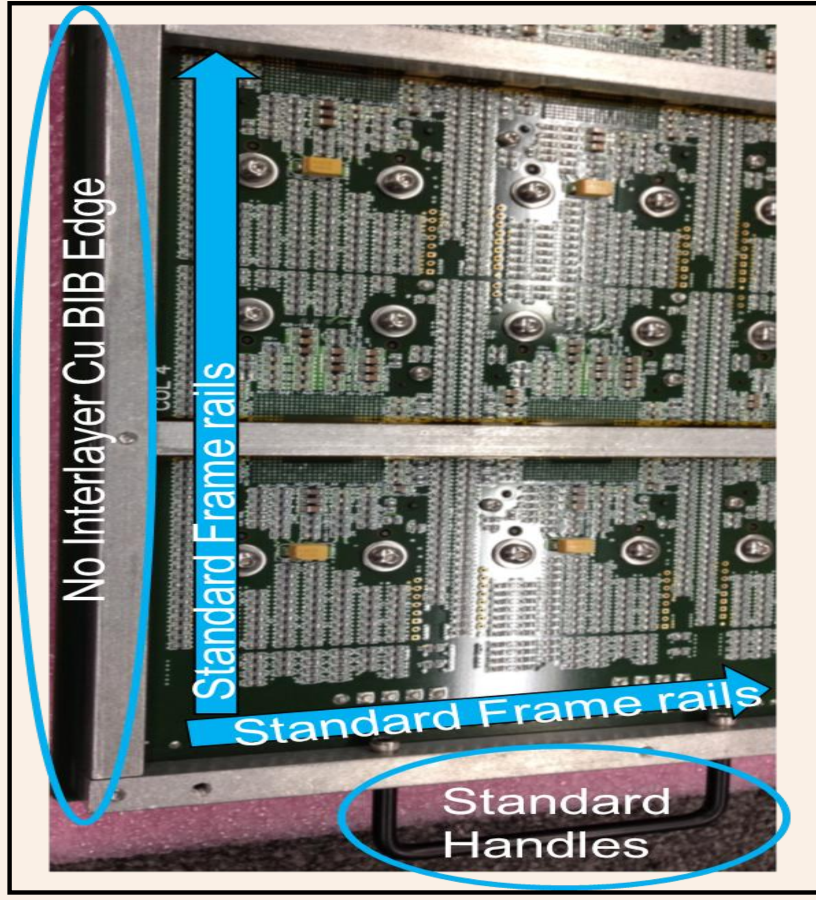
Standard BIB Template Features



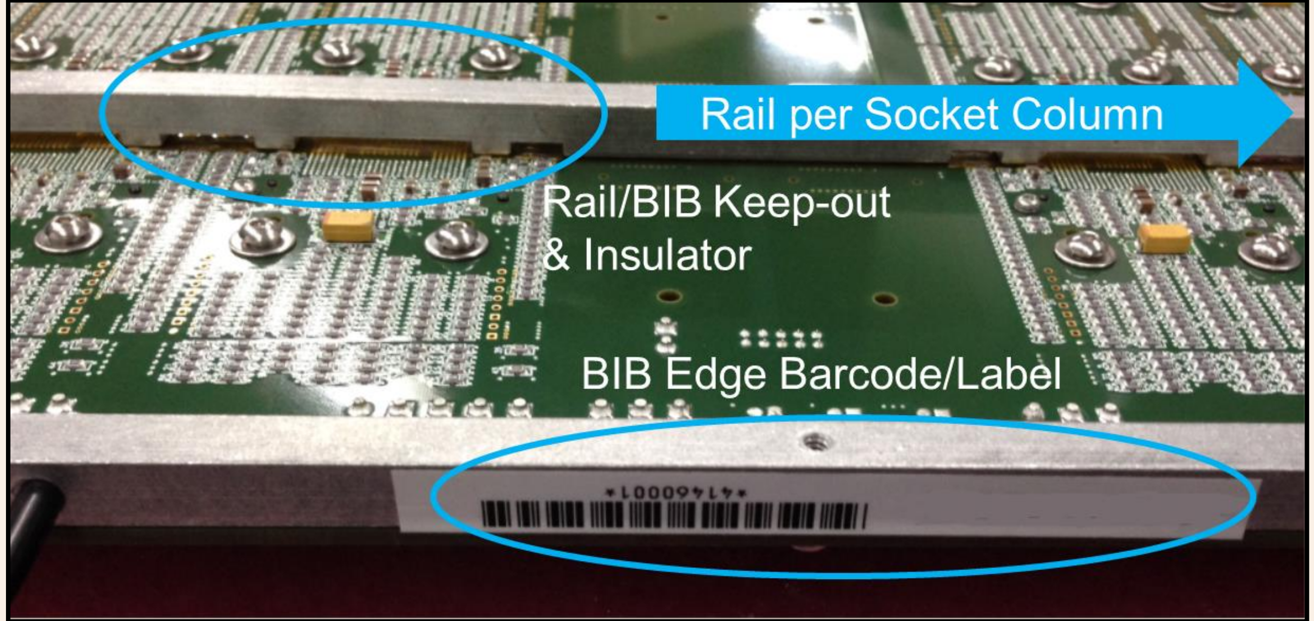
Standard BIB Template Features



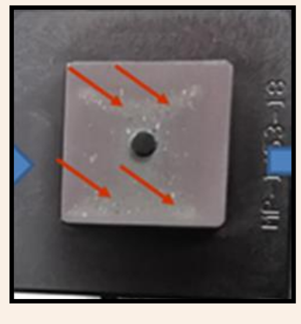
Standard BIB Template Features

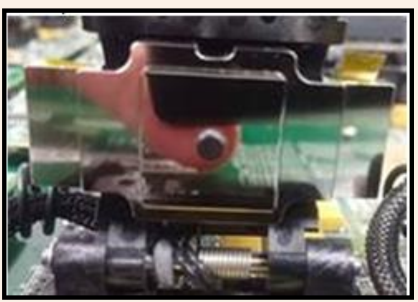


Standard BIB Template Features

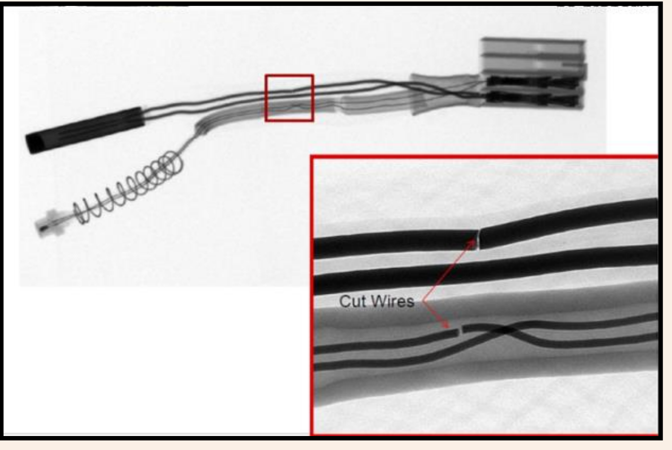


Hardware Issues and Improvements



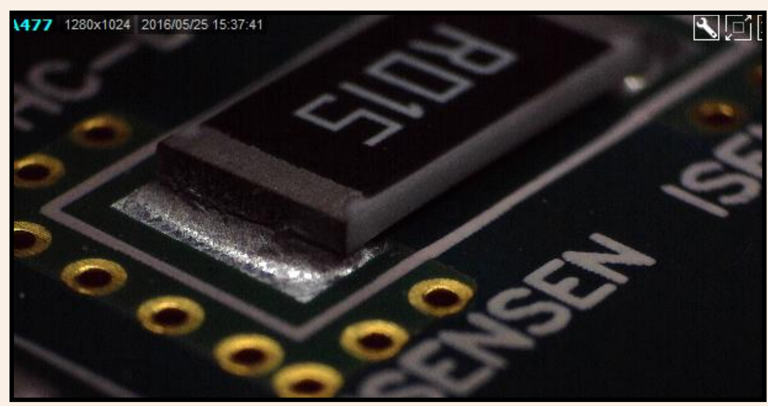


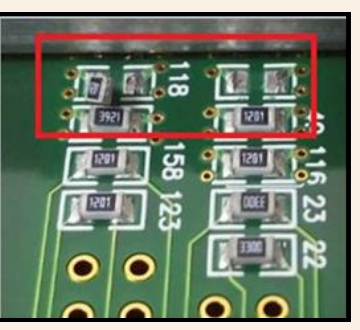
- Socket Boss Surface Roughness Spec
- Socket Heater Supply On Voltage LEDs
- Solid Core → Multi-Stranded Socket Wire
- BIB Rail Change Al → Stainless Steel

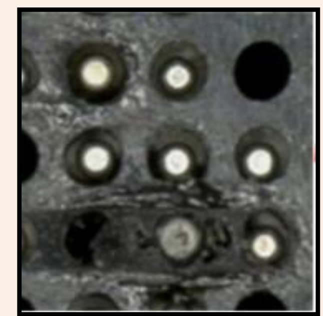


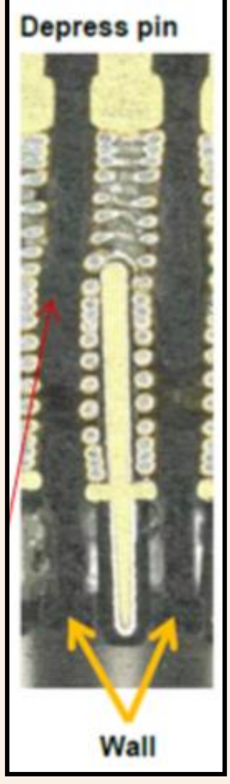
Hardware Issues and Improvements

- Improper Keep Out Area
- Socket Pin Stuck / Melted
  - Resulted in detailed socket qualification process.
- Isense Resistor: Surface Mount → Axial
- Temperature controller vendor change









Software Issues and Improvements

- Additional supply fault and thermal fault program bins were created to provide granularity to aid in yield improvement activities.

```
50, "'F' UnderTemp");
51, "'F' OverTemp");
52, "'F' HIGH_WCS");
53, "'F' HIGH_HTR");
54, "'F' HotDevice");
55, "'F' THERMAL_SENSOR");
3,  "'P' EORSF");
41, "'F' OverCurrent" );
43, "'F' OverVoltage" );
44, "'F' UnderVoltage" );
56, "'F' GoodTime_Fault" );
45, "'P' INCOMPLETE" );
2, "'F' TEST_FAIL" );
1, "'P' EBin_1" );
```

Software Issues and Improvements

- Oven diagnostic test cases were fixed to address coverage gaps.
  - Modified for better per channel details as opposed to channel groups.
- Oven operating system was updated to resolve many issues.
  - Yield calculation updates for masked sockets and good bin acceptance.
  - Disallow operator from unmasking masked sockets.
  - Added hardware serial numbers to test database.
  - Added unique compile id to run reports.
  - Email notifications upon slot faults

Manufacturing Process Improvements

- Improved preventative maintenance and oven cleaning. Quarterly PM → Daily PM.
- Oven diagnostics are now run daily.
- BIB maintenance not completed regularly→ Weekly
- Production operators used to be subcontractors → TI employees, have direct control / influence
- Oven hardware fault tracking including closed loop resolution.
  - Weekly call with factory and oven manufacturer ensure the feedback loop from production to vendor.

Manufacturing Process Improvements

- BIB maintenance not completed regularly→ Weekly

Type	Defect Name	Defect Description/ Criteria	Samples
Socket	Damage pins	Bending of socket pins. Any deformation of socket casing and pins caused by electrical surge or massive heat	
	Damage top cover	Broken or missing top cover and guide post	
Burn In Board	Damage edge finger	Any broken, crack or burnt gold finger	
	Damage edge protector	Any crack, deformed edge protector or corner	
	Missing/Damage components	Any detached terminal, burnt or broken components	
	Missing/ Loose screw	Any broken, missing and loose screws	
	Barcode sticker (applicable for BIBs running in ALU)	Detached, worn out, faded or dilapidated barcode sticker	
Heatsink	Damage heatsink lock and TIM	Any bent, broken and worn out heatsink lock and thermal interface.	

Infrastructure Improvements

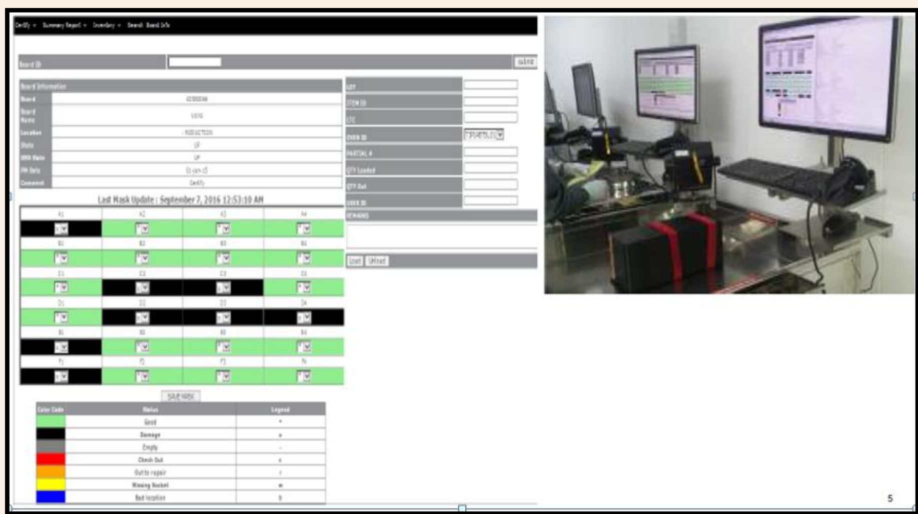
- Infrastructure improvements were implemented including:
  - Addition of BIB loading tables
  - Paper to electronic conversion
  - Data handling / software / database creation
  - Exhaust system and air handling improvements to reduce pin electronic heat
  - Dampener installation to reduce oven vibrations

The Power Of Data

- Per socket BI test data uploaded to database for interrogation.

BIB Maps

- Electronic BIB loading / unloading Maps using BIBID barcode



- Automated BIB Map loading to the oven

Hardware Decertification

- Automated BIB and socket decertification system based on pre-determined set of rules.

OVEN_STOP_TIME	A1	A2	A3	A4	A5	B1	B2	B3	B4	B5	C1	C2	C3	C4	C5	D1	D2	D3	D4	D5	E1	E2	E3	E4	E5	F1	F2	F3	F4	F5
9/6/2016 14:29	1	90	90	1	90	90	90	90	1	1	1	3	1	90	90	90	2	1	2	1	1	1	1	3	1	90	1	2	1	1
9/6/2016 8:39	1	90	90	1	90	90	90	90	1	1	1	1	1	90	90	90	3	1	1	1	1	1	1	2	1	90	1	2	1	1
9/6/2016 2:08	1	90	90	1	90	90	90	90	1	1	1	2	1	90	90	90	1	1	3	1	1	1	1	2	1	90	1	2	1	1
9/5/2016 21:13	1	90	90	1	90	90	90	90	1	1	2	1	1	90	90	90	3	1	1	1	1	1	1	2	1	90	1	1	1	1

Oven and BIB Management

- Oven management tool created which provides at a glance oven / slot status information.
- BIB Management system providing socket availability, decertified boards, repair history and success rate.

BI Yield Tracking

- High level yield tracking per program helped to identify problem areas.

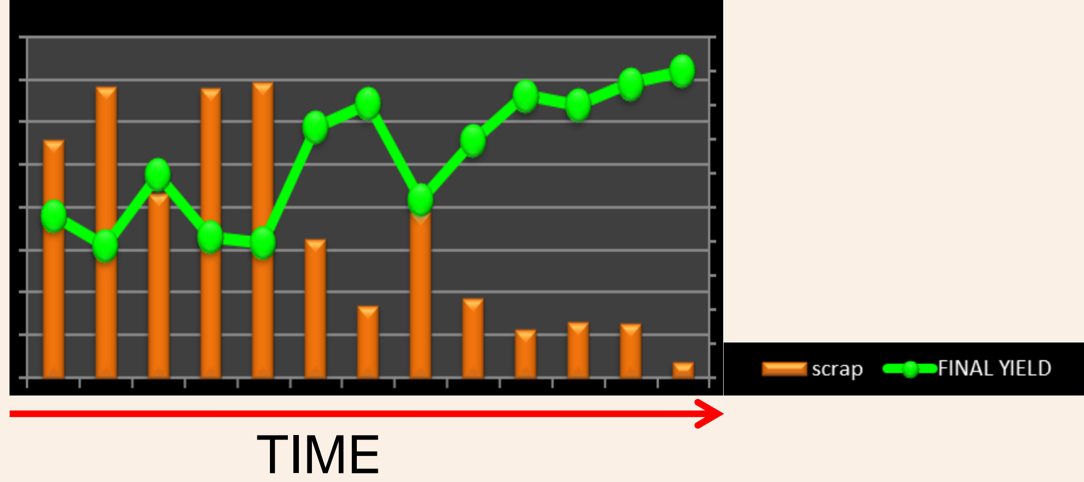
Burn-In Summary Yield Report by BI Program

Report date: 12/15/2016
Start date: 11/1/2016
End date: 11/30/2016
Run mode: RUN
TIPI as of: 12/15/2016 22:59
Display All Yield Bins: ☑
Next Page
Display Format: Web Excel

BI PROGRAM	CAT1 UNITS	CAT2 UNITS	CAT3 UNITS	CAT4 UNITS	CAT90 UNITS	CAT91 UNITS	QTY IN	SLOT FAULTS	QTY-IN PER FAULT	SLOT LOADS	FAULTS PER SLOT LOADS	FPY	PROCESS YIELD
Program A	254	0	0	0	1	0	254	0		17	0.00%	100.00%	100.00%
Program B	26,010	449	9,988	477	4,990	226	36,924	21	1,758	1,505	1.40%	70.44%	98.71%
Program C	33	66	100	0	114	23	199	0		14	0.00%	16.58%	100.00%
Program D	277	210	412	34	1,204	13	933	4	233	86	4.65%	29.69%	96.36%
Program E	89	1	1	0	101	8	91	0		8	0.00%	97.80%	100.00%
Program F	19,081	18,387	4,767	2,334	9,666	1,029	44,569	68	655	1,256	5.41%	42.81%	94.84%
Program G	7,542	4,046	574	935	2,596	235	13,097	27	485	362	7.46%	57.59%	92.86%
Program H	627	4	16	0	60	13	647	0		15	0.00%	96.91%	100.00%
Program I	121,985	2,588	7,191	983	64,699	1,126	132,747	42	3,161	4,513	0.93%	91.89%	99.26%
Program J	119,534	1,831	4,461	606	15,292	1,348	126,432	21	6,021	4,471	0.47%	94.54%	99.52%
Program K	686	4	27	42	171	30	759	1	759	20	5.00%	90.38%	94.47%

Conclusion

- Attacked total Burn-In Operation and Device Burn-In Solution development including boards, sockets, programs, equipment, process and infrastructure, resulting in higher yield and throughput.



Acknowledgements

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