
EIGHTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 3
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Session 3

Ila Pal

Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 4:30 pm

Reality Check

"Augmenting form factor designs with validation and debug capability"

John Kelbert - Intel Corporation

"New Possiblity with Coax Via Risers"

Matthew Priolo, Adrian Rodriquez, Christopher Kinney, Adewale Oladeinde – Intel

"Processes for Validating and Maintaining Electrical DUT Interfaces"

Martin Gao, Carolina Lock - Texas Instruments

Processes for Validating and Maintaining Electrical DUT Interfaces

Martin Gao, Carolina Lock
Texas Instruments

BiTS Workshop
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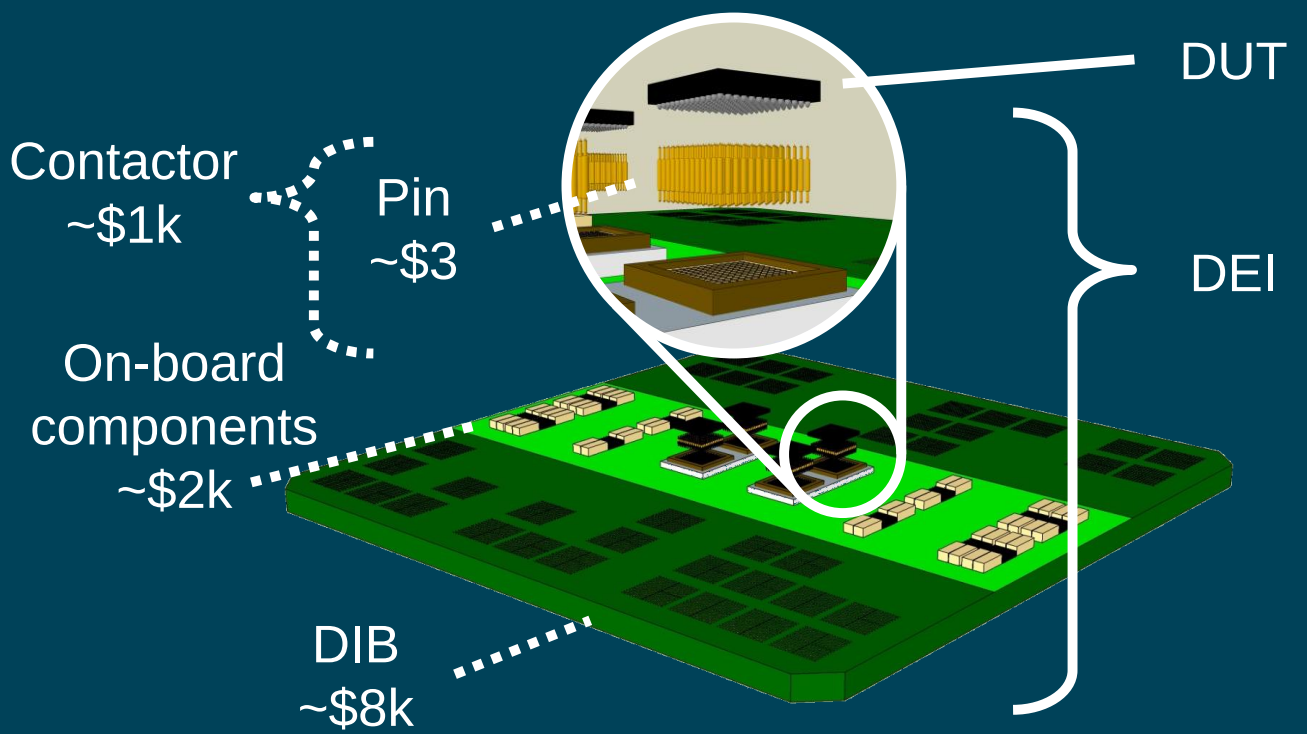
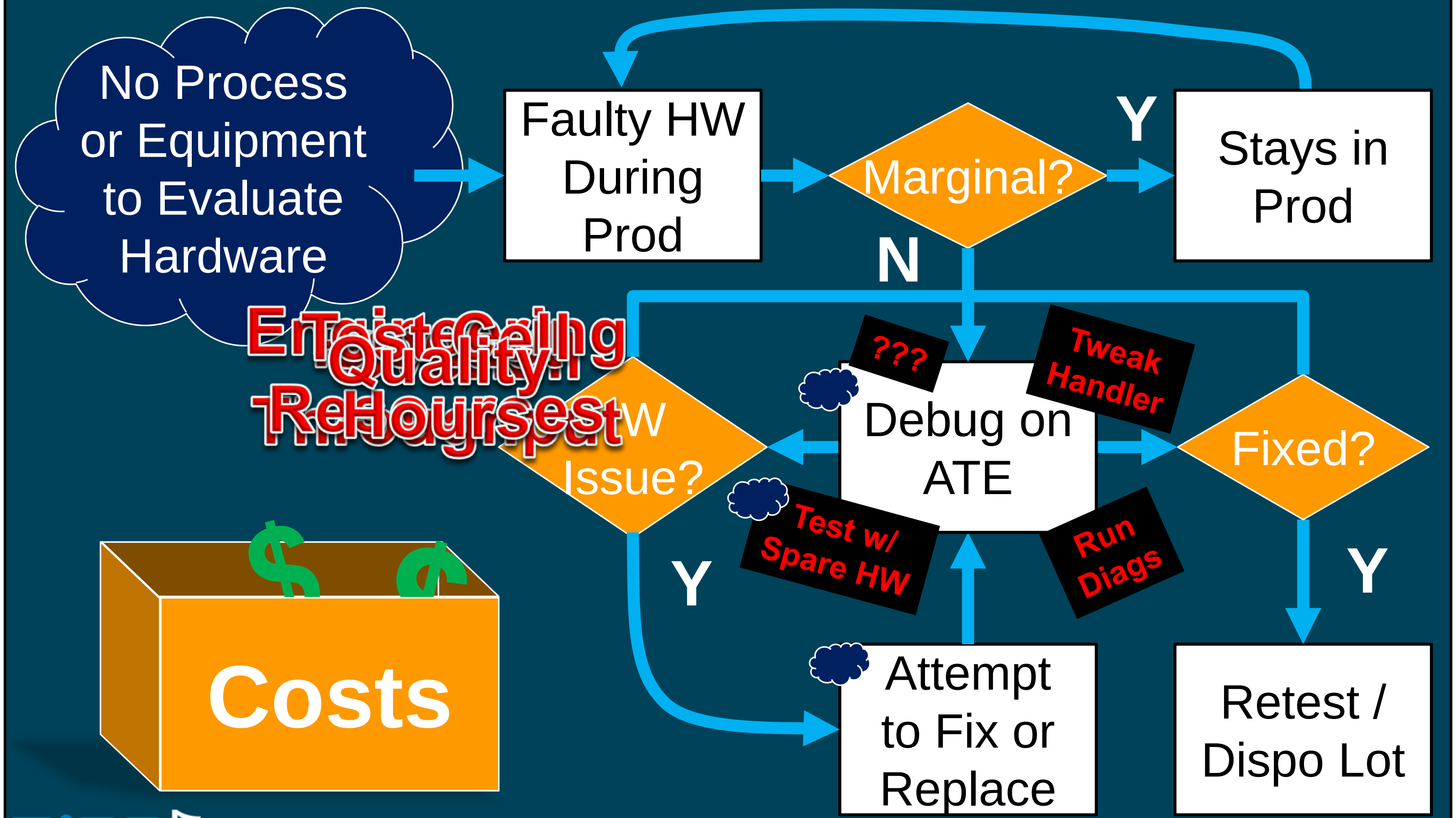
Contents

- What & Why
- Proposed Processes
- Current Development
- Data
- Final Thoughts

What: Improve DUT Electrical Interface (DEI) Above ATE

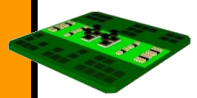


Why: No Process/Equipment = Money, Time, and Resource Costs

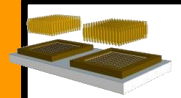


Proposed Processes

New Product Acceptance

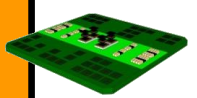


Vendor pre-screen with SEICA*

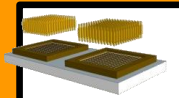


Factory qualify contactor with respective test cell at various temperatures

Production Release

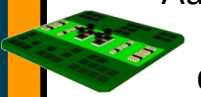


Factory verify with SEICA*

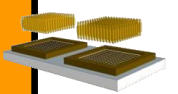


Factory cycle contactor to spec'd # of insertions & periodically test CRES using *dedicated* tester (not ATE)

Preventative Maintenance



Automatically flag HW for PM at designated # of insertions & device yield thresholds

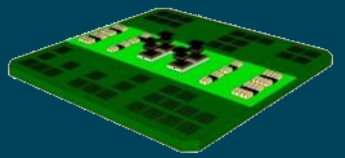


Gate release to production on passing evaluation

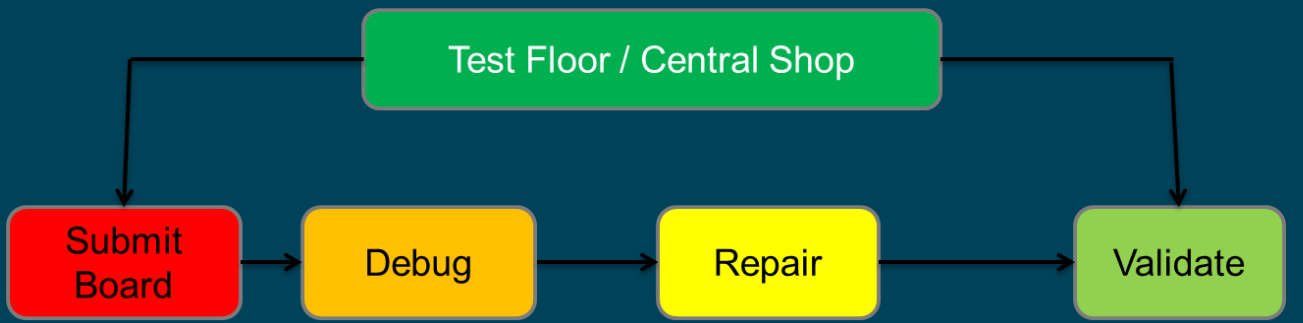
Required Infrastructure

Automatic Data Logging and Movement to Central Locations
Repair Shop & Vendor Standardizations

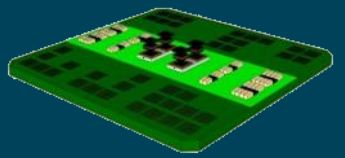
*SEICA: flying probe tester – conducts point-to-point component and PCB testing



Current Development

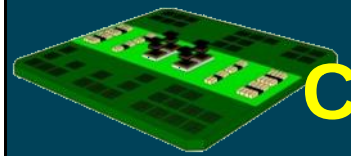


- ATE boards breakdown due to:
  - Active components (relays, switches, muxes)
  - Passive components (resistors, capacitors, etc)
  - Broken solder joints
  - Internal PCB trace / material breakdown
- Downed boards are tracked via S/W



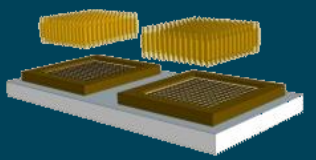
Current Development

- Debug with SEICA V8 flying probe tester
  - Run VIVA programs created with board
  - Log all failures for repair into tracking S/W
- Shop technicians repair boards
  - Replace broken components using appropriate repair equipment (soldering iron, preheater, etc)
  - Reorder new spare boards for more serious issues
- All repaired boards are validated on tester before releasing back into prod



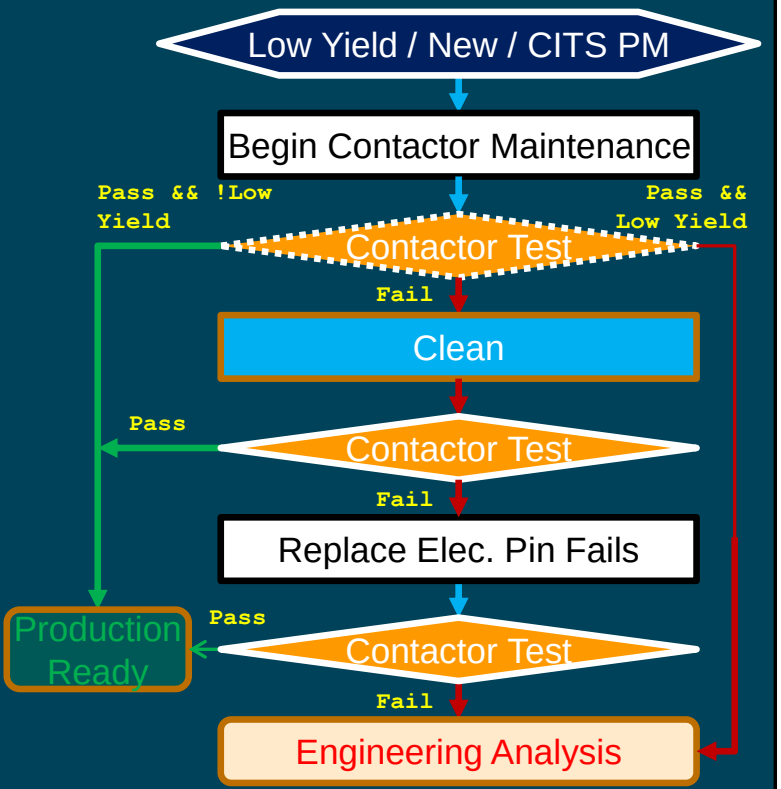
Current Development: Tester

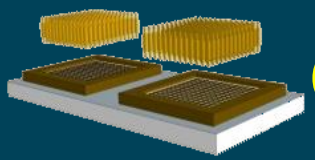
- SEICA Pilot V8 Flying Probe Tester
  - Component Assembly Check
  - Identifies manufacturing errors and component defects
  - High level of test coverage
  - 2-sided testing with 8 probes
  - Standardized probes
  - On probe CCD cameras
  - Easy to debug GUI
  - Generate programs with CAD data



Current Development

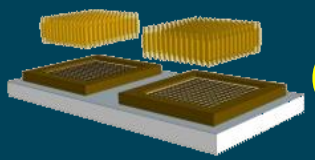
- Contactor Insertion Tracking System (CITS)
  - Trigger PM based on insertion counts
- Contactor Test
  - Dedicated tester in Repair Shop, does not impact production capacity





Current Development: Tester

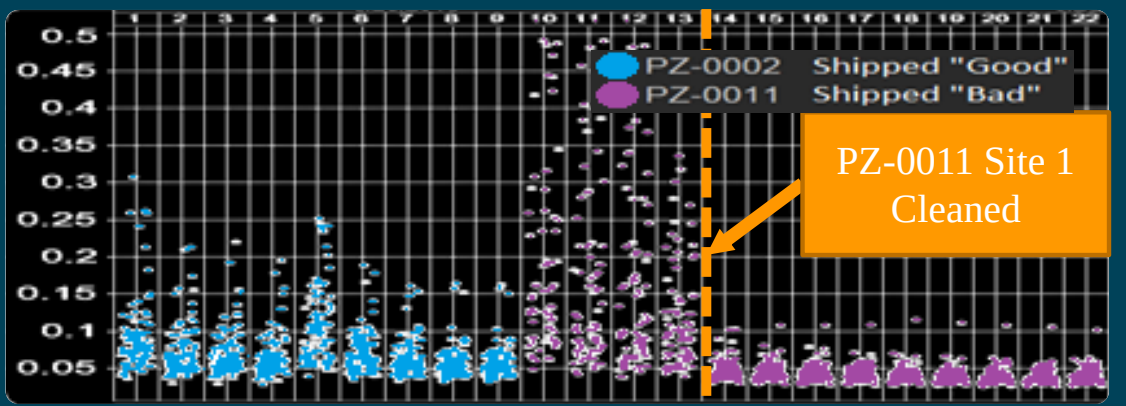
- MPT™ Parametric Tester
  - 4-wire Kelvin per-pin CRES (±1.5mΩ to ±200μΩ precision)
- MTC™ Cycling Station
  - Force and displacement (±1.5kg and ±1μm resolution)
- Extras
  - Cognex In-Sight Micro
  - Multi-Nest pusher attachment
- Considerations
  - Interface Items: PCBs, Nests, Simulators, Attachments, etc.
  - No per-pin force isolation



Current Development: Tester

TI Frames - "Bad" vs "Good"

Socket Per-Pin CRES w/ Cycling In-Between (Ohm)



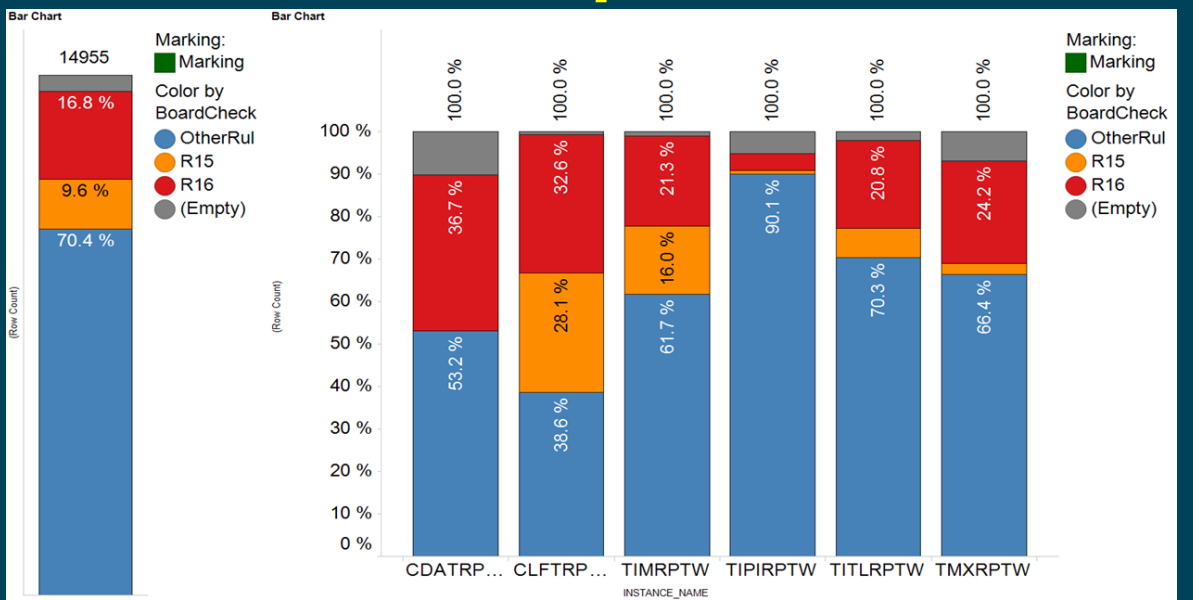
Average Lifetime Tracking

- Software Tracking
  - Repair shop centralized S/W tracks amount of board breakdowns per units tested (insertions)
    - Average ATE PCB expected to breakdown between 1.6-3 million insertions – not counting new boards with design issues
  - Contactor Insertion Tracking System (CITS) tracks the lifespan of contactors (insertion count)
    - Average insertions between cleaning 5-8K
    - Average insertions between pin change 45-65K

Test Coverage Improvement

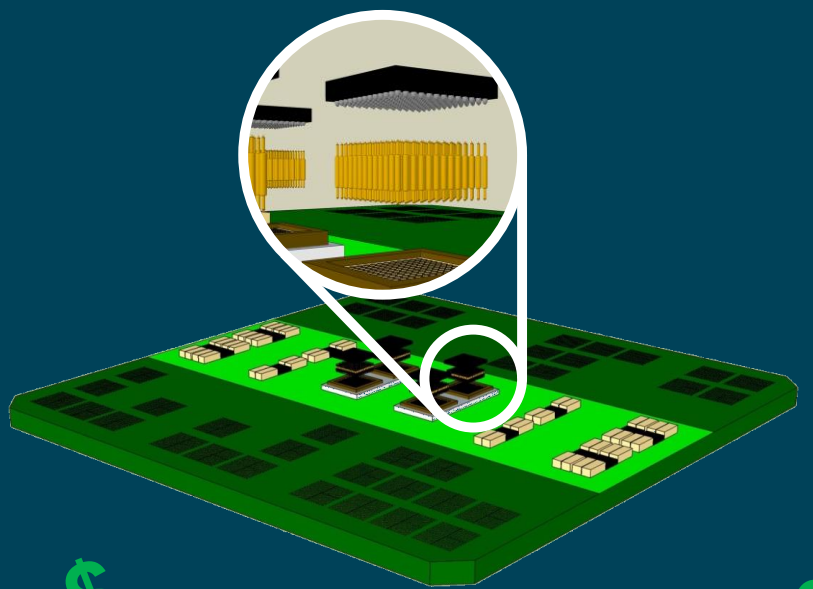
- DIB Diag vs SEICA % coverage
  - Average DIB Diag coverage 70-80% of all on-board components
  - SEICA V8 coverage 95-97% of all components
- SEICA – speed of debug increased
  - SEICA program average run time 30 minutes
  - Average manual debug time – 1 day
- Contactor speed of debug increased
  - Contactor checker average run time 30 minutes
  - Average manual pin-change – 2 hours + pin cost

Overall Improvement

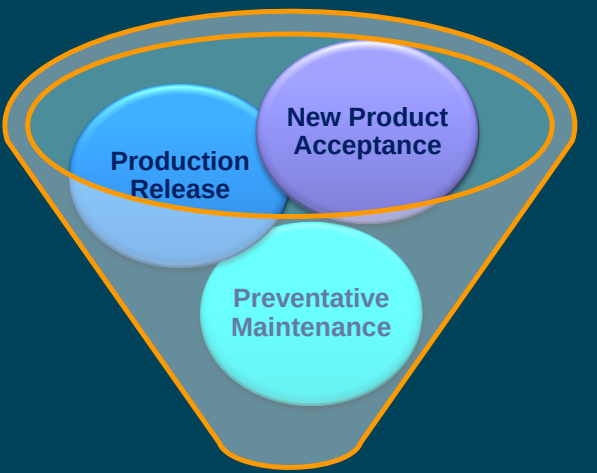


- Before DEI improvement efforts
  - DEI issues 33% of all ATE downtime
- Estimated 10-15% of downtime after improvement effort

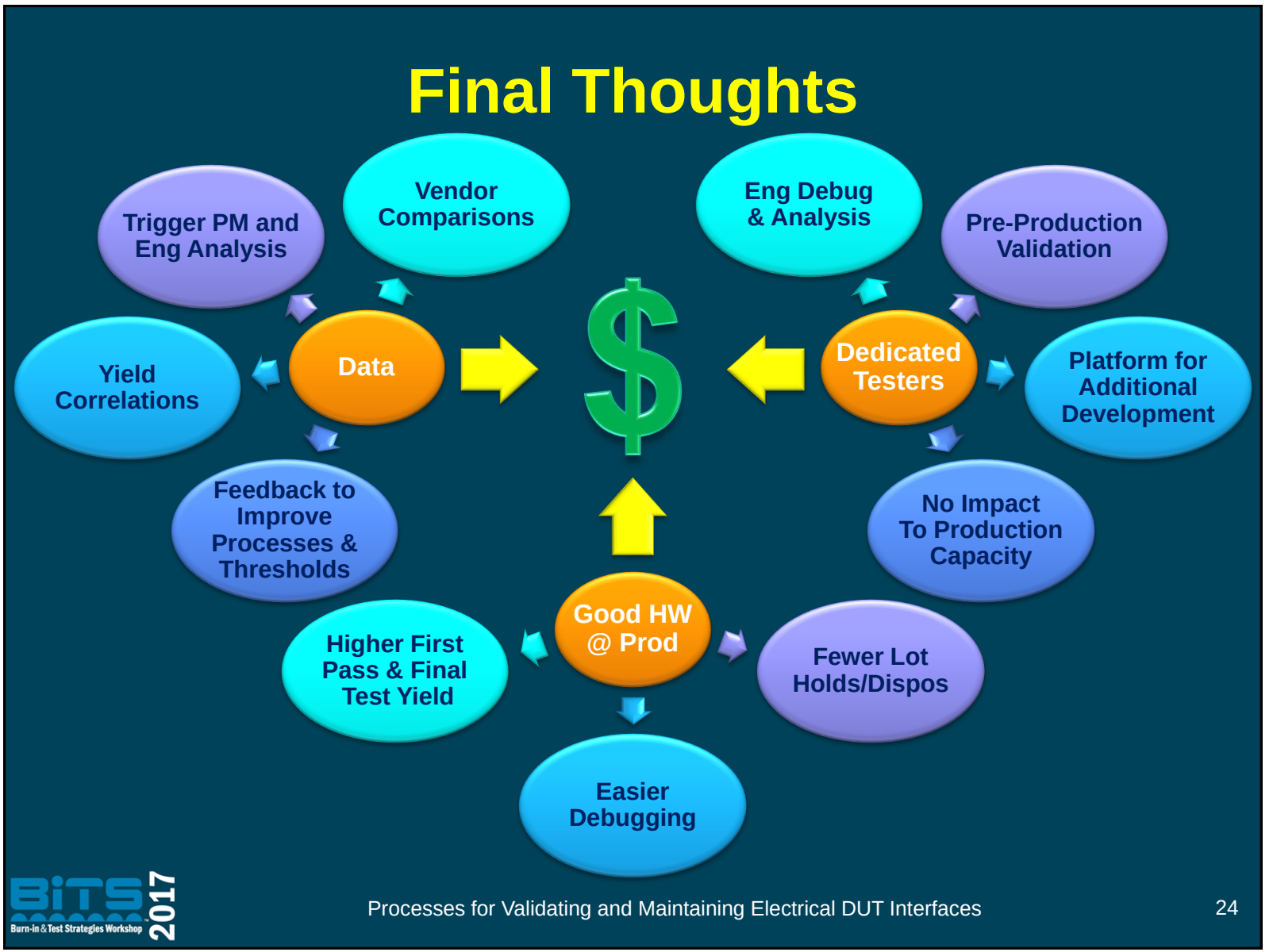
Final Thoughts



Develop Standardized Processes for Evaluation and Maintenance



Faulty DIB / Contactor Interfaces Lead to Yield, Resource, Capacity, etc. Costs


Final Thoughts
Vendor Comparisons
Trigger PM and Eng Analysis
Eng Debug & Analysis
Pre-Production Validation
Yield Correlations
Data
$
Dedicated Testers
Platform for Additional Development
Feedback to Improve Processes & Thresholds
No Impact To Production Capacity
Good HW @ Prod
Higher First Pass & Final Test Yield
Fewer Lot Holds/Dispos
Easier Debugging
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