
EIGHTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 3
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Session 3

Ila Pal

Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 4:30 pm

Reality Check

"Augmenting form factor designs with validation and debug capability"

John Kelbert - Intel Corporation

"New Possiblity with Coax Via Risers"

Matthew Priolo, Adrian Rodriquez, Christopher Kinney, Adewale Oladeinde – Intel

"Processes for Validating and Maintaining Electrical DUT Interfaces"

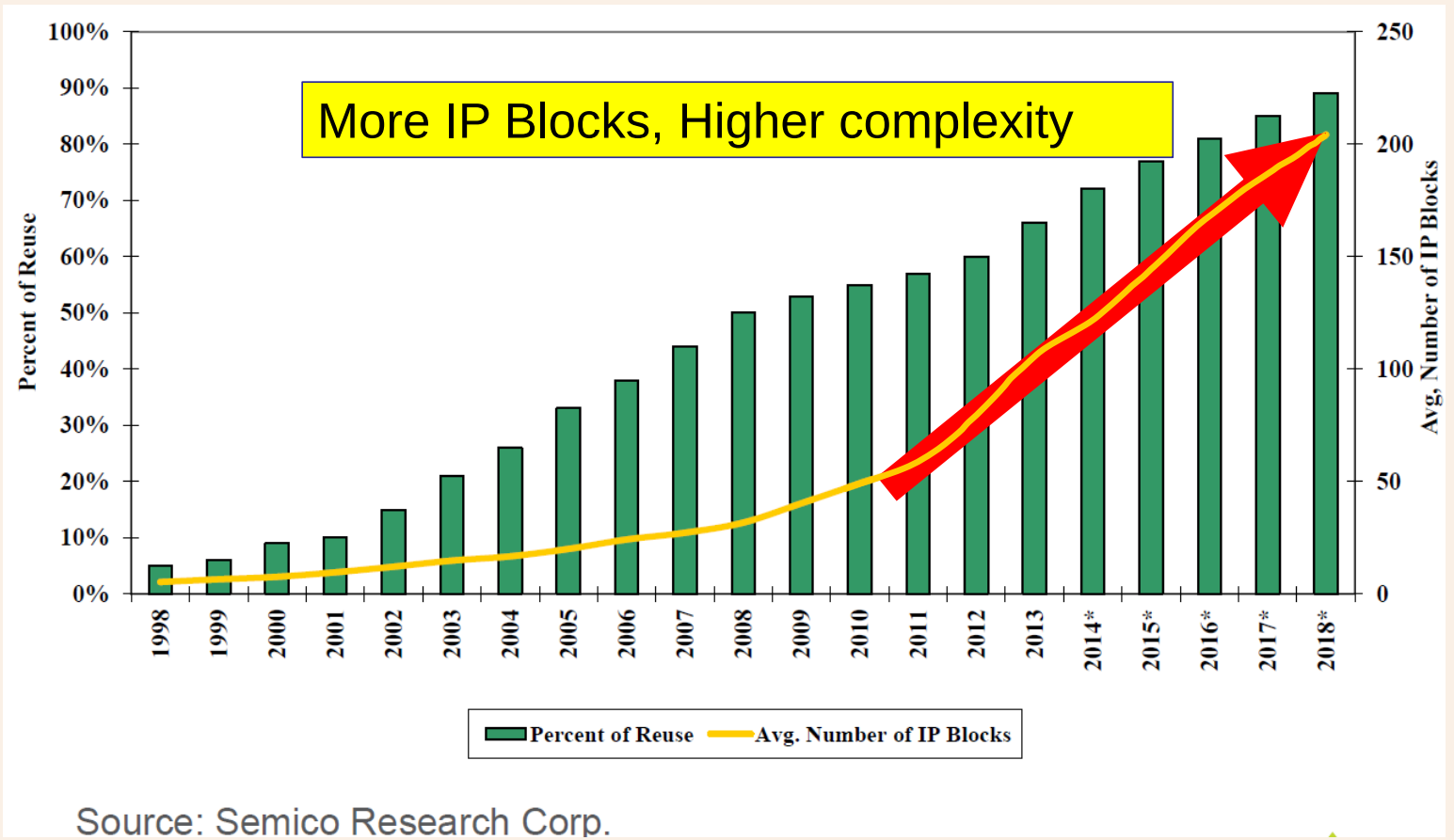
Martin Gao, Carolina Lock - Texas Instruments

Augmenting Form Factor Designs with Validation and Debug Capability

John Kelbert
Intel Corporation

BiTS Workshop
March 5 - 8, 2017

Product Complexity Rising



Source: Semico Research Corp.

Product Cadence Unchanged

GSMA MOBILE WORLD CONGRESS

CES

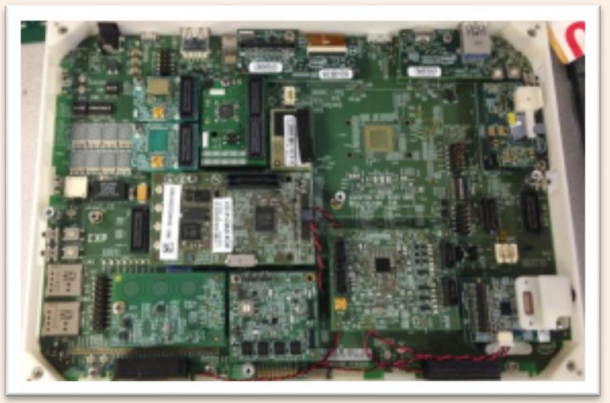
Reality – Many Products are Late

"..79% of new products miss the launch date[1], companies have an enormous opportunity to increase sales and profitability by improving new product time to market (TTM)[2]"

[1]CGT/Sopheon Survey

[2]https://www.sopheon.com/new-product-time-to-market/

Complexity Management with Multi-step Platform Approach



Initial debug platform

Start with this

- Easy to access
- Easy to debug
- Modular, reconfigure

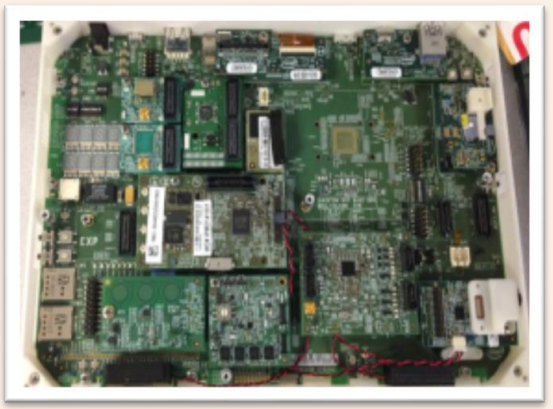
Complexity Management with Multi-step Platform Approach

Progress to this →

End point: product

- Difficult to access
- Challenging to debug
- Fixed configuration

Complexity Management with Multi-step Platform Approach



Starting point: debug platform

- Easy to access
- Easy to debug
- Modular, reconfigure

End point: product

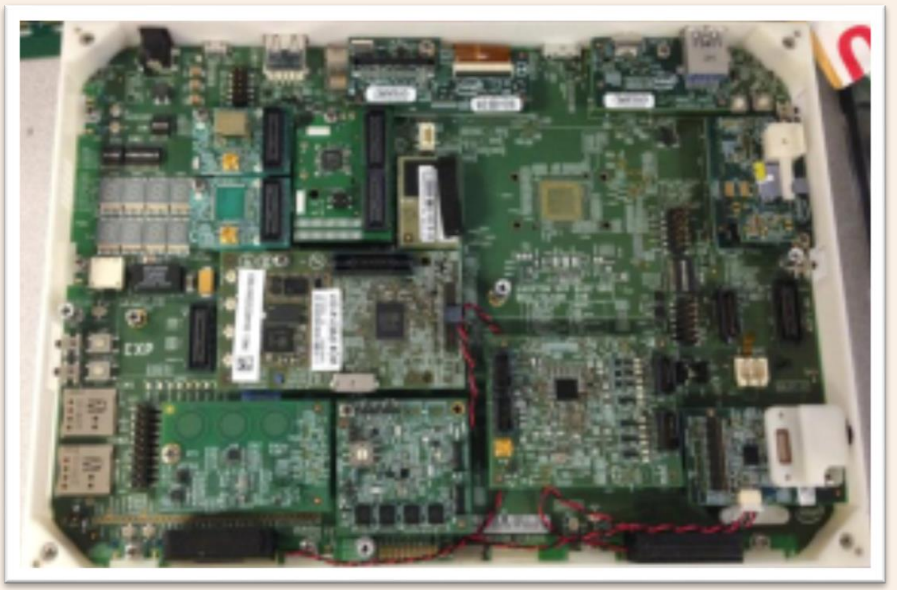
- Difficult to access
- Challenging to debug
- Fixed configuration

Complexity Management with Multi-step Platform Approach

- All the while avoiding shortcuts that could lead to disaster

Upside of Multi-step Platform

- Advantages of specialized test platforms
  - Flexibility, expose key interfaces, added instrumentation, capability, …



Initial starting point

Downside of Multi-step Platform

Initial starting point

Complexity added here…

Disadvantages

- PCB layers added for debug and test
- Longer routing of critical interfaces
- Connectors added to modularize
- Added test points
- Mounting holes for sockets

Downside of Multi-step Platform

Initial starting point

Key Differences

Power and Performance
Drivers, FW/BIOS
Component placement
PCB stackup
Signal Integrity
Power Integrity

End point

Complexity added here…

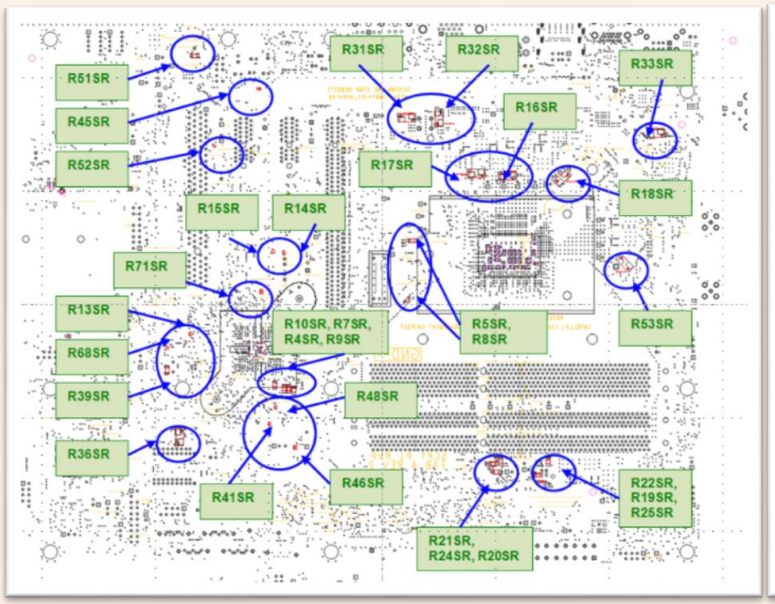
Compromises efforts and investment to get here.

POWER AND PERFORMANCE PRODUCT TUNING

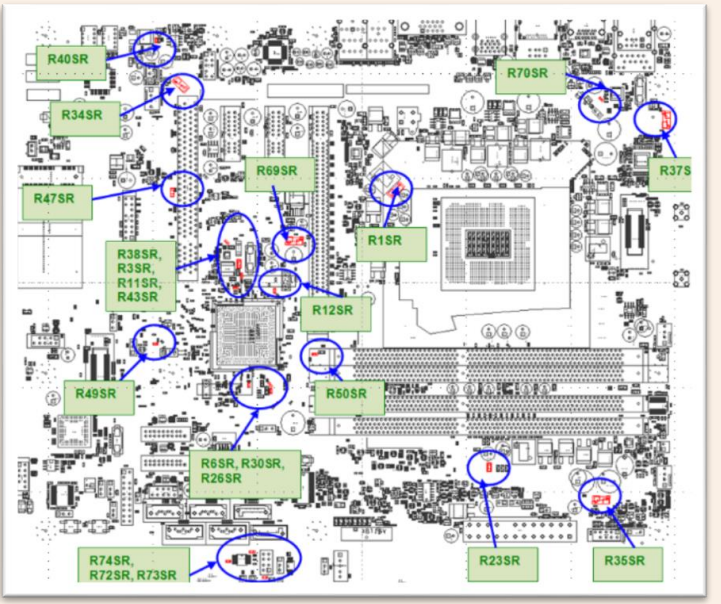
Multi-step approach example:

Designing in complexity

Example: Power and Performance Board Layout



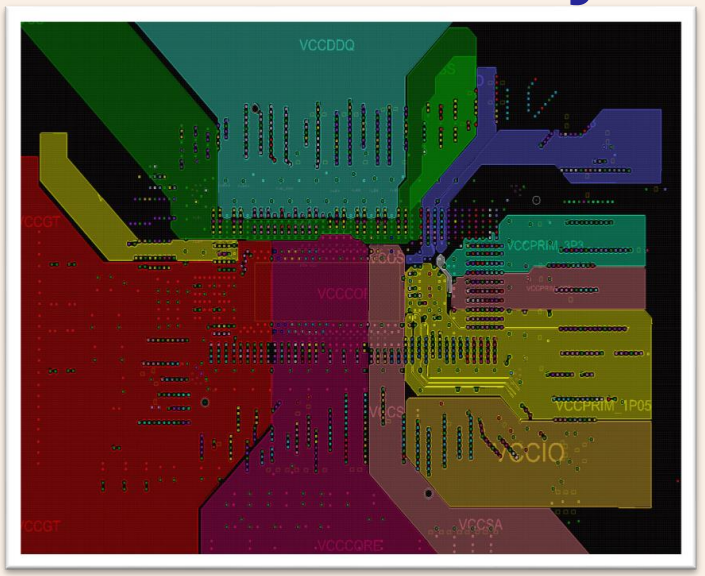
PCB placement bottom view

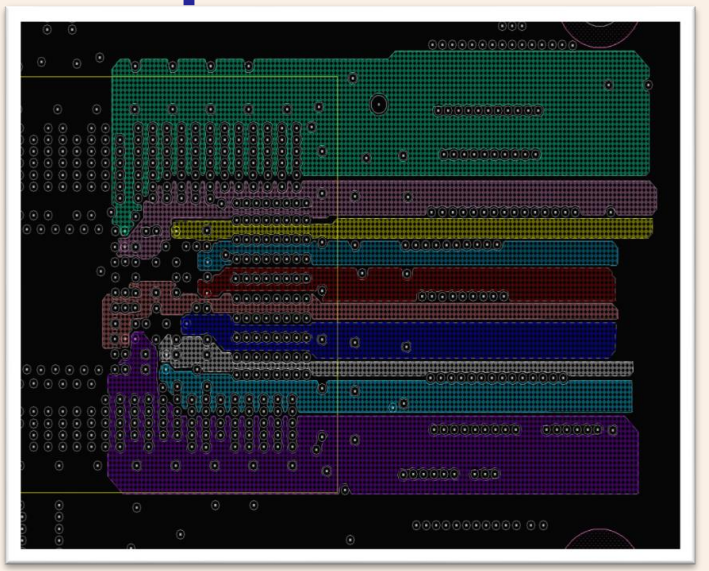


PCB placement top view

53 current sense resistors added to tune power-performance product point

Example: Power and Performance Power Layout Compromise





- Recommended product power shapes
- Product component placement

- Compromised power shapes for instrumentation
- Component placement pushed out from SoC

Example: Power and Performance Physical Connections

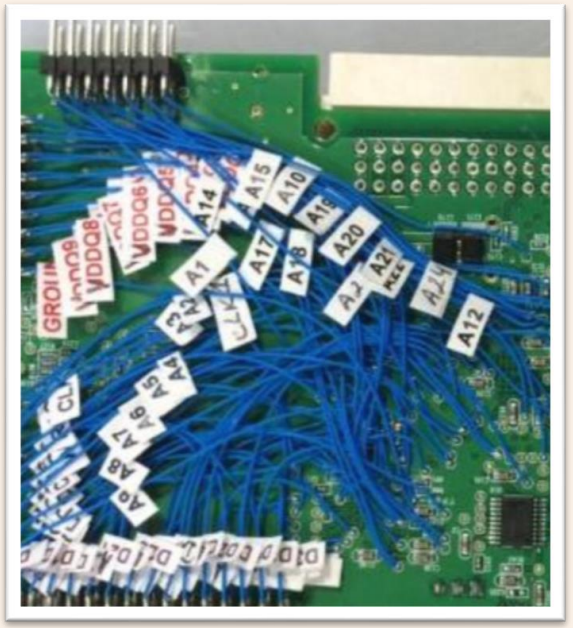
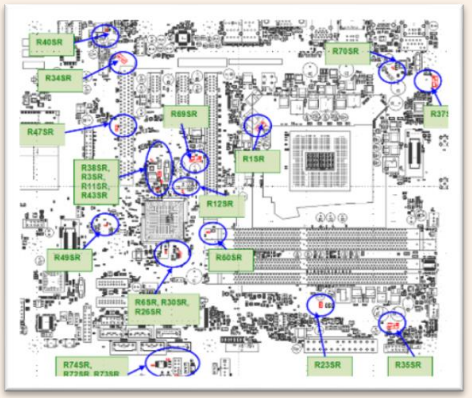


Image: Best Inc.

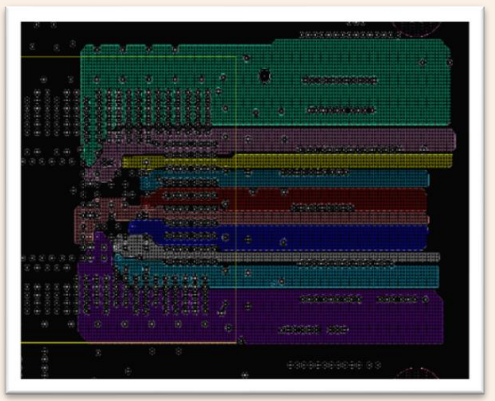
Blue wires connections added for data acquisition equipment

Consequences

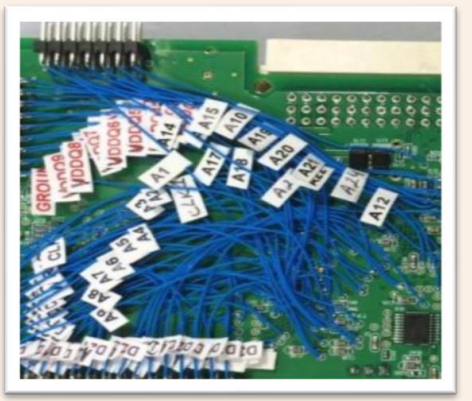
Non-product deviations



Placement



Layout



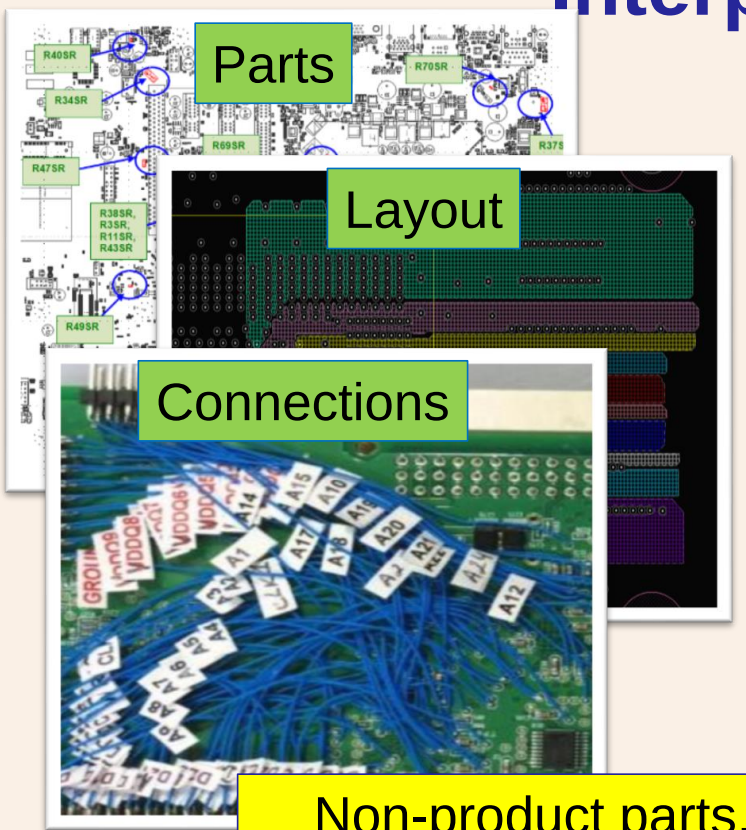
Debug Features

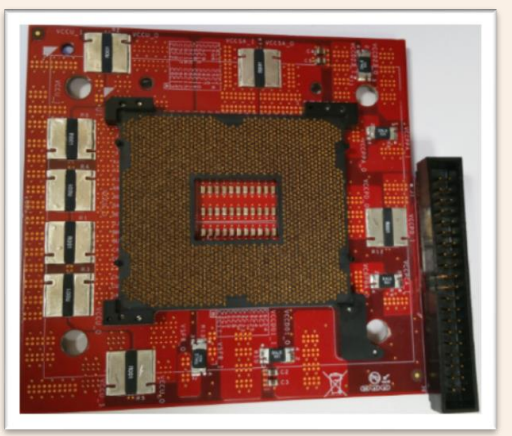
Deviations irrelevant to final product

AUGMENTATION WITH INTERPOSERS

A different approach

Move Test Feature Complexity to Interposers

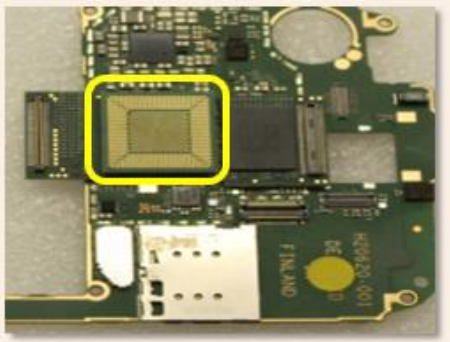




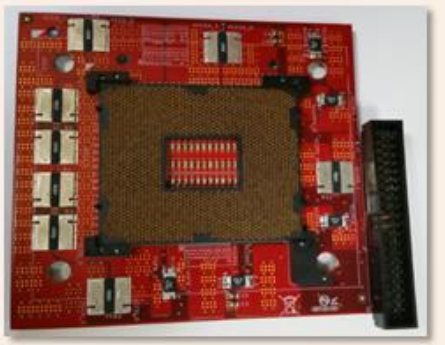
Interposer

Non-product parts, layout, connections moved from baseboard to interposer

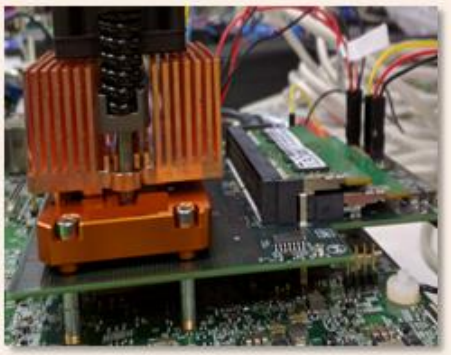
Interposer Possibilities



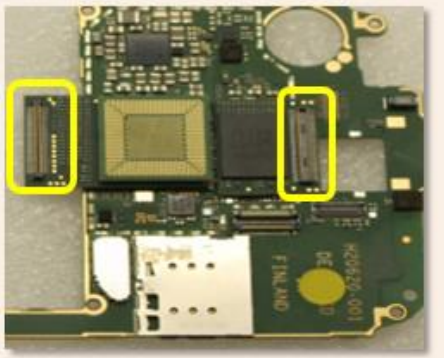
Socketing Solutions



Power Profiling

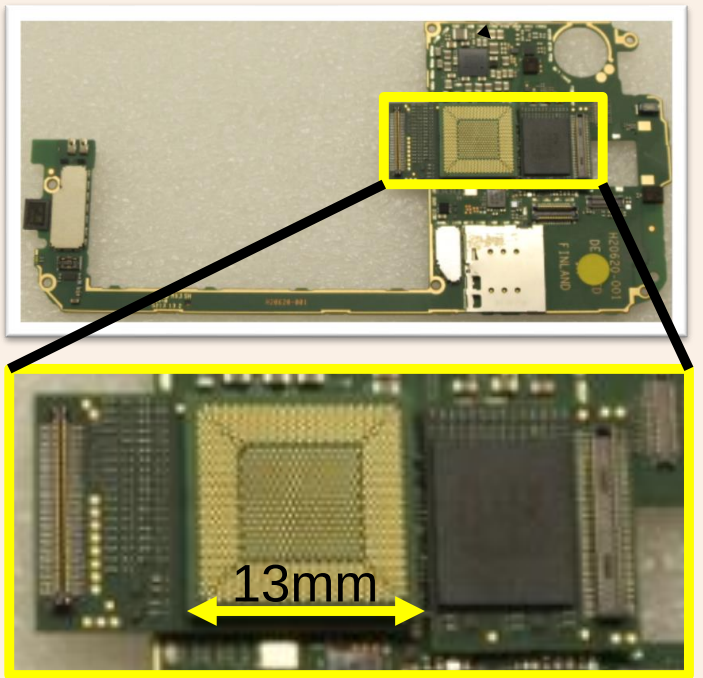


Memory Configurations

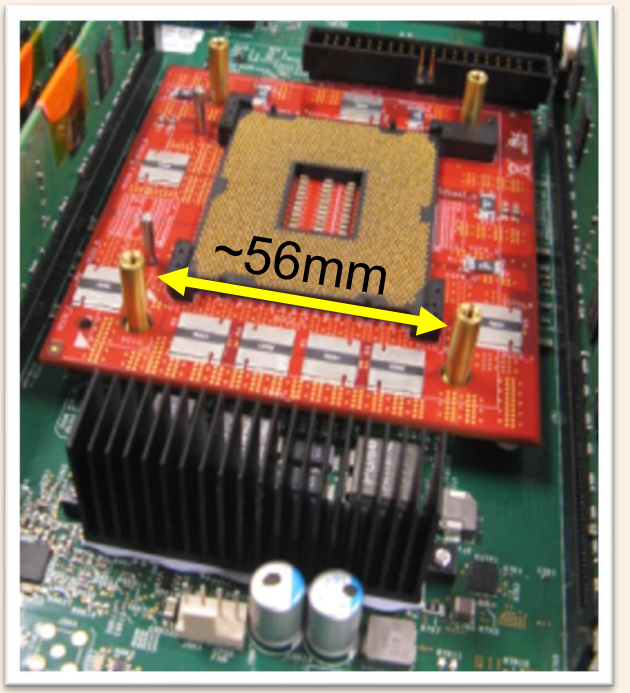


Debug Interfaces

Interposer Extremes

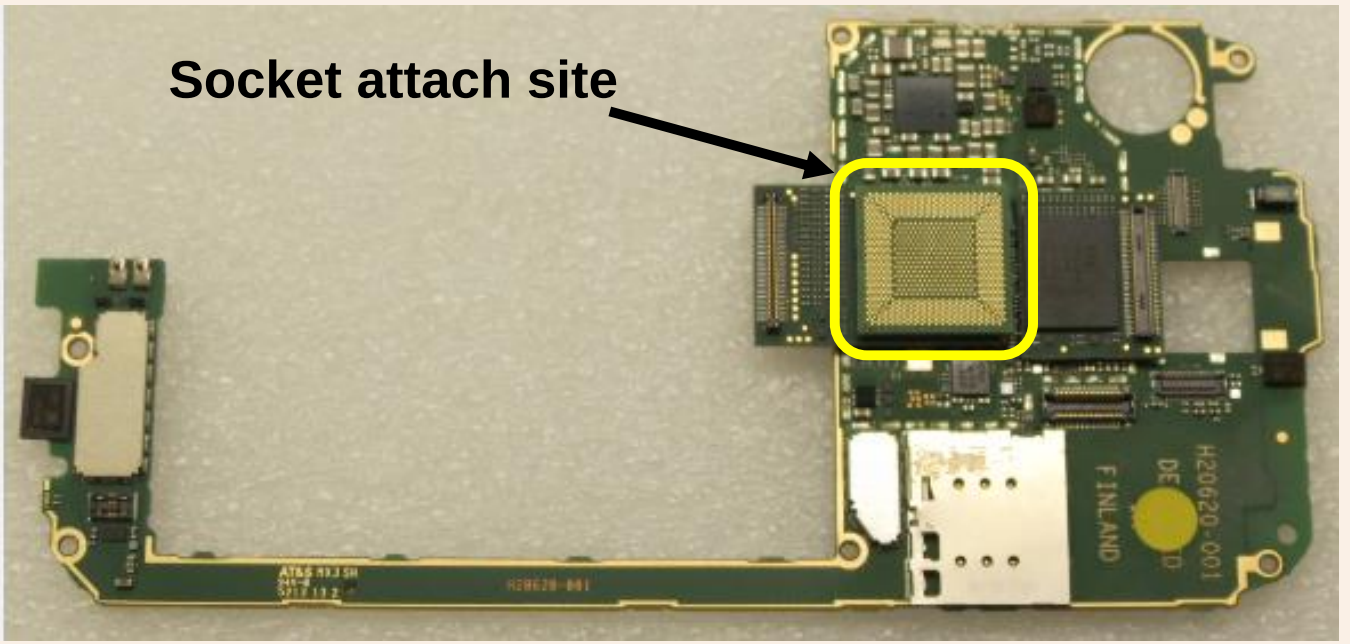


0.4mm pitch devices class debug interposer solution



1.0mm pitch server class power profiling solution

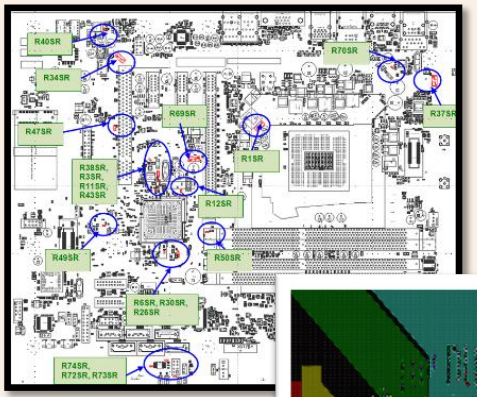
Socket Attach Opportunity



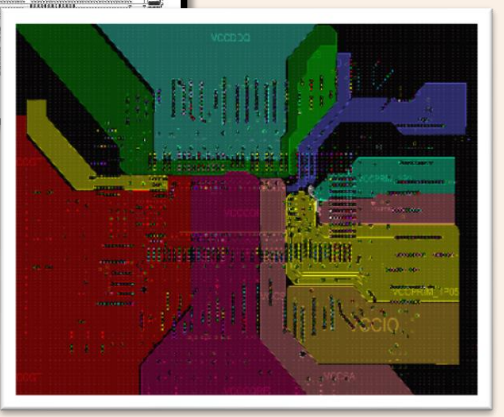
Interposers became ideal candidates for attaching sockets without the need for additional mounting holes or keep out volume

Augmentation enables a Return to Product Focus

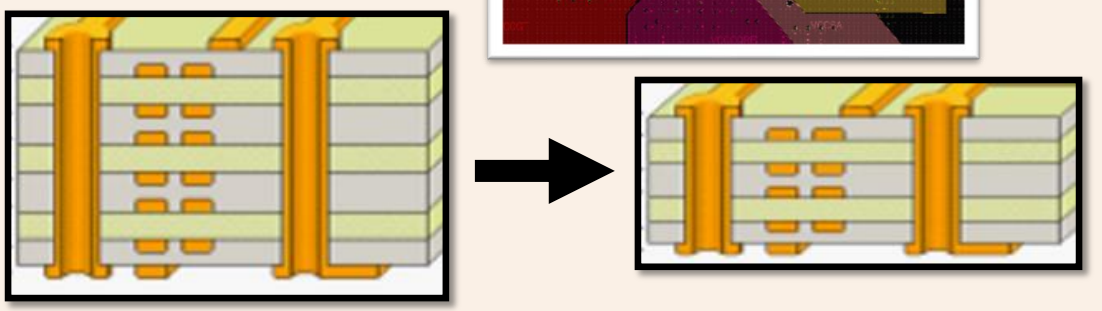
Reduce non-product components
Maintain product component placement



Utilize product power plane shapes



Eliminate need for added PCB layers



Interposer Implementation Challenges and Limitations

- Signal and power integrity impact
- Attachment of interposer to system
- Mechanical conflicts and keep out volumes
- Capability is limited to what can be exposed at component's system interface

Conclusion

Product complexity rising

No change in product cadence

Validation and debug capability drive deviation from product focus

Interposers move complexity from target system while providing needed capability

Augmentation with interposers enables a stronger focus on the end product

Acknowledgements

Interposer and riser development:
Floy Campbell – Intel Corporation
Ashok Kabadi – Intel Corporation (retired)
Matthew G Priolo – Intel Corporation
Adrian R Rodriguez – Intel Corporation