
EIGHTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 2
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Session 2

Jason Mroczkowski

Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 1:30 pm

Performance Prediction

"Coaxial Test Socket - Evolution & Optimization"

Frank Zhou - Smiths Connectors

"100G Testing Fixture Design and Verification"

Jackie Luo - Shanghai Zenfocus Semi-Tech

"Inductance Rise Due To Plating"

Gert Hohenwarter - GateWave Northern, Inc.

"Spring probe current-carrying capacity (continuous vs pulse) analysis and improvement"

Yuanjun Shi - TwinSolution Technology Ltd

BiTS 2017 Burn-in & Test Strategies Workshop

Inductance Rise Due To Plating

Gert Hohenwarter
GateWave Northern, Inc.

BiTS Workshop
March 5 - 8, 2017

Objective

- Identify RF performance changes caused by plating
- Examine impact of these changes on system Signal Integrity (SI) and Power Integrity (PI) performance
- Develop understanding of significance in applications

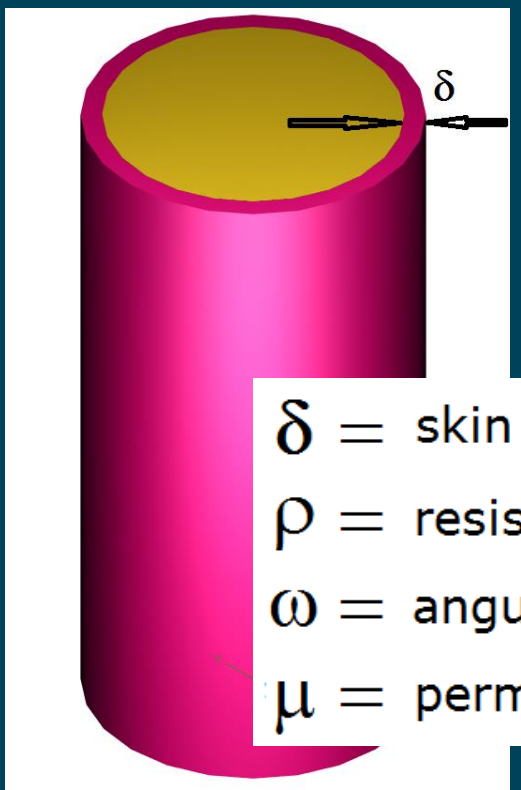
Approach

- Define problem
- Perform measurements and simulations
- Evaluate inductance as a function of frequency
- Illuminate impact on signals by simulation of complete SI / PI path

Tools

- 40 / 100 GHz VNA
- ANSYS HFSS FEA
- Mentor HyperLynx SI
- SPICE simulator

Conductor cross-section



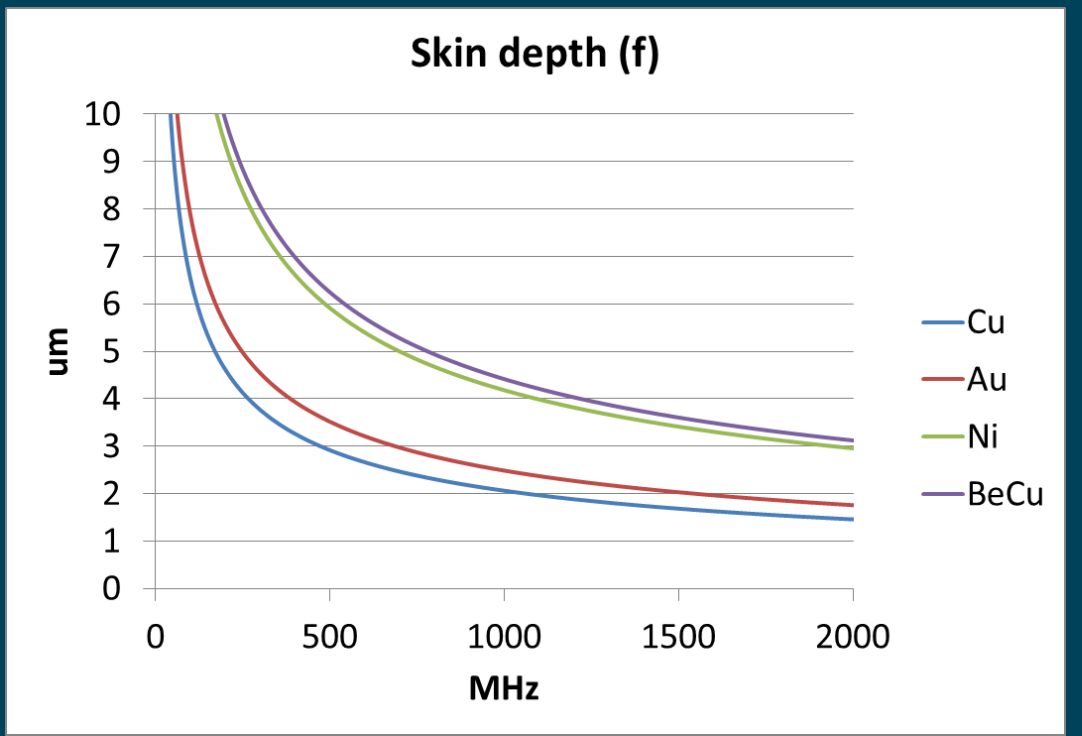
$$\delta = \sqrt{\frac{2*\rho}{\omega*\mu}}$$

δ =	skin depth	=	[m]
ρ =	resistivity	=	[Ω*m]
ω =	angular frequency	=	$2*\Pi*f$ [rad*sec^{-1}]
μ =	permeability	=	$\mu_r*\mu_0$ [V*sec / A]

Field penetration

Inductance Rise Due To Plating

Skin depth in different materials

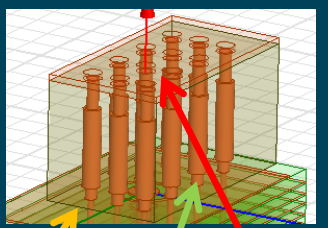


---> RF currents flow mostly on surface of conductor

Field penetration

Inductance Rise Due To Plating

Contact sets with plating



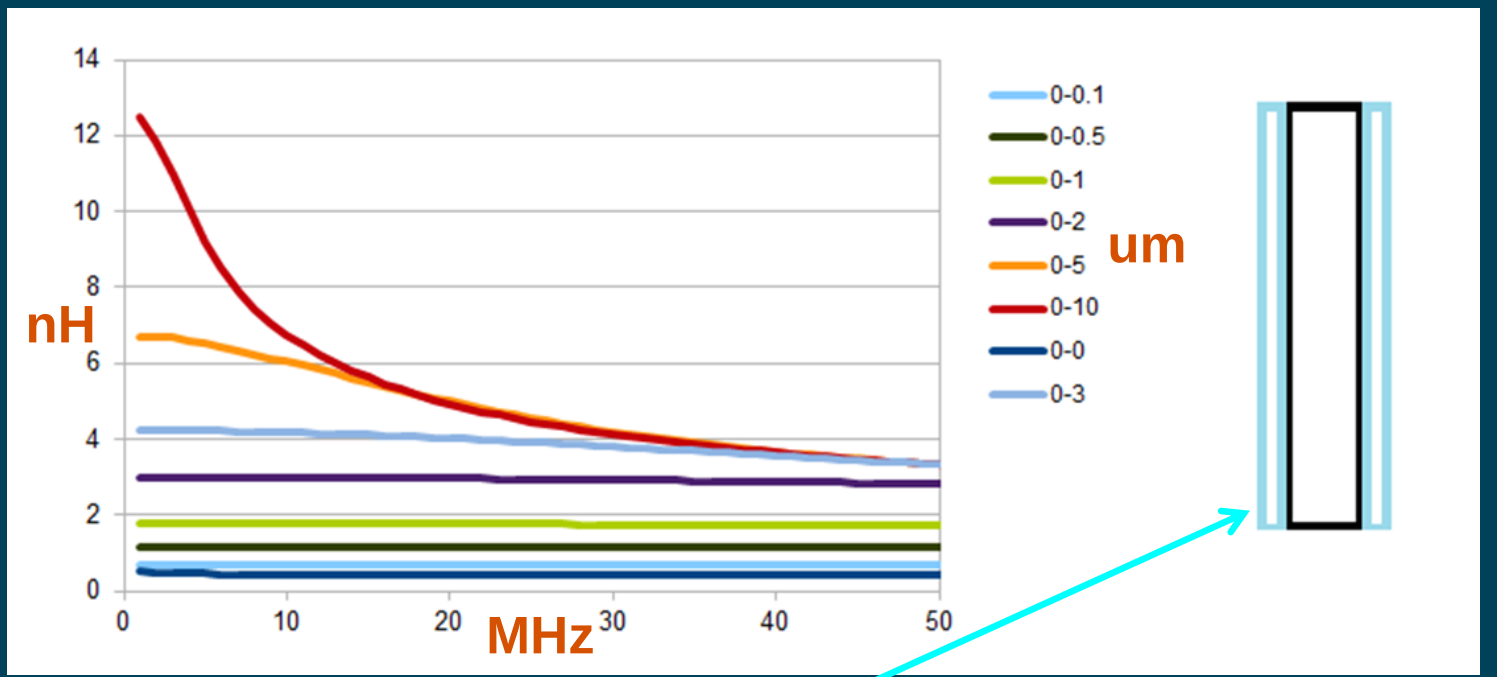
Corner, edge and field locations examined

3x4 array of contacts (measured and simulated)

Ferromagnetic plating may have a significantly higher permeability at low frequencies than the material used for the contact itself.

Socket with generic ‘contacts’

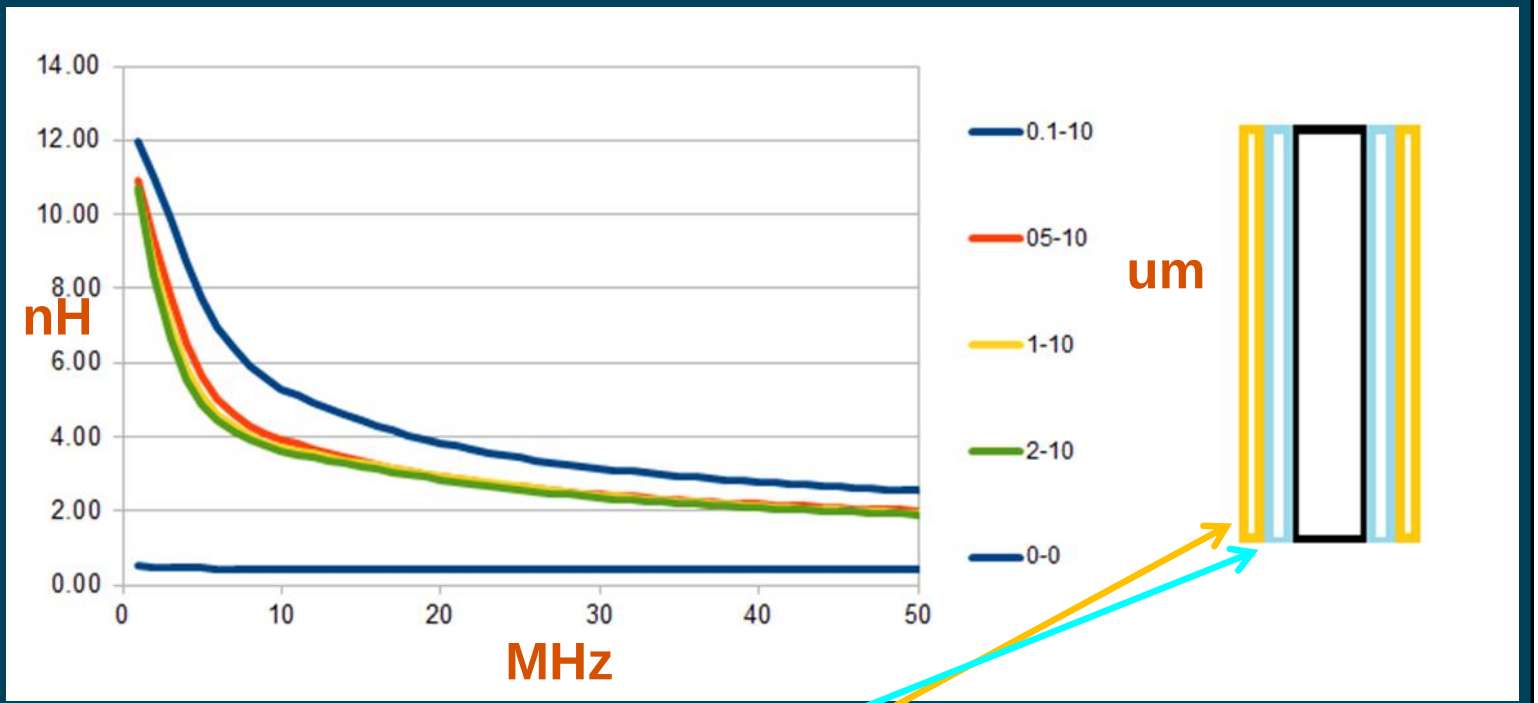
Inductance from simulations



Ni plating (field site)

Inductance Rise Due To Plating

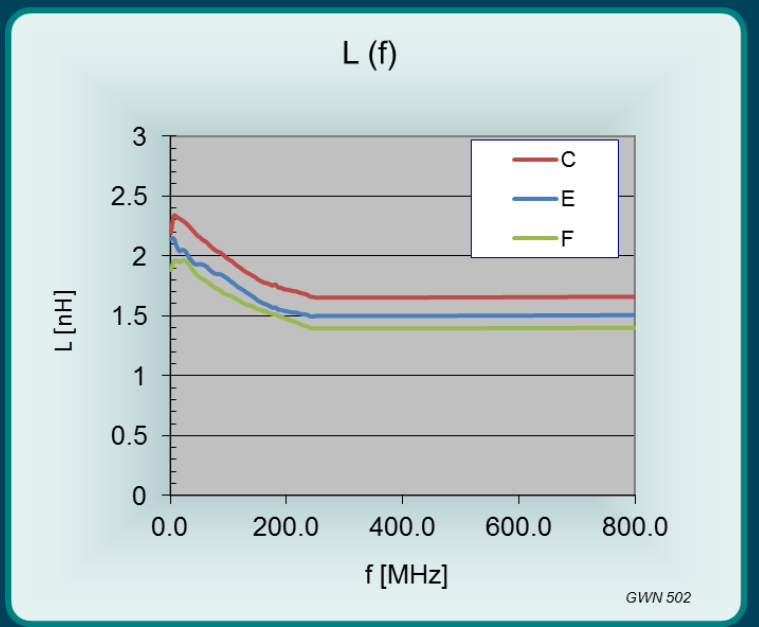
Inductance from simulations



Ni-Au plating (field site)

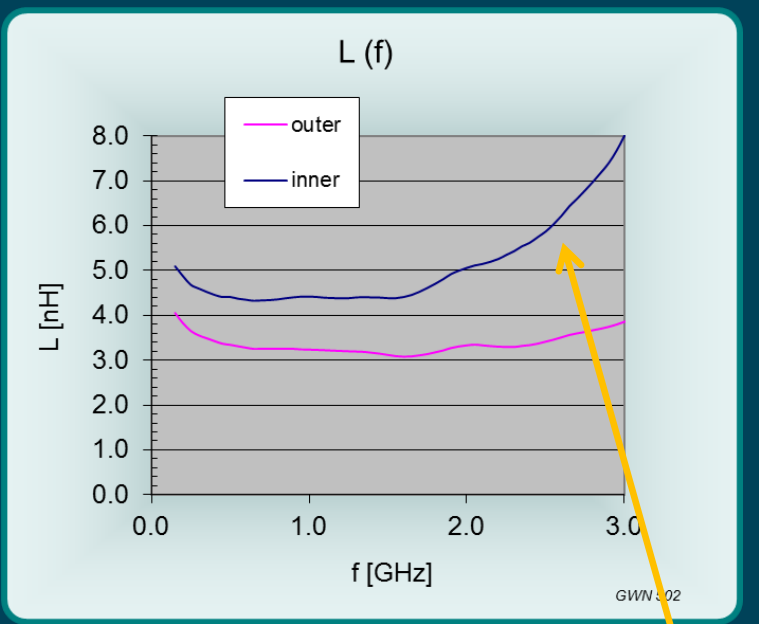
Inductance Rise Due To Plating

Inductance measurements



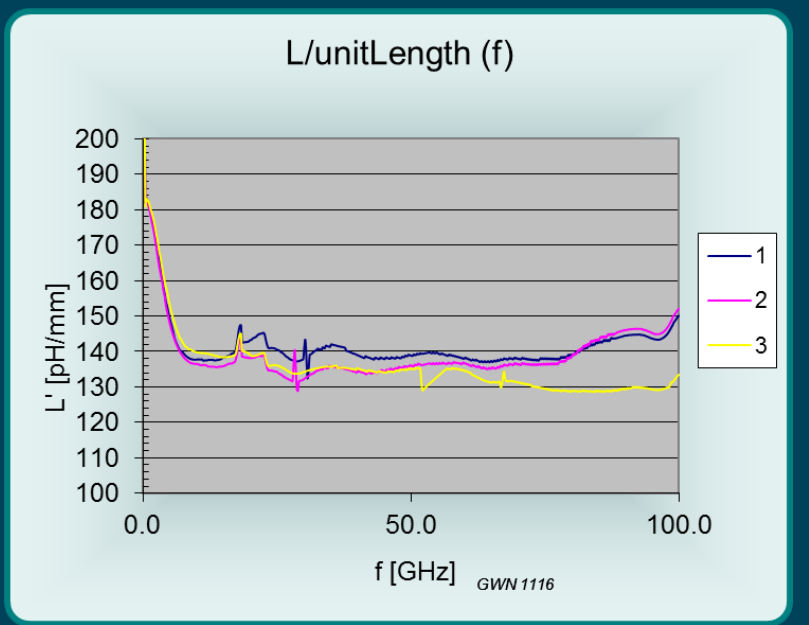
BGA / LGA socket

C=corner, E=edge, F=field



4T (Kelvin) socket ?

Inductance rise at high frequencies



1=corner, 2=edge, 3=field

Inductance per unit length does not rise significantly at high frequencies

Parameters to be considered

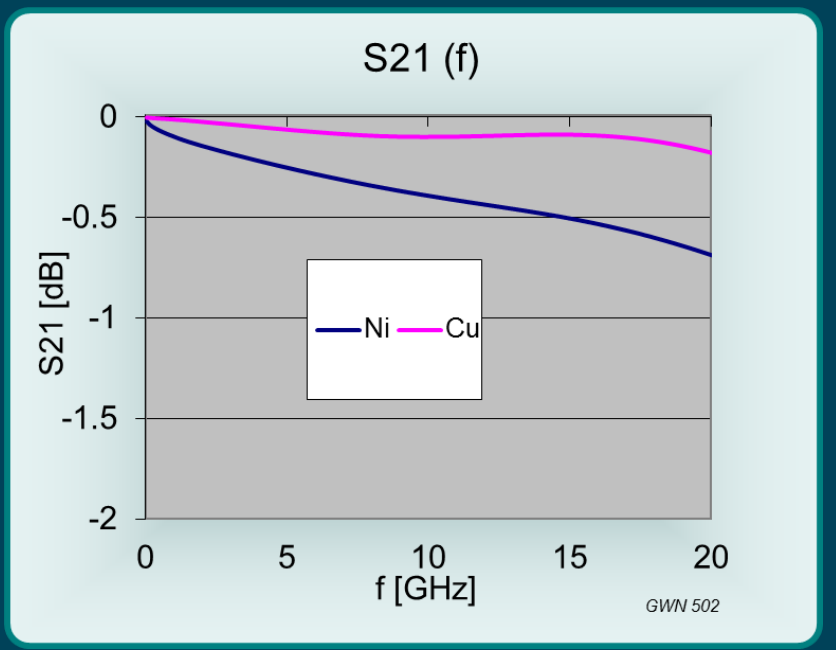
Under control of the contact designer:

- Plating material types
- Material thicknesses
- Housing materials

Not under control of the contact designer:

- Contact arrangement
  - Pitch
  - Signal/ground/power locations
- SI/PI requirements

Insertion loss S21

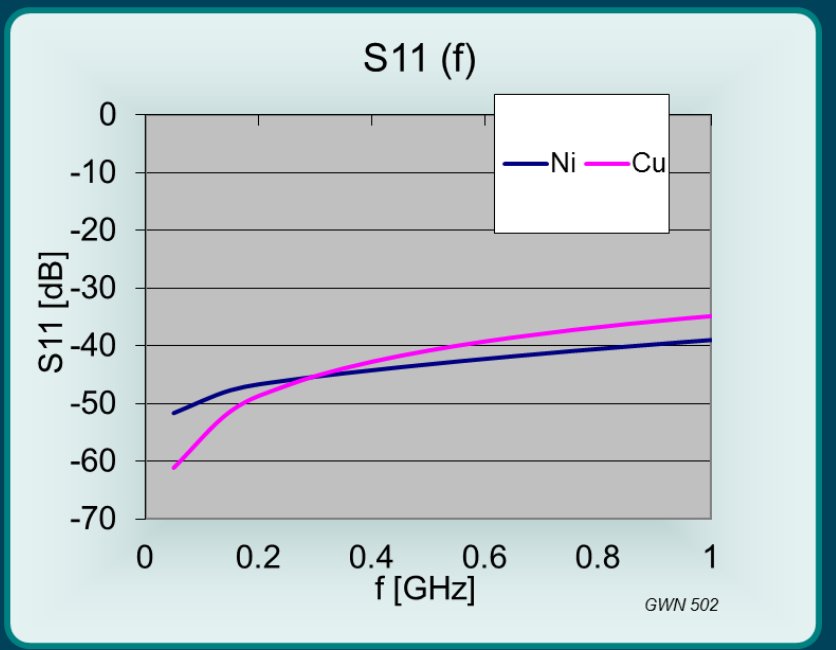


Loss at high frequencies is NOT due to inductance rise but because RF currents flow mostly on surface of conductor

Socket plus via field

Inductance Rise Due To Plating

Return loss S11



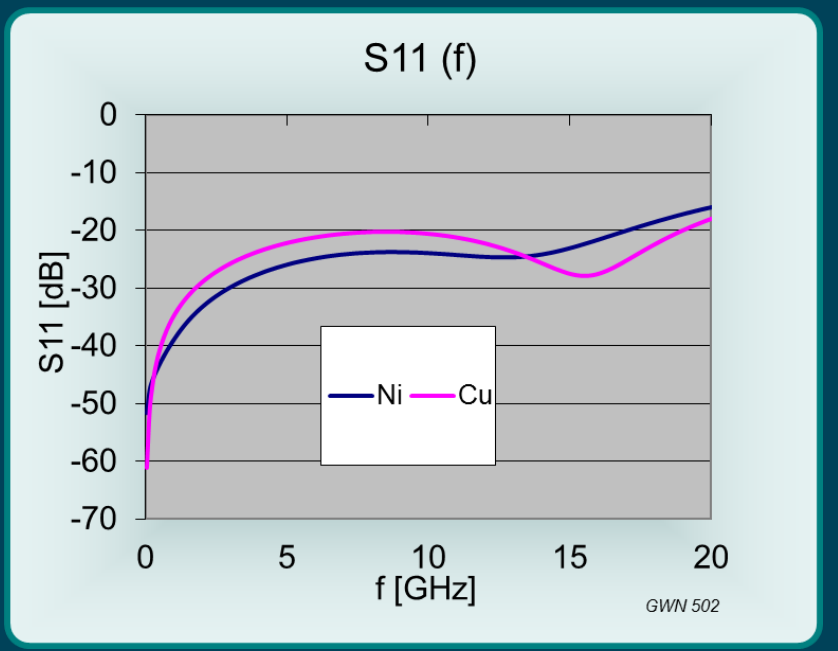
S11 change at low frequencies is due to inductance rise.

Improvement at high frequencies is due to increased loss.

Low frequencies

Inductance Rise Due To Plating

Return loss S11



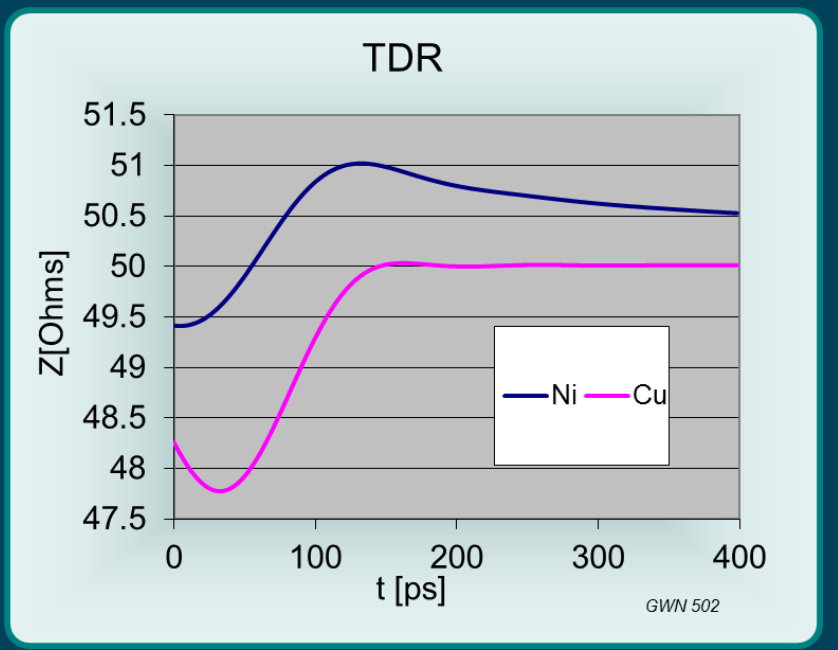
Crossover above 14 GHz is due to better impedance matching for unplated contacts (only for this specific case)

Full range

Inductance Rise Due To Plating

Impedance

Ohms

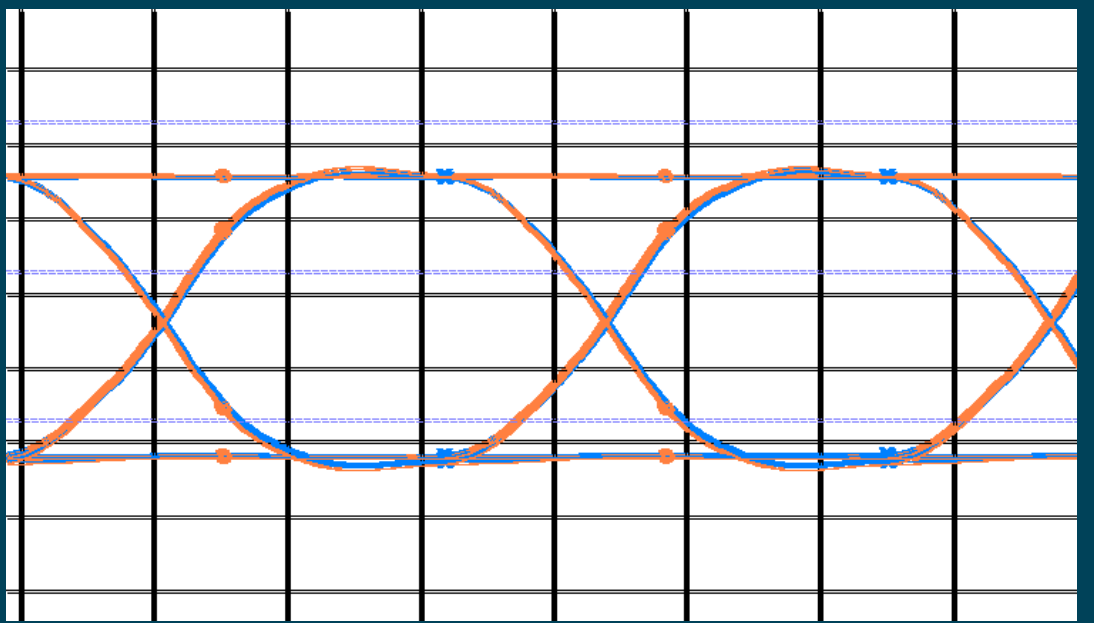


ps

Better impedance matching is due to inductance rise

TDR into 50 ohm load through socket

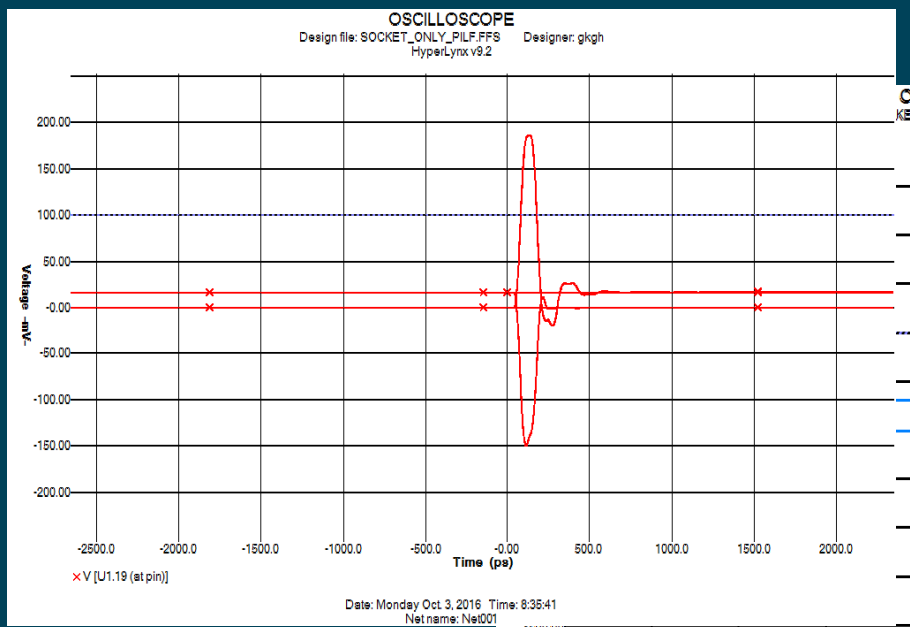
Eye diagram socket only

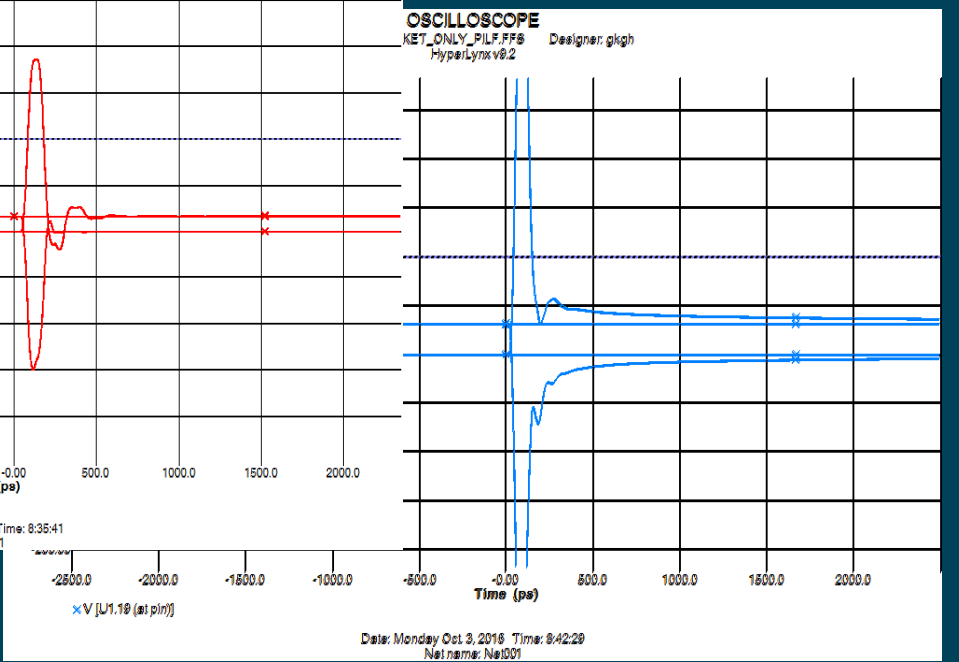


There is no point investigating the difference between plated (blue) and unplated (orange) contacts in this case

G-S-G, 6 GB/s, 50 ohm source and load impedance

Simulated noise at DUT, socket only



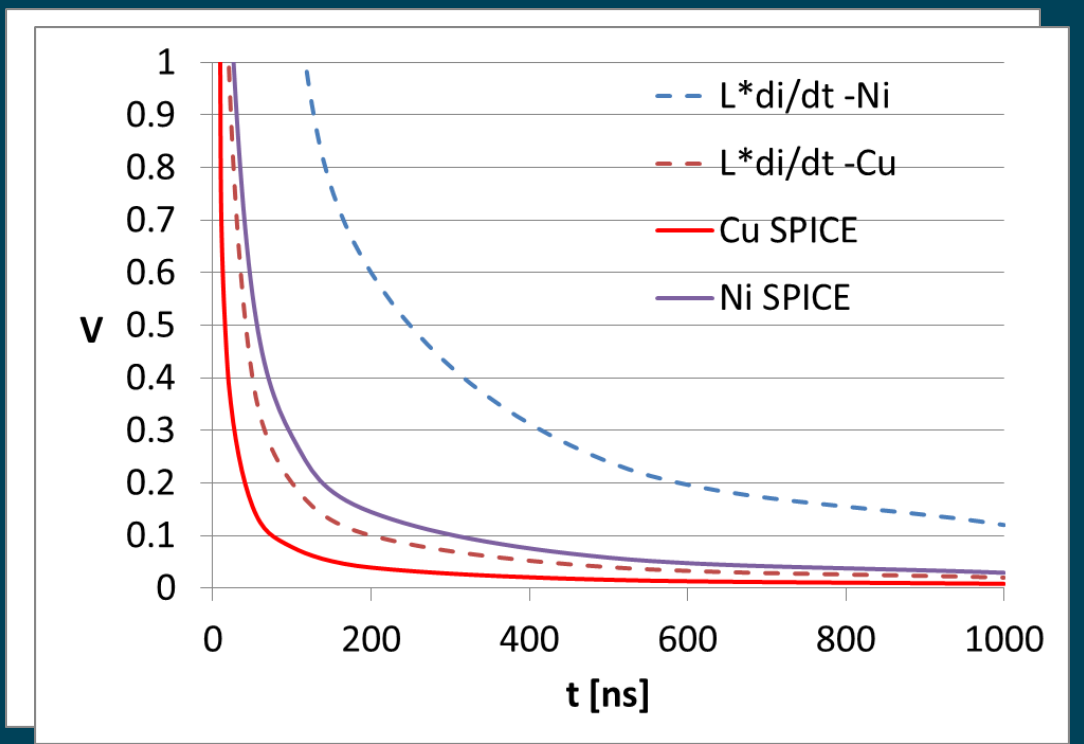


Low frequency pulse current source

Unplated (orange), plated (blue) contacts

Noise at DUT, socket only

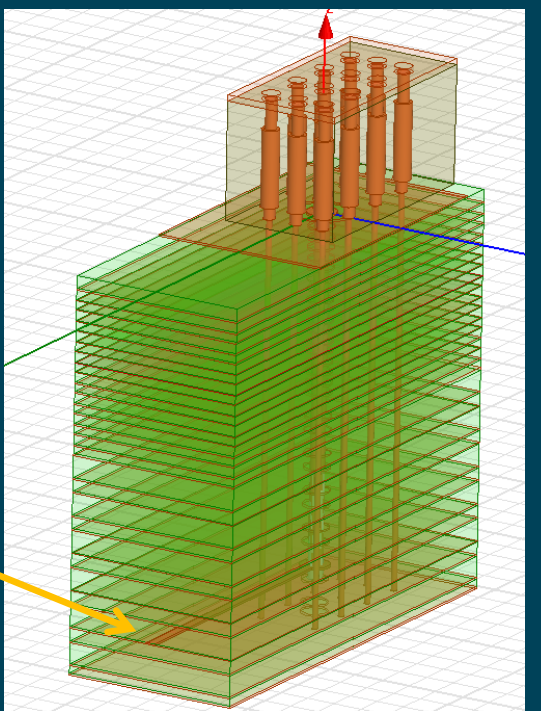
Unplated (orange), plated (blue) contacts



Ramped pulse current source, 10A

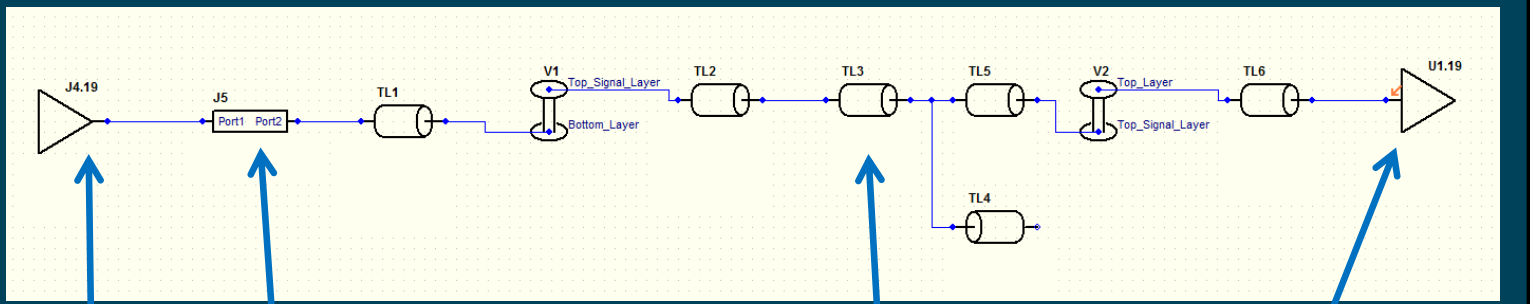
Spreadsheet values (L*di/dt) over estimate size of problem

Socket on a PCB



Socket with generic ‘contacts’

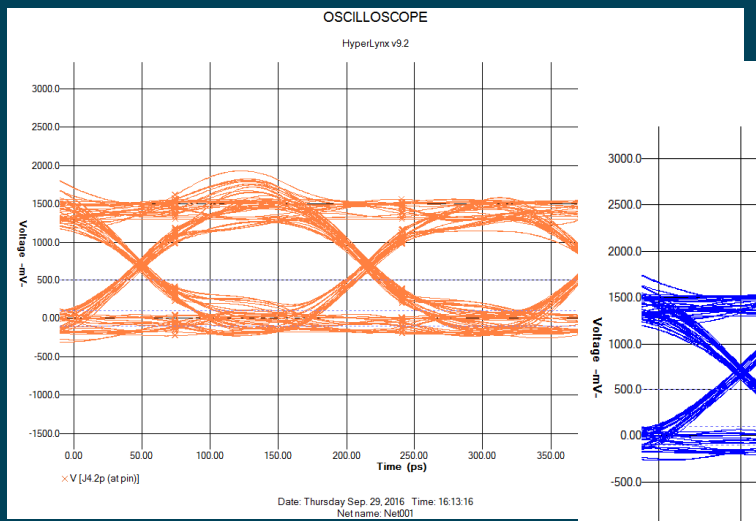
Circuit diagram PCB with socket, SI



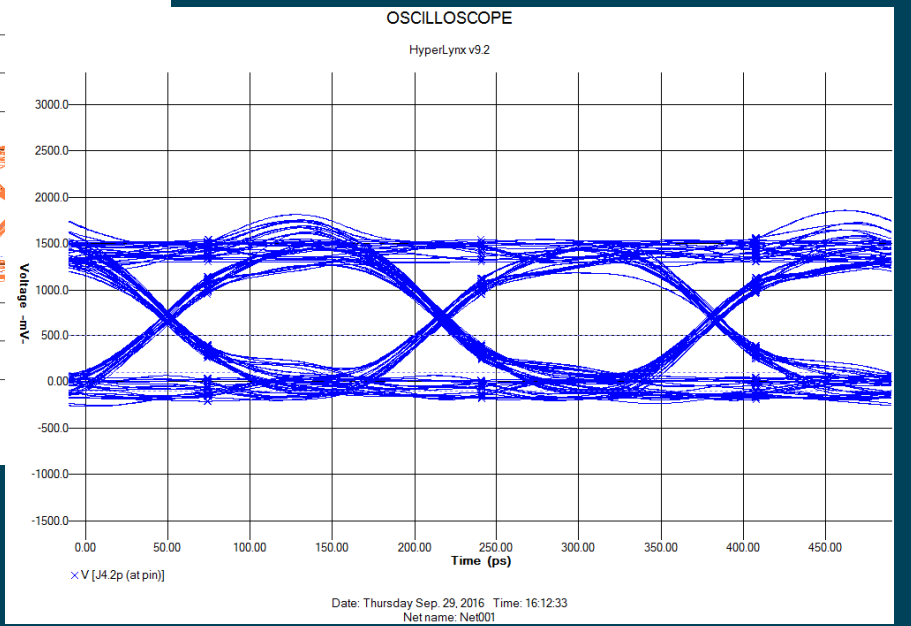
DUT *Socket* *PCB* *Tester*

Source-to-load signal path

Eye diagram of PCB with socket, SI



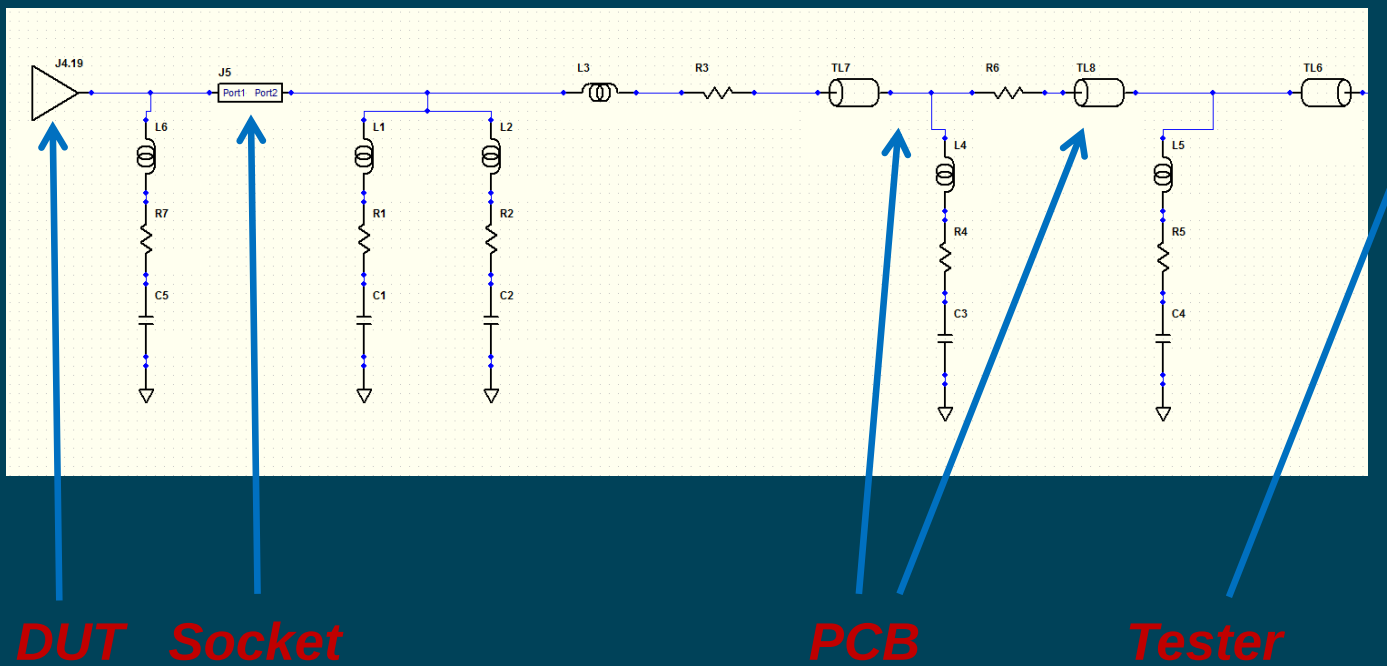
Unplated (Cu)



There is no significant difference, Cu is slightly worse

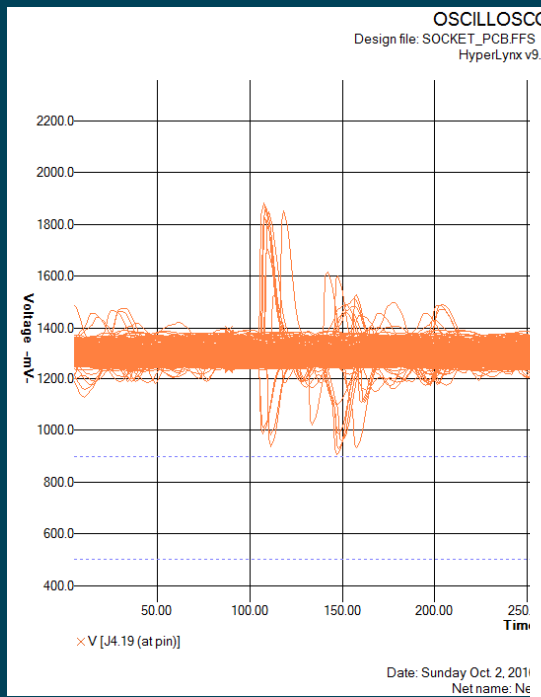
Data line, 6 GB/s, with socket

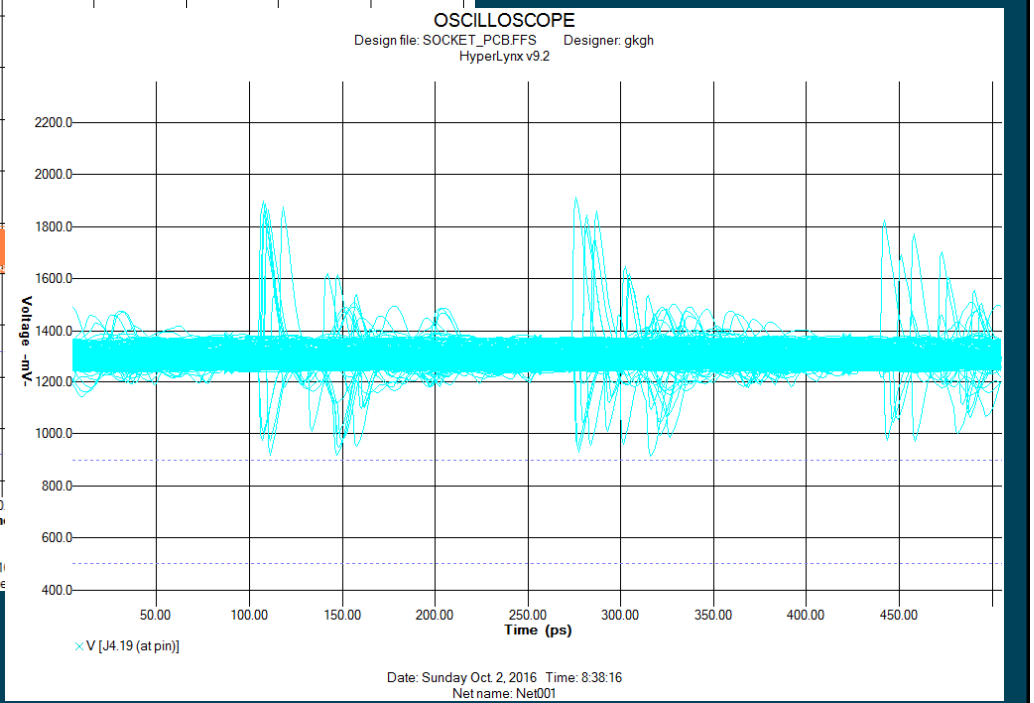
Circuit diagram PCB with socket, PI



Power supply bypassing circuitry

Noise at DUT, PCB with socket

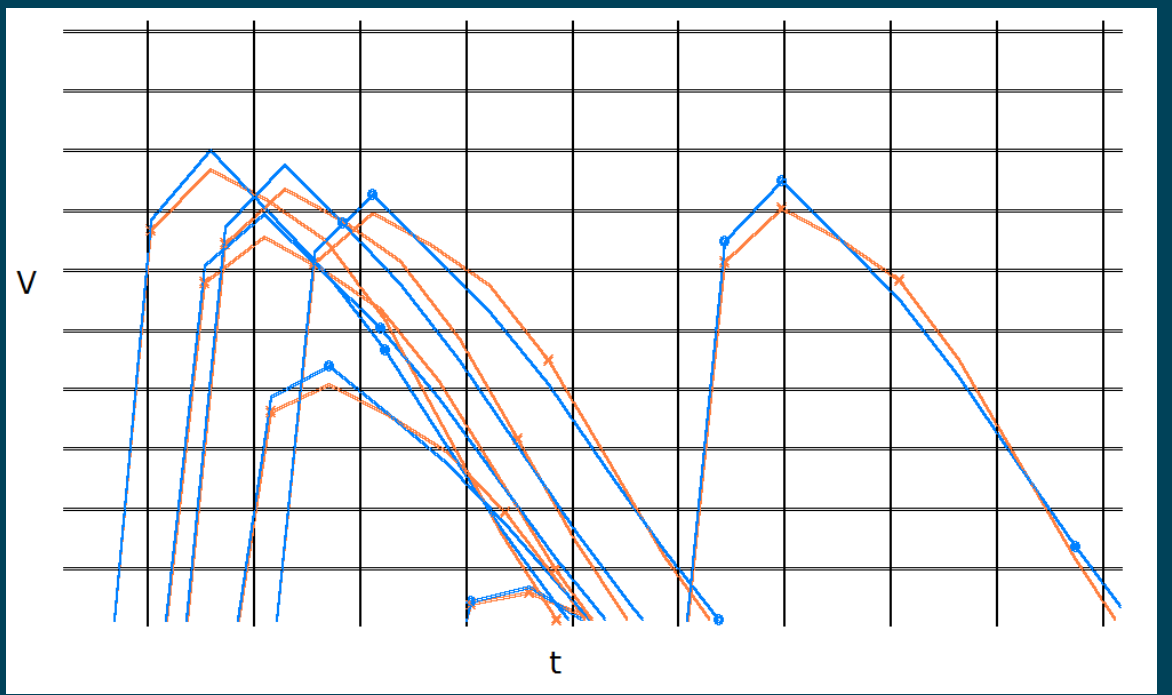




PRBS source

Unplated (orange), plated (blue) contacts

Noise detail at DUT, PCB with socket



Fast PRBS source (GB/s)

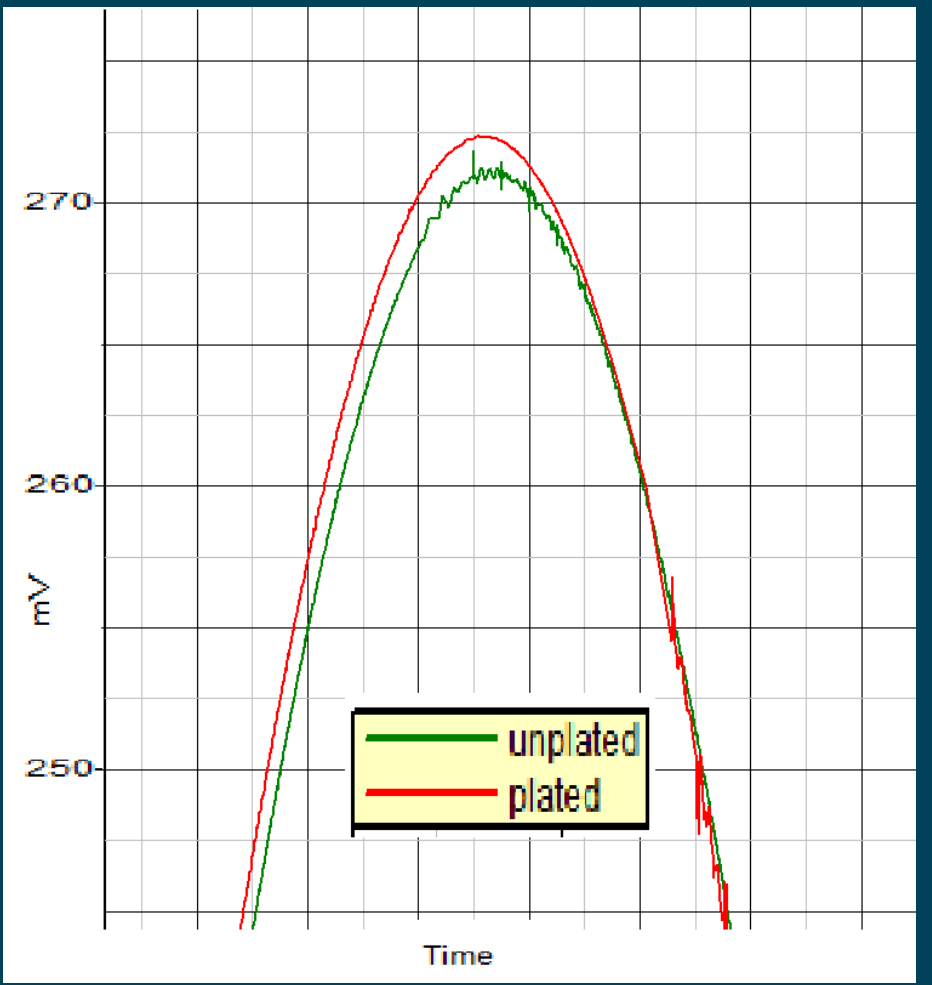
Unplated (or), plated (blu) contacts

Noise voltage at DUT

Unplated vs. plated for sinusoidal

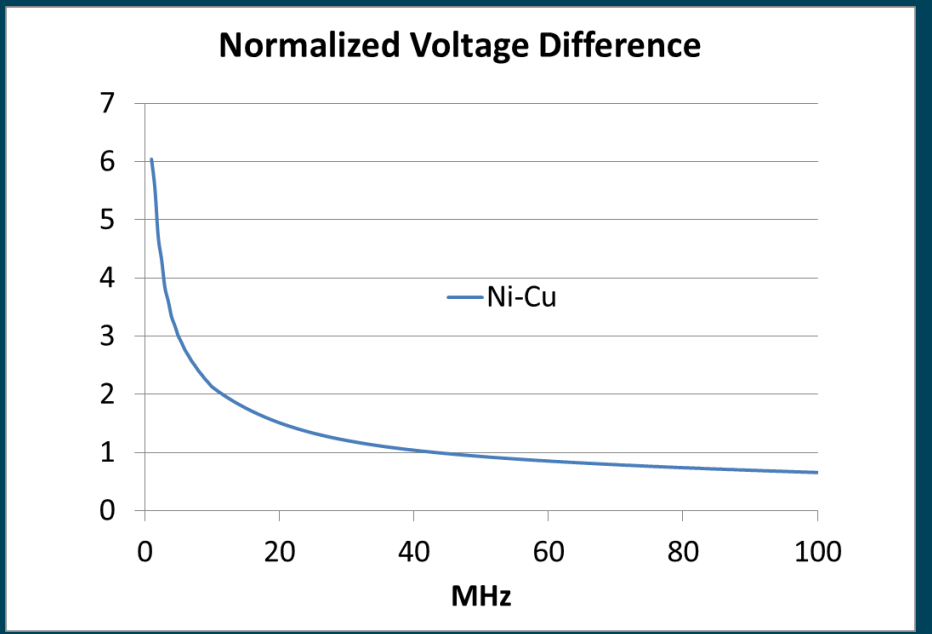
1A / 1 MHz

current at DUT on load board



Inductance Rise Due To Plating

Simulated noise at DUT, socket only



Sinusoidal current source

Vplated / Vunplated

Conclusion

- Low frequency inductance rise is of little consequence for GB/s data streams and may actually help
- Even for low frequency data operation noise levels should not be a problem
- Sinusoidal currents at low frequency may result in increased voltage drop
- High power applications with power switching devices (ns) must be carefully examined
- Assumptions based on ‘basic principles’ may lead to errors in either direction.