BiTS 2017

Performance Prediction - Electrical simulation



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Performance Prediction - Electrical simulation

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Session 2

Jason Mroczkowski Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 1:30 pm

Performance Prediction

"Coaxial Test Socket - Evolution & Optimization"

Frank Zhou - Smiths Connectors

"100G Testing Fixture Design and Verification"

Jackie Luo - Shanghai Zenfocus Semi-Tech

"Inductance Rise Due To Plating"

Gert Hohenwarter - GateWave Northern, Inc.

"Spring probe current-carrying capacity (continuous vs pulse) analysis and improvement"

Yuanjun Shi - TwinSolution Technology Ltd





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100G Testing Fixture Design and Verification

Jackie Luo Shanghai Zenfocus Semi-Tech



BiTS Workshop March 5 - 8, 2017



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Agenda

- 100G High-Speed Interface Introduction
- 100G High-Speed Interface Testing
- 100G Testing Fixture Design
- Testing Verification based on PLTS
 (*Physical Layer Test System*)
- Conclusion



100G Testing Fixture Design and Verification

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100G High-Speed Interface Introduction

- Core/Data
- Switches
- Routers
- Servers
- Storage
- Standard I/O Interface
 - SFP+
 - QSFP+
 - miniSAS
 - ZQFP+

- ZQSFP+
- XCP
- CFP
- CFP2
- CFP4





100G Testing Fixture Design and Verification

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100G High-Speed Interface Introduction

100G Interface Module



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100G High-Speed Interface Testing

Host-to-Module Electrical Specifications (host output)

Parameter	Min.	Max.	Units			
Differential input		C	ar			
return loss	-	See Equation	ab	Í	95 - 0.37f	$0.01 \le f \le 8$
Common to differential				RLd(f) > d	515 015 IJ	0.01 =) < 0
mode conversion return	_	See Equation	dB	RLu() 2	$4.75 - 7.4 \log_{10} \left(\frac{f}{1.4} \right)$	8 ≤ <i>f</i> < 19
loss				Į	010(14/	

Module-to-Host Electrical Specifications (host input)

Parameter	Min.	Max.	Units
Differential input return loss	_	See Equation	dB
Differential to common mode input return loss	_	See Equation	dB

$$RLdc(f) \ge \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \le f < 12.89\\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \le f < 19 \end{cases}$$

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100G Testing Fixture Design and Verification

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100G High-Speed Interface Testing

• Based on IEEE802.3bm (CAUI-4) Specification



MCB : Module Compliance Board

Parameters to be Tested:

Test point: B' Module_OUTPUT_SDD11max Module_OUTPUT_SDC11max



Test point: C' Module_INPUT_SDD11max Module_INPUT_SCD11max

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100G High-Speed Interface Testing

Module-to-Host Electrical Specifications (module output)

Parameter	Min.	Max.	Units
Differential input return loss	Ι	See Equation	dB
Common to differential mode conversion return loss	_	See Equation	dB

Host-to-Module Electrical Specifications (module input)

Parameter	Min.	Max.	Units
Differential input		See Equation	dB
return loss	—	See Equation	
Differential to common		See Equation	dB
mode input return loss	-	See Equation	E E

	9.5 - 0.37f	$0.01 \leq f < 1$
$RLd(f) \ge \langle$	$4.75 - 7.4 \log_{10}\left(\frac{f}{14}\right)$	8 ≤ <i>f</i> < 19

$$RLdc(f) \ge \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \le f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \le f < 19 \end{cases}$$



100G Testing Fixture Design and Verification

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100G High-Speed Interface Testing

Based on IEEE802.3bj Specification





Parameters to be Tested: Insertion loss Return loss Differential to common-mode return loss Differential to common-mode conversion loss Common-mode to commonmode return loss COM (Channel Operating

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Margin)

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100G High-Speed Interface Testing



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Fixture Mating Testing Based on IEEE802.3bj Specification





Parameters to be Tested: Insertion loss Return loss common-mode to Differential return loss Differential to common-mode conversion loss Common-mode to common-mode return loss Integrated crosstalk noise

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100G Testing Fixture Design MCB and HCB Mating Diagram Material, Connector evaluation, Via Modelling and Stackup Design, impedance control, insertion loss, Optimization cross talk, common to Trace differential mode conversion, etc Impedance, Insertion loss, etc. 100G Testing Fixture Design and Verification 14

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100G Testing Fixture Design



IL VS. Trace Width/Air Gap



Impedance VS. Trace Width/Air Gap



Material Verification Board, useAFR (Automatic Fixture Removal) or PLTS (Physical Layer Test System) to do calibration, to get real performance of the material after fabrication

100G Testing Fixture Design and Verification

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100G Testing Fixture Design

copper foil Roughness



Different Processes contribute to different roughness after fabrication







Before Fabrication(VLP) After Traditional Process After low-roughness process



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100G Testing Fixture Design

Low-Roughness Process

Take full advantage of HVLP copper foil



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100G Testing Fixture Design

Glass Fiber Impact to Differential Signals

Differential signals transmit on High Er and Low Er media will have differential delays



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Glass Fiber Impact to Differential Signals

Improvement:

- 1. Design rotated traces;
- 2. Fabricated rotated patterns;





100G Testing Fixture Design and Verification

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Material with issue, phase and delay will be abnormal, and has resonance in IL plot



Material without issue, the phase and delay will be normal, and has no resonance in



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100G Testing Fixture Design

Via Modelling and Optimization



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No stub

18.9

25

30

37.8

44.1 mils

15

Frequency, GHz

20

56.6

10

5

mils

100G Testing Fixture Design

0

-1

-2

-3

-4

-5

-6

-7

-8

-9

-10 └─ 0

S₂₁, dB

STUB length impact to signal Performance



100G Testing Fixture Design and Verification

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100G Testing Fixture Design



Connector Selection

- 1. Insertion Loss
- 2. Return Loss
- 3. Differential pair delay
- 4. Xtalk



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100G Testing Fixture Design



Connector Verification board, use AFR of PLTS to do calibration, to get real performance of the material after fabrication

My fixture inputs are:					
 Single Ended Differential 	-				Þ.
My measurement is: 01 Port 02 Ports OMultiport		Current Fixture Fixture Match Fixture Length DUT ZO: will b	and DUT As : A ≠ B : A = B e set to S	sumptions ystem ZO	
Advanced settings After fixture removal set Ca System ZO" OMeasured Fixture ZO So Ohms Set "System ZO" to Calibn Jumat to correct for Fixt	libration	Reference ZO to erence ZO A ≠ B	:		
I want to correct for Fixt My fixture is band limited	ure Length (use Bandp	A ≠ B A ≠ B ass time domain	mode)		



100G Testing Fixture Design and Verification

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100G Testing Fixture Design

Get parameters from real evaluation board of material and connectors, then simulate to get the performance of the whole trace



This method works for long distance board also (40inch, Meet IEEE802.3bj Spec)



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Fixture Verification based on PLTS

MCB and HCB Verification







Testing Setup :

- 1. Keysight PXI Modular network analyzer
- 2. PLTS physical layer testing SW
- 3. Calibration kits, Coaxial Cables, etc.

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Fixture Verification based on PLTS

Comparison with IEEE802.3bj Spec



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Conclusion

- High-Speed Testing moved from some independent modules to an integrated complex system
- To design a testing fixture which perform as good as expected, we need to evaluate material, stackup, trace, via, interconnection and connectors to get real performance of each segment, then simulate the whole trace to get whole trace performance.
- Fixture verification based on PLTS gives the fixture performance comparing with Specification
- The same methodology can be leveraged to cover higher and higher testing requirement in ATE environment.

