
EIGHTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 2
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Session 2

Jason Mroczkowski

Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 1:30 pm

Performance Prediction

"Coaxial Test Socket - Evolution & Optimization"

Frank Zhou - Smiths Connectors

"100G Testing Fixture Design and Verification"

Jackie Luo - Shanghai Zenfocus Semi-Tech

"Inductance Rise Due To Plating"

Gert Hohenwarter - GateWave Northern, Inc.

"Spring probe current-carrying capacity (continuous vs pulse) analysis and improvement"

Yuanjun Shi - TwinSolution Technology Ltd

BiTS 2017 Burn-in & Test Strategies Workshop

100G Testing Fixture Design and Verification

Jackie Luo
Shanghai Zenfocus Semi-Tech

BiTS Burn-in & Test Strategies Workshop

BiTS Workshop
March 5 - 8, 2017

ZENFOCUS 上海泽丰半导体科技有限公司

Agenda

- 100G High-Speed Interface Introduction
- 100G High-Speed Interface Testing
- 100G Testing Fixture Design
- Testing Verification based on PLTS (*Physical Layer Test System*)
- Conclusion

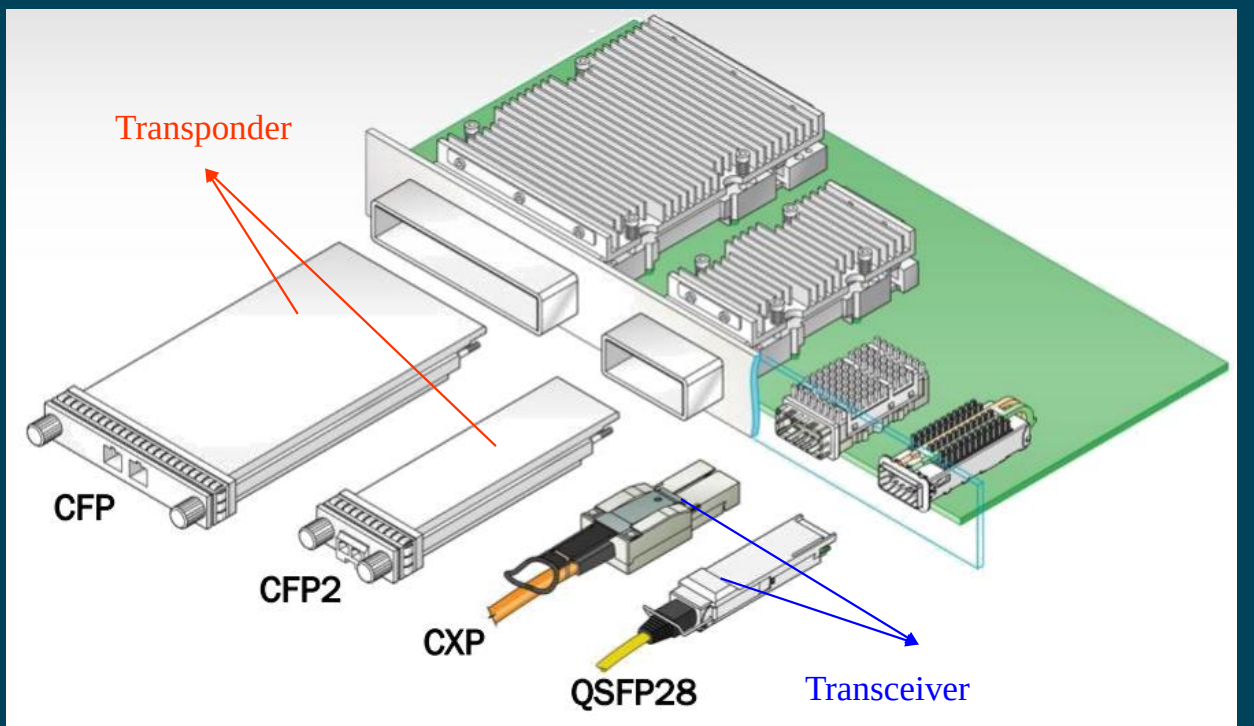
100G High-Speed Interface Introduction

- Core/Data
- Switches
- Routers
- Servers
- Storage

- Standard I/O Interface
  - SFP+
  - QSFP+
  - miniSAS
  - ZQFP+
  - ZQSFP+
  - XCP
  - CFP
  - CFP2
  - CFP4

100G High-Speed Interface Introduction

100G Interface Module



100G High-Speed Interface Testing

Host-to-Module Electrical Specifications (host output)

Parameter	Min.	Max.	Units
Differential input return loss	_	See Equation	dB
Common to differential mode conversion return loss	_	See Equation	dB

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases}$$

Module-to-Host Electrical Specifications (host input)

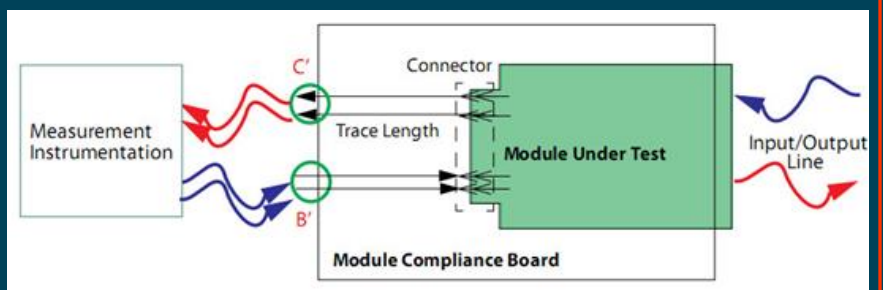
Parameter	Min.	Max.	Units
Differential input return loss	_	See Equation	dB
Differential to common mode input return loss	_	See Equation	dB

$$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases}$$

100G High-Speed Interface Testing

- Based on IEEE802.3bm（CAUI-4）Specification

MCB : Module Compliance Board



Parameters to be Tested：

Test point： B'
Module_OUTPUT_SDD11max
Module_OUTPUT_SDC11max

Test point： C'
Module_INPUT_SDD11max
Module_INPUT_SCD11max

100G High-Speed Interface Testing

Module-to-Host Electrical Specifications (module output)

Parameter	Min.	Max.	Units
Differential input return loss	_	See Equation	dB
Common to differential mode conversion return loss	_	See Equation	dB

$$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases}$$

Host-to-Module Electrical Specifications (module input)

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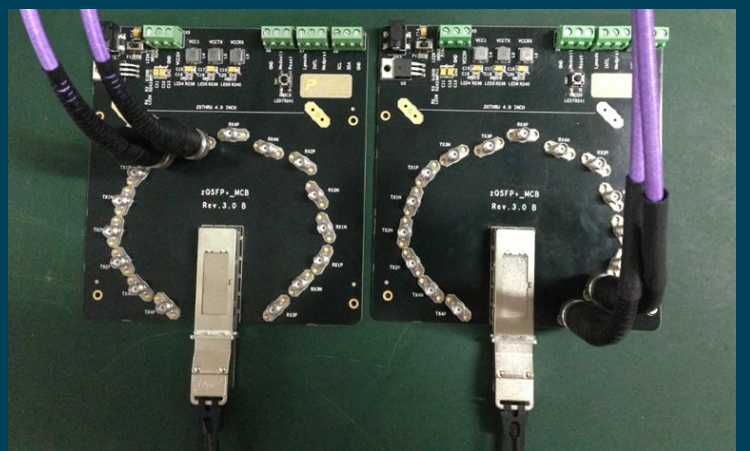
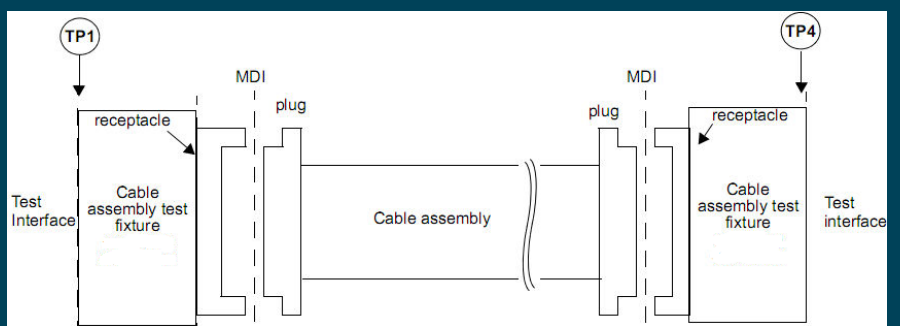
100G High-Speed Interface Testing

- Based on IEEE802.3bj Specification





Parameters to be Tested:

Insertion loss

Return loss

Differential to common-mode return loss

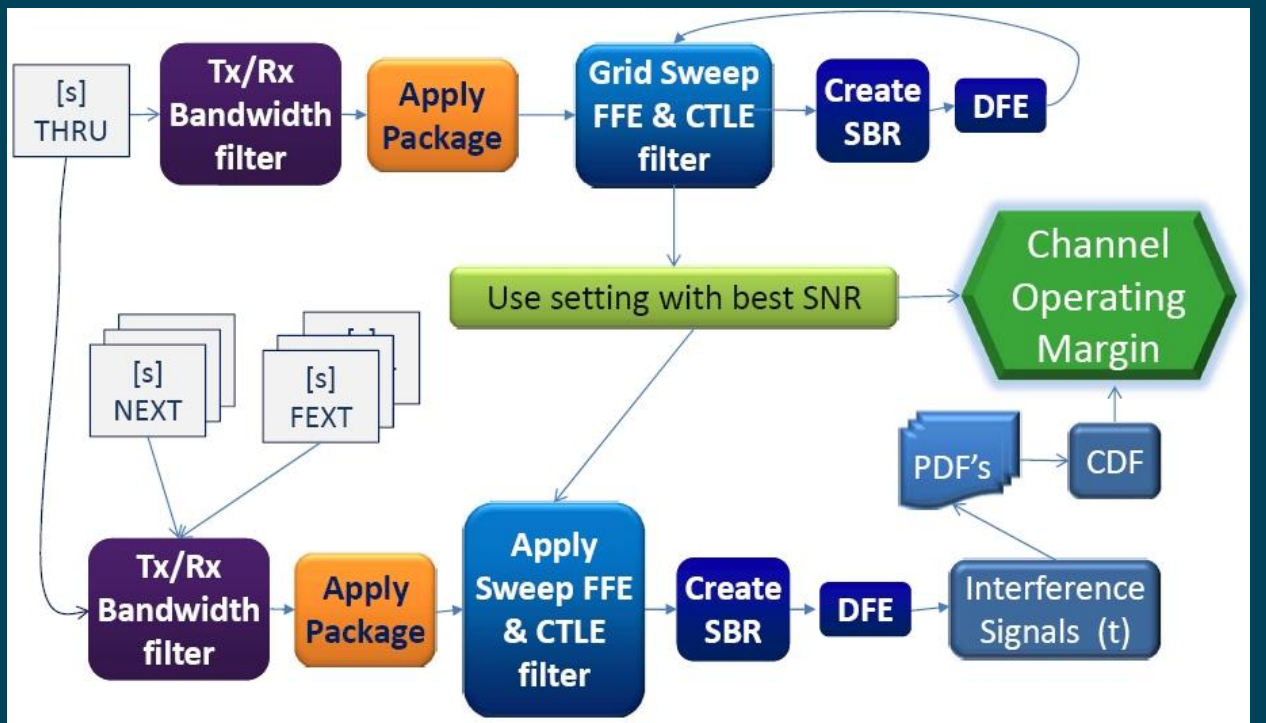
Differential to common-mode conversion loss

Common-mode to common-mode return loss

COM（ Channel Operating Margin）

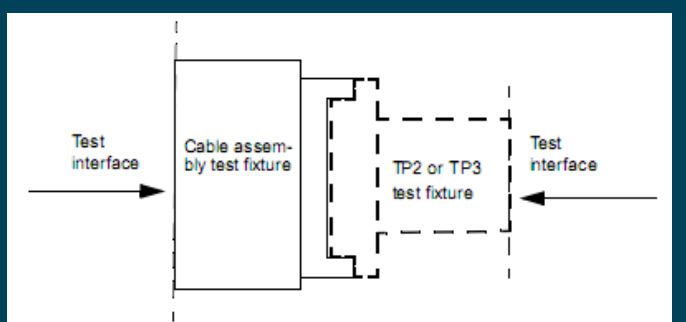
100G Testing Fixture Design and Verification

100G High-Speed Interface Testing



100G High-Speed Interface Testing

Fixture Mating Testing Based on IEEE802.3bj Specification



Parameters to be Tested:

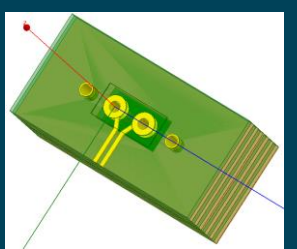
- **Insertion loss**
- **Return loss**
- **common-mode to Differential return loss**
- **Differential to common-mode conversion loss**
- **Common-mode to common-mode return loss**
- **Integrated crosstalk noise**

100G Testing Fixture Design

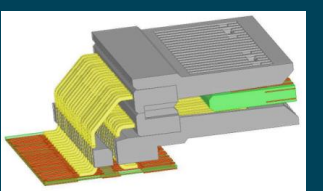
MCB and HCB Mating Diagram

Material, Stackup Design, Trace Impedance, Insertion loss, etc.

Via Modelling and Optimization

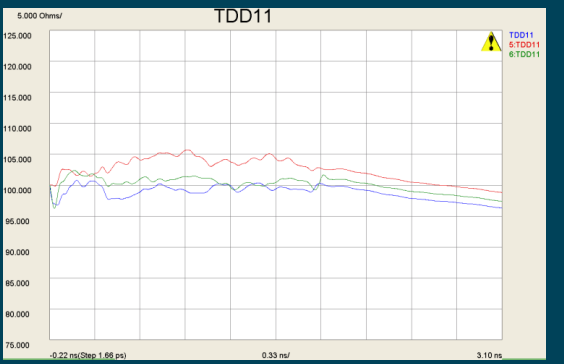


Connector evaluation, impedance control, insertion loss, cross talk, common to differential mode conversion, etc

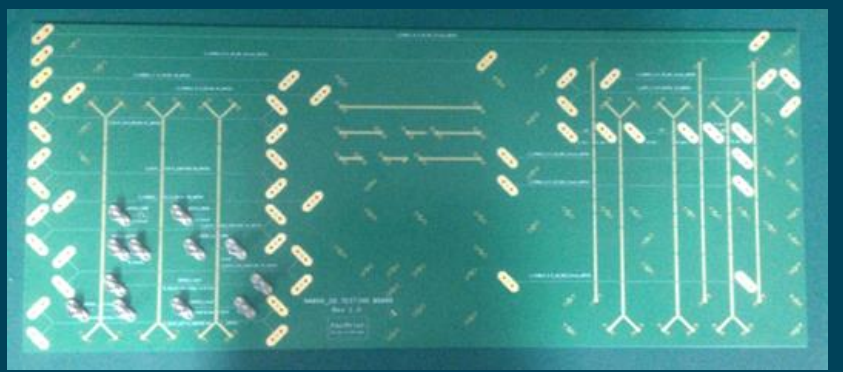


100G Testing Fixture Design

IL VS. Trace Width/Air Gap



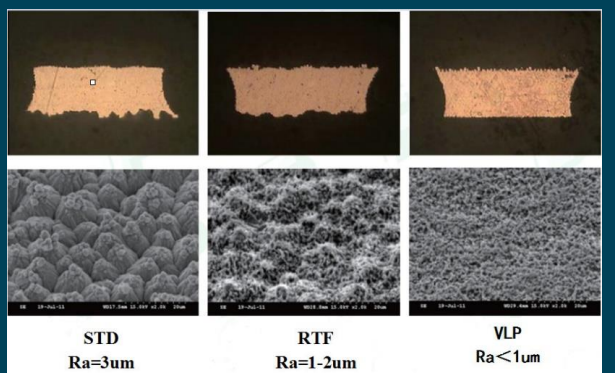
Impedance VS. Trace Width/Air Gap



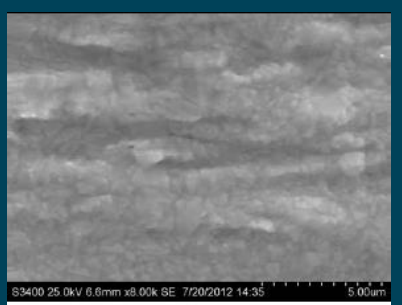
Material Verification Board, useAFR (Automatic Fixture Removal) or PLTS (Physical Layer Test System) to do calibration, to get real performance of the material after fabrication

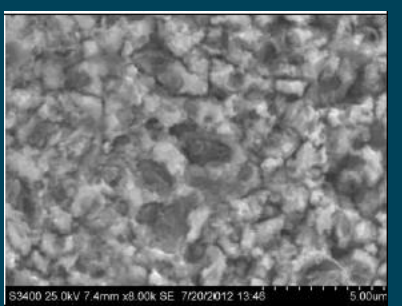
100G Testing Fixture Design

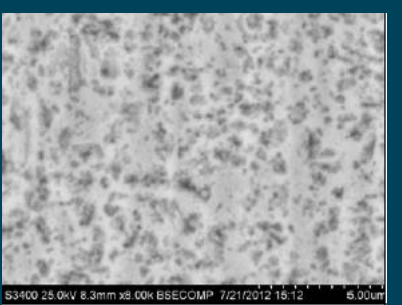
copper foil Roughness



Different Processes contribute to different roughness after fabrication





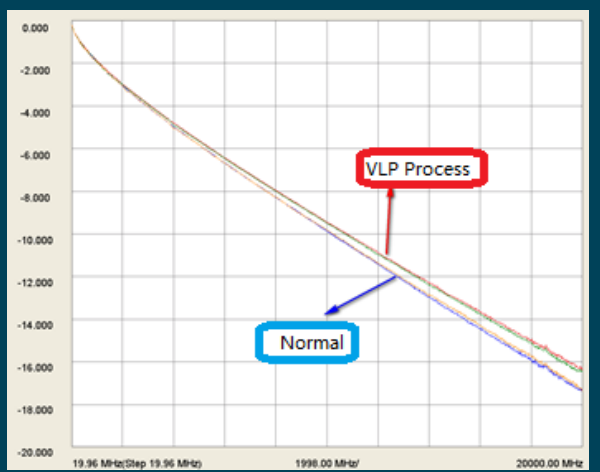


Before Fabrication(VLP) **After Traditional Process** **After low-roughness process**

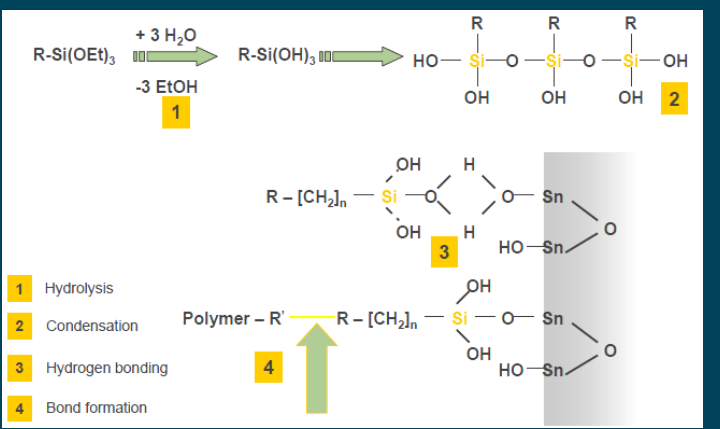
100G Testing Fixture Design

Low-Roughness Process

Take full advantage of HVLP copper foil



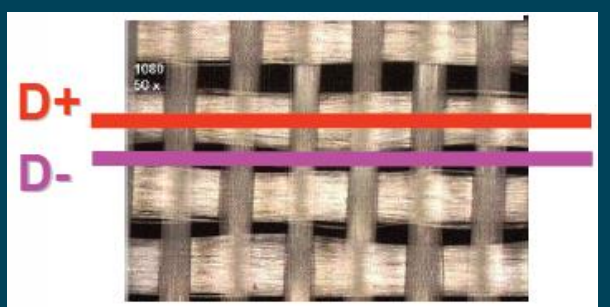
IL Vs. Process



100G Testing Fixture Design

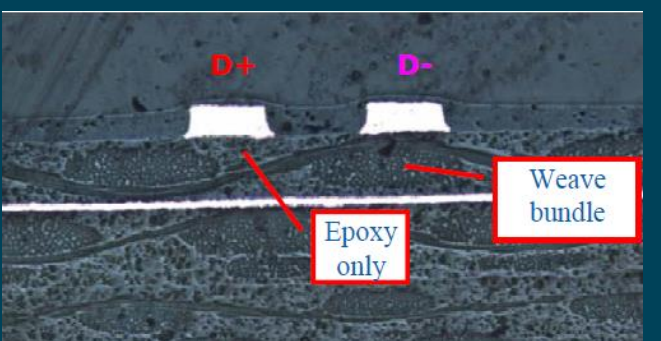
Glass Fiber Impact to Differential Signals

Differential signals transmit on High Er and Low Er media will have differential delays



High Er

Low Er



$$v = \frac{c}{\sqrt{\varepsilon_r}}$$

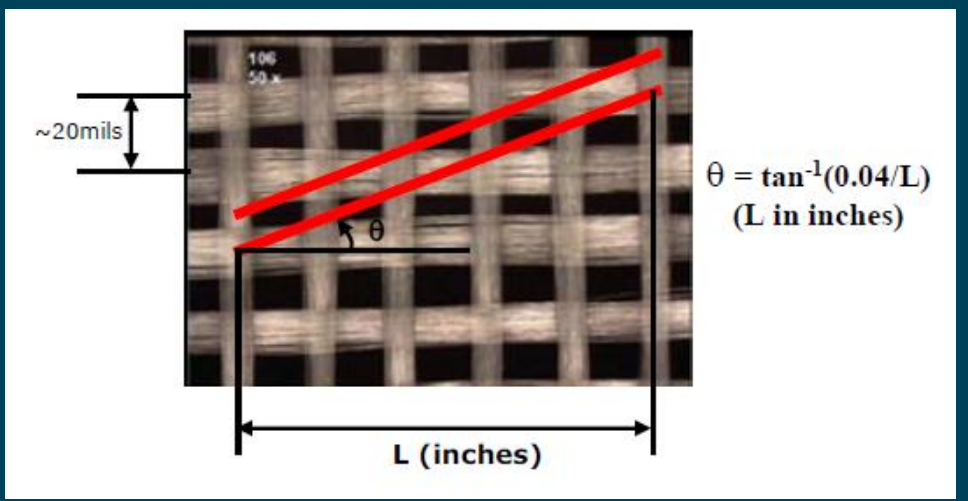
Signals travel faster when Er is lower

100G Testing Fixture Design

Glass Fiber Impact to Differential Signals

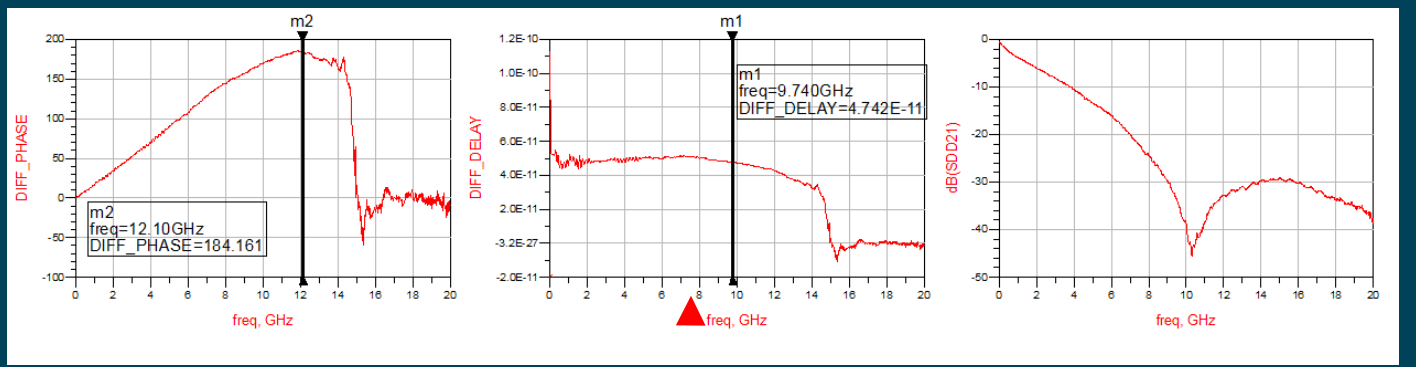
Improvement:

1. Design rotated traces;
2. Fabricated rotated patterns;

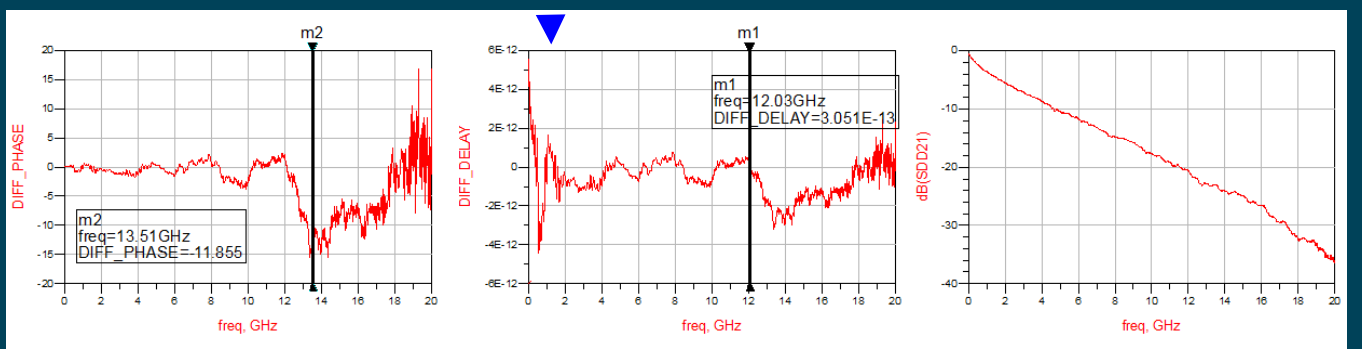


100G Testing Fixture Design

Material with issue, phase and delay will be abnormal, and has resonance in IL plot

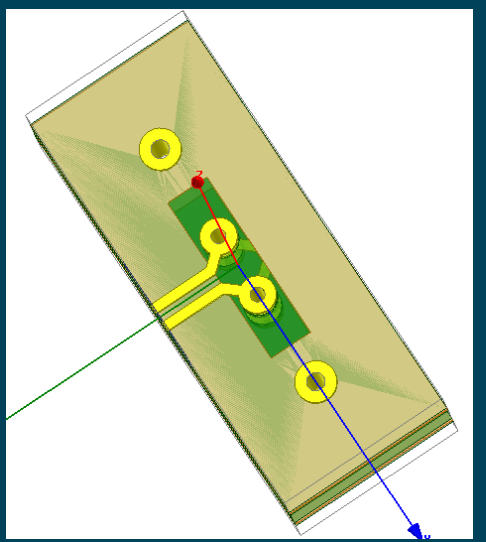


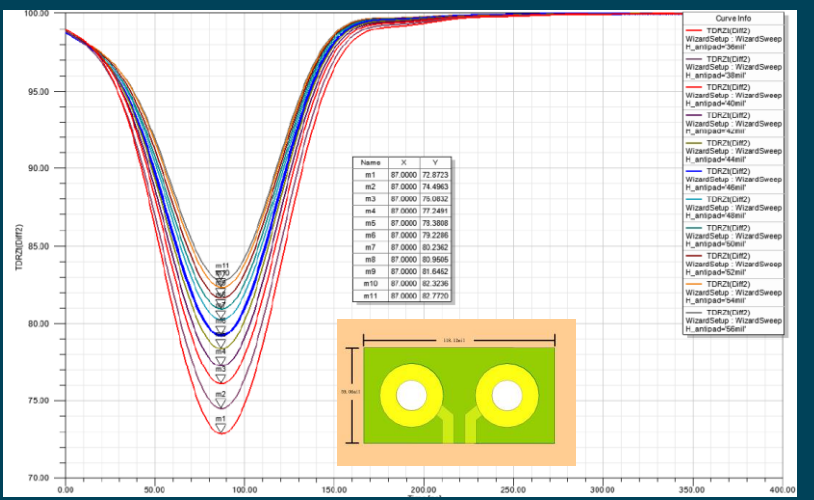
Material without issue, the phase and delay will be normal, and has no resonance in IL plot



100G Testing Fixture Design

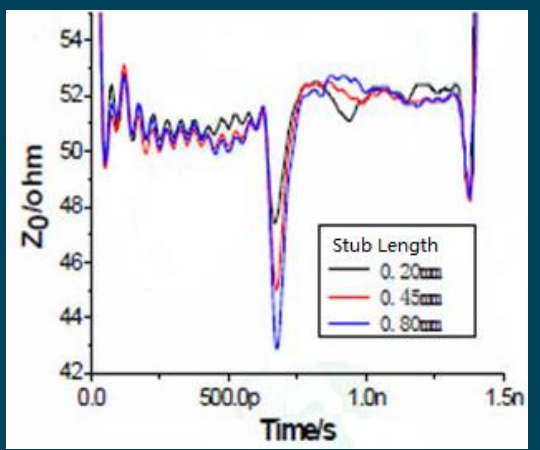
Via Modelling and Optimization

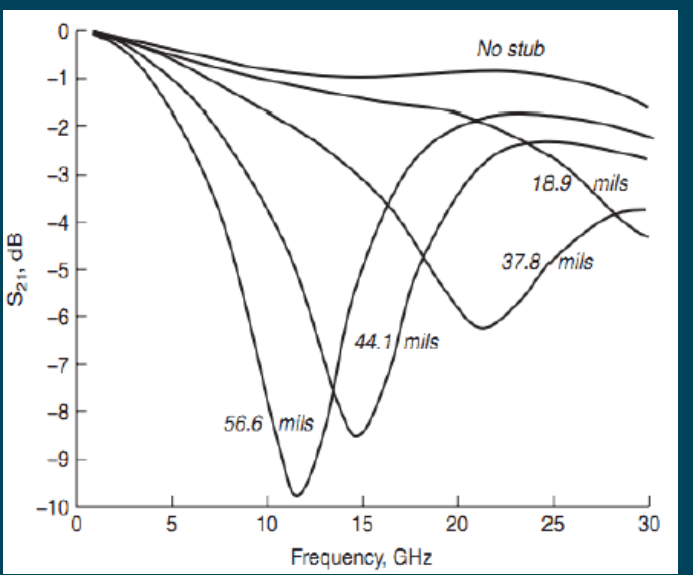




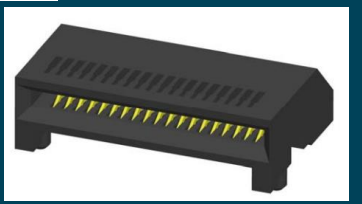
100G Testing Fixture Design

STUB length impact to signal Performance



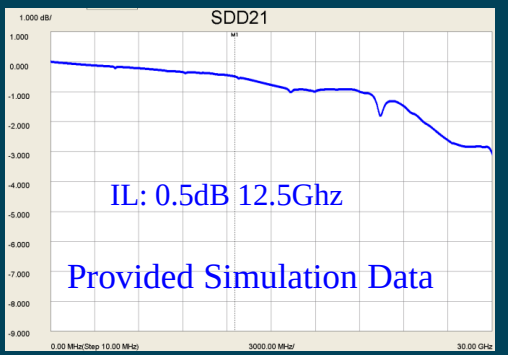


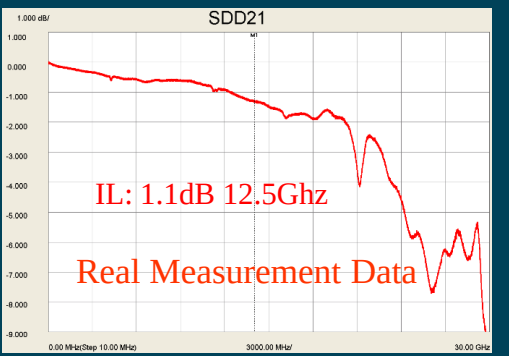
100G Testing Fixture Design



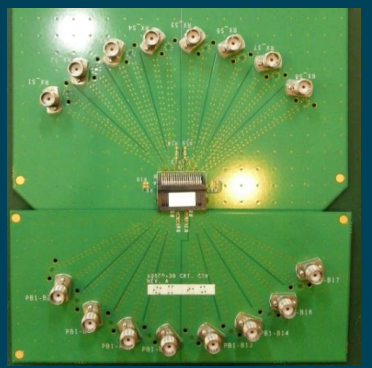
Connector Selection

1. Insertion Loss
2. Return Loss
3. Differential pair delay
4. Xtalk

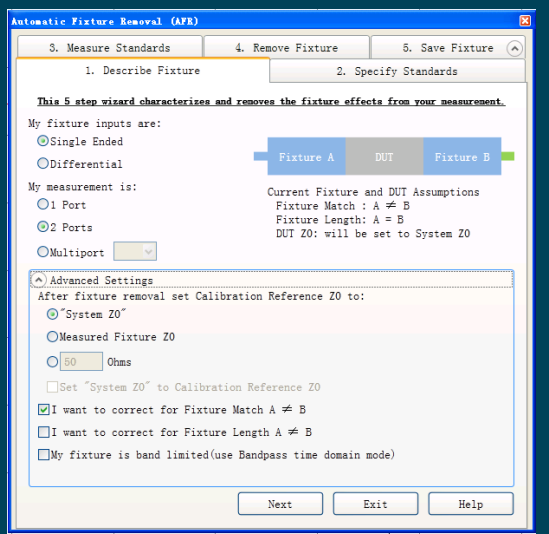




100G Testing Fixture Design

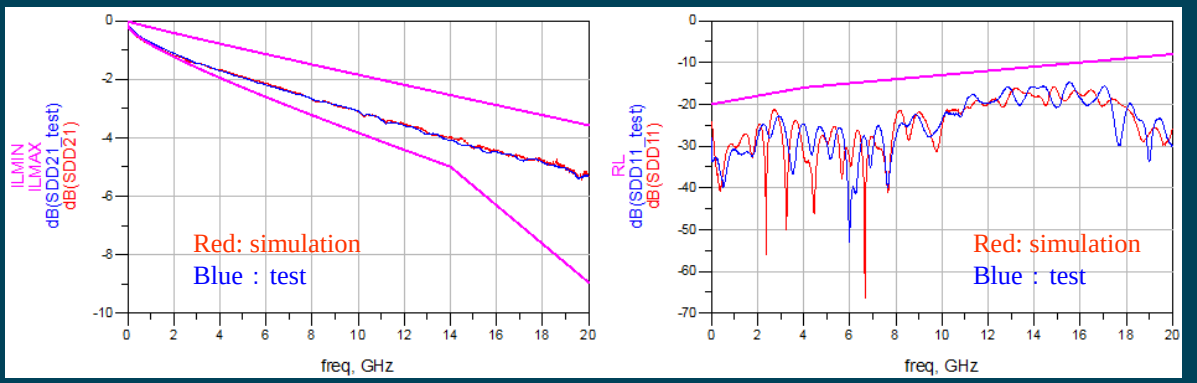


Connector Verification board, use AFR of PLTS to do calibration, to get real performance of the material after fabrication

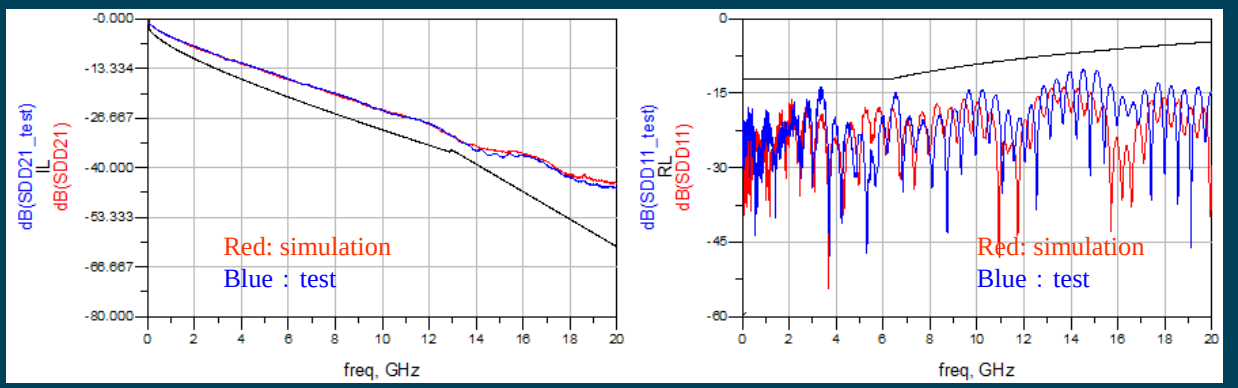


100G Testing Fixture Design

Get parameters from real evaluation board of material and connectors, then simulate to get the performance of the whole trace

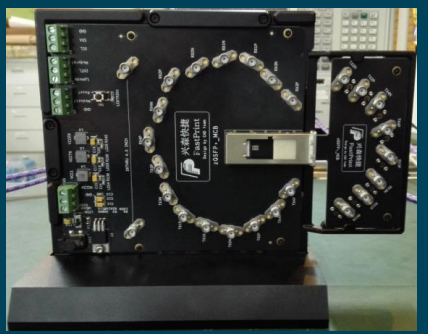


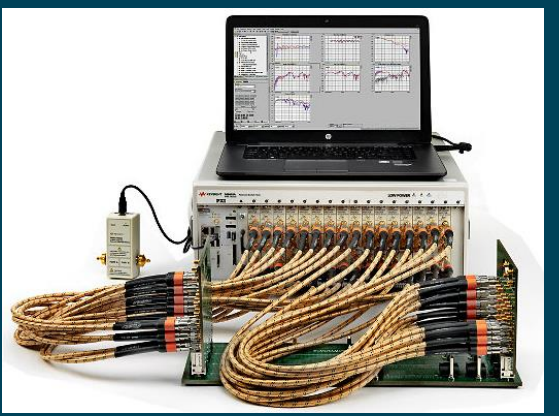
This method works for long distance board also (40inch, Meet IEEE802.3bj Spec)

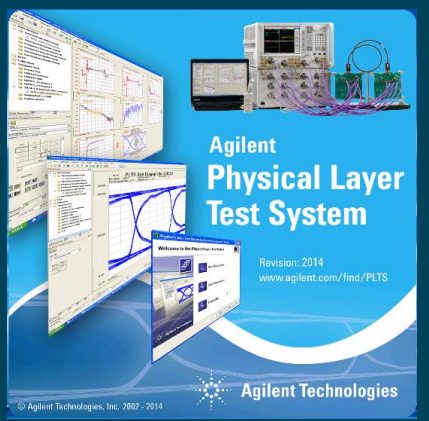


Fixture Verification based on PLTS

MCB and HCB Verification







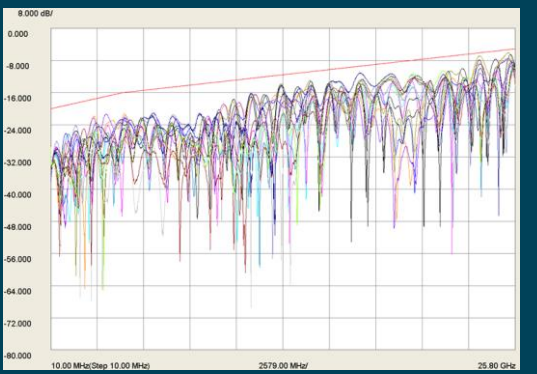
Testing Setup :

1. Keysight PXI Modular network analyzer
2. PLTS physical layer testing SW
3. Calibration kits, Coaxial Cables, etc.

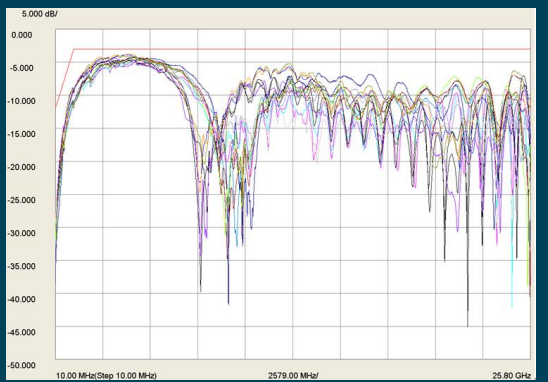
Fixture Verification based on PLTS

Comparison with IEEE802.3bj Spec

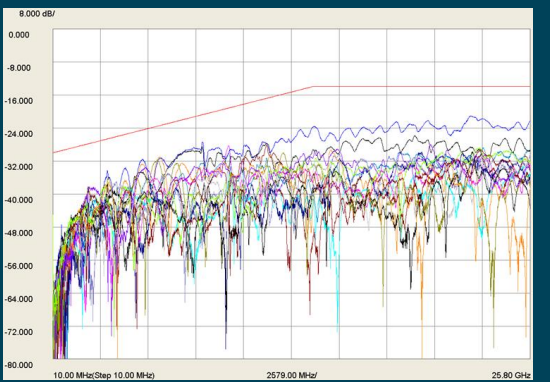
Differential insertion loss



Differential Return loss



Common Return loss



Differential to Common Mode insertion loss

Conclusion

- High-Speed Testing moved from some independent modules to an integrated complex system
- To design a testing fixture which perform as good as expected, we need to evaluate material, stackup, trace, via, interconnection and connectors to get real performance of each segment, then simulate the whole trace to get whole trace performance.
- Fixture verification based on PLTS gives the fixture performance comparing with Specification
- The same methodology can be leveraged to cover higher and higher testing requirement in ATE environment.