
EIGHTEENTH ANNUAL
BiTS
TM
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 1
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Session 1

Marc Moessinger

Session Chair

BiTS Workshop 2017 Schedule

Performance Day

Monday March 6 - 10:30 am

Driving Performance

"Design for performance and advanced characterization of new contactors"

Markus Wagner – Cohu & Milen Cheshmedjiev – Melexis

"Investigation into Various Via Structures in High Speed Interconnect"

Carol McCuen - R&D Altanova

"Contactor and Package Design Effects on Crosstalk"

Noureen Sajid & Jeff Sherry - Johnstech International

"Contactor Based Final Test at 77 GHz on a Multi-Channel Radar Transceiver Chipset"

Brian Nakai & Jeffrey Finder - NXP Semiconductors

BiTS Burn-in & Test Strategies Workshop 2017

Investigation into Various Via Structures in High Speed Interconnect

Carol McCuen

R&D Altanova Semiconductor IC Test

BiTS Workshop
March 5 - 8, 2017

Overview

A. Review of the "Need for Speed" -- High Frequency Applications

B. S-parameters and Eye Diagrams of similar Interconnect,
   - 25 mm long 50 Ω stripline trace
   - 350um pitch via structure at one end
   - Tuned 3 x 3 via structure at other end

   in two different Interconnect Processes.

   I. Conventional Fine Pitch PCB Process
   II. Build-Up Technology
      a. Traditional Staggered (Offset) vias, pads on every layer
      b. Traditional Aligned vias, pads on every layer
      c. Damascene, Padless vias, deposition then planarization after every layer

C. Continued Work

Need for High-Speed Interconnect

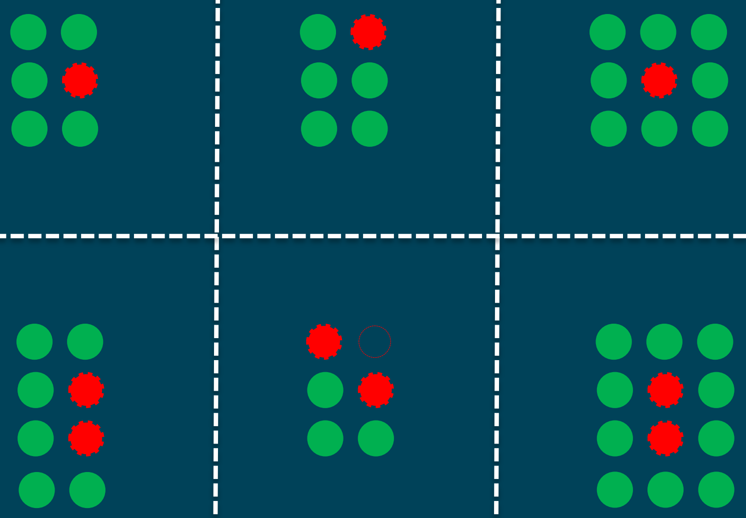
- Transmit/Receive Frequencies for 4G (700 MHz to 6 GHz) and 5G (14, 28, 39, 64 GHz) "smart" wireless devices are going into millimeter wave range.
- Parallelism in computing has lead to off-chip signaling interfaces at 56Gbps, also PCI Express 3.0.
- Data centers and Cloud Computing using 100Gbps Ethernet that require 28 and 56 Gbps in copper before going optical.

Various Via Structures in 350 um Pitch
(will not show all data in presentation)

Data Collected: Edge | Corner | Field

Single Ended:
- "Edge"
- "Corner"
- "Field"

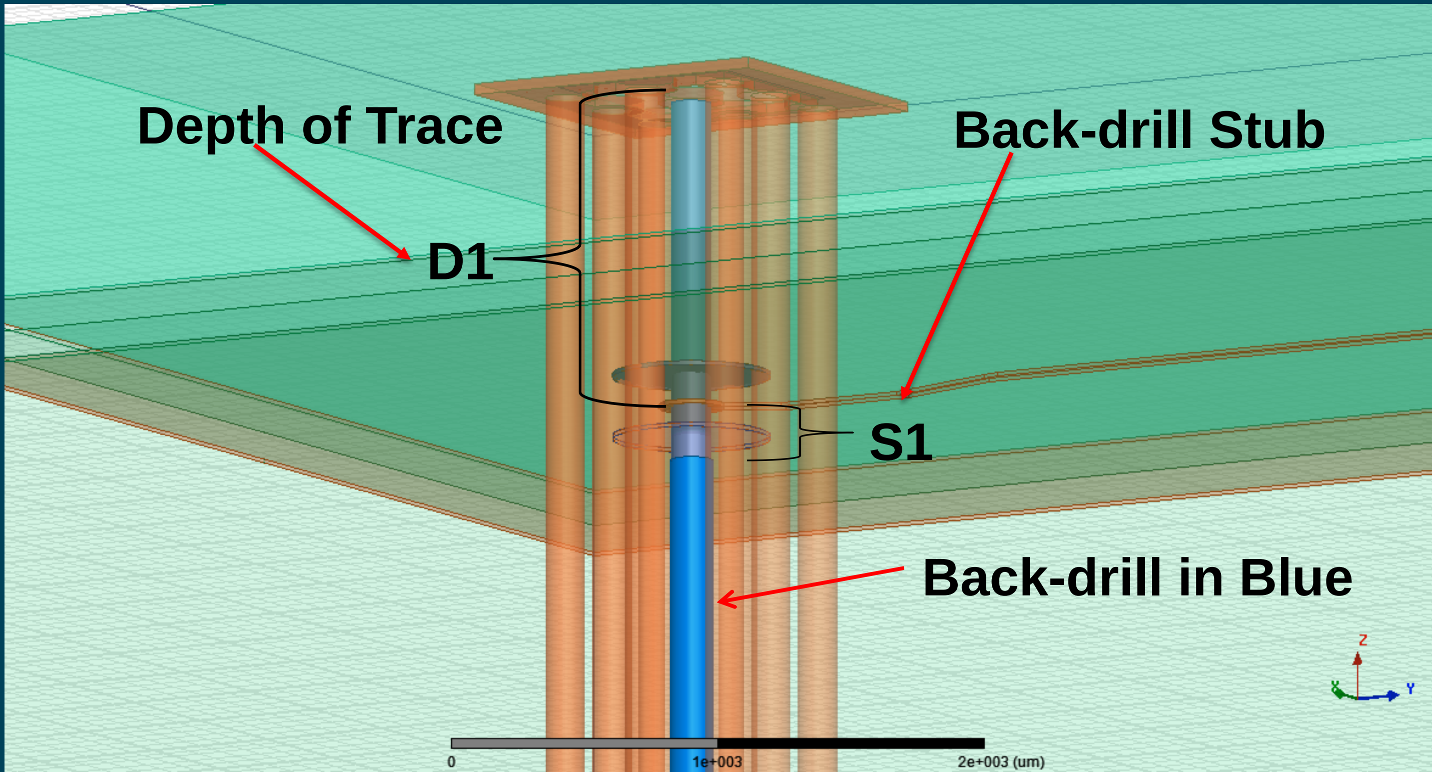
Differential:
- "Edge"
- "Corner"
- "Field"



Conventional Fine Pitch Via Structures

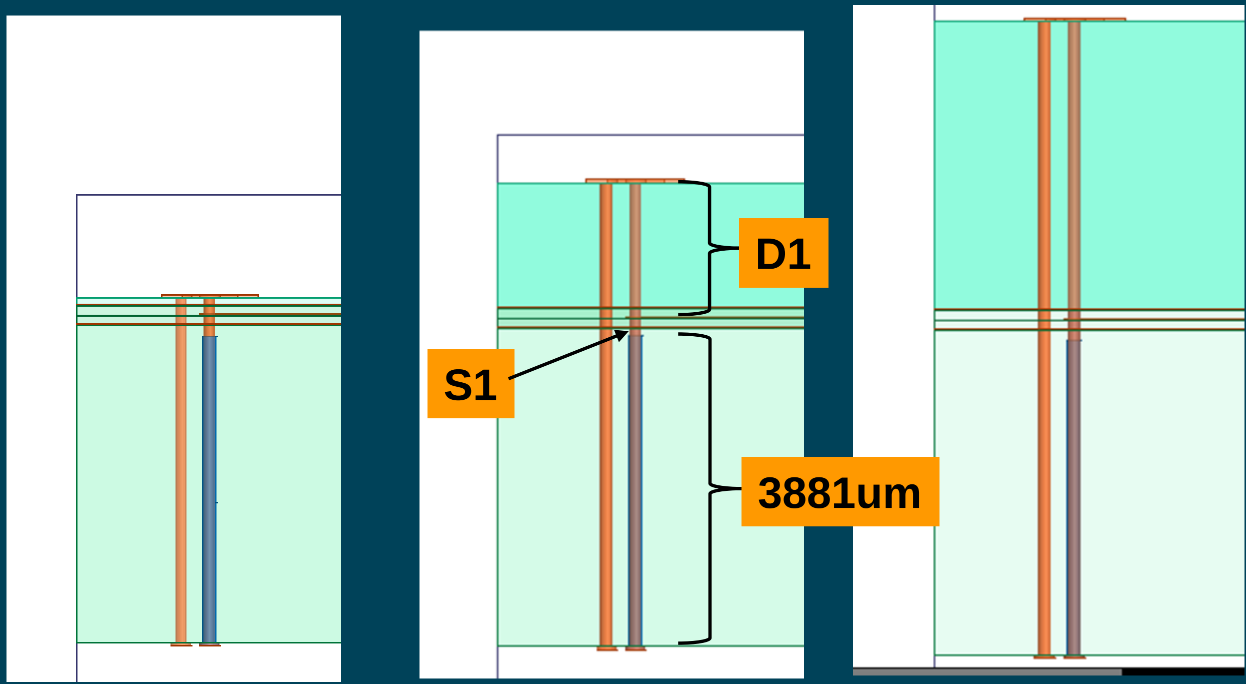
1) The Purpose is to Determine the Highest frequency of acceptable performance for a 350um Via Structure under several Trace and Via Conditions
   1) Vary Depth of the Trace, showing S-parameters of "Edge" Pattern only, leaving the substrate thickness below the trace constant, approximately 3.8mm.
   2) Vary length of Signal Via Stub, showing S-parameters of "Edge" Pattern only, up to 2000um long, remaining after Backdrill.
   3) Compare Impedance (TDR_Z) for three different Via Patterns.
   4) Create Eye Diagrams for a Differential and a Single Ended design.

Sweep Trace Depth and Via Stub Length



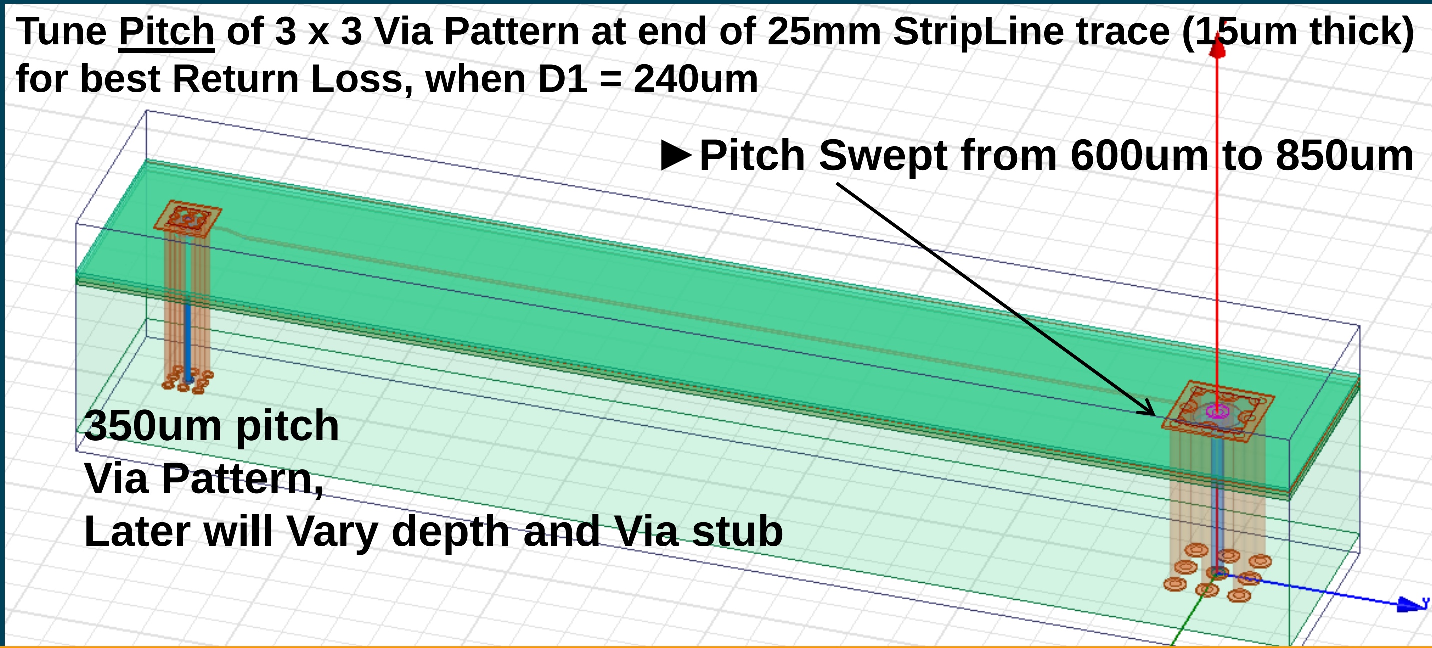
Range of Sweep for Depth of Trace below top surface

D1 = 240 um D1 = 1680 um D1 = 3600 um



Via Stub Length, S1, is 250 um for ALL shown

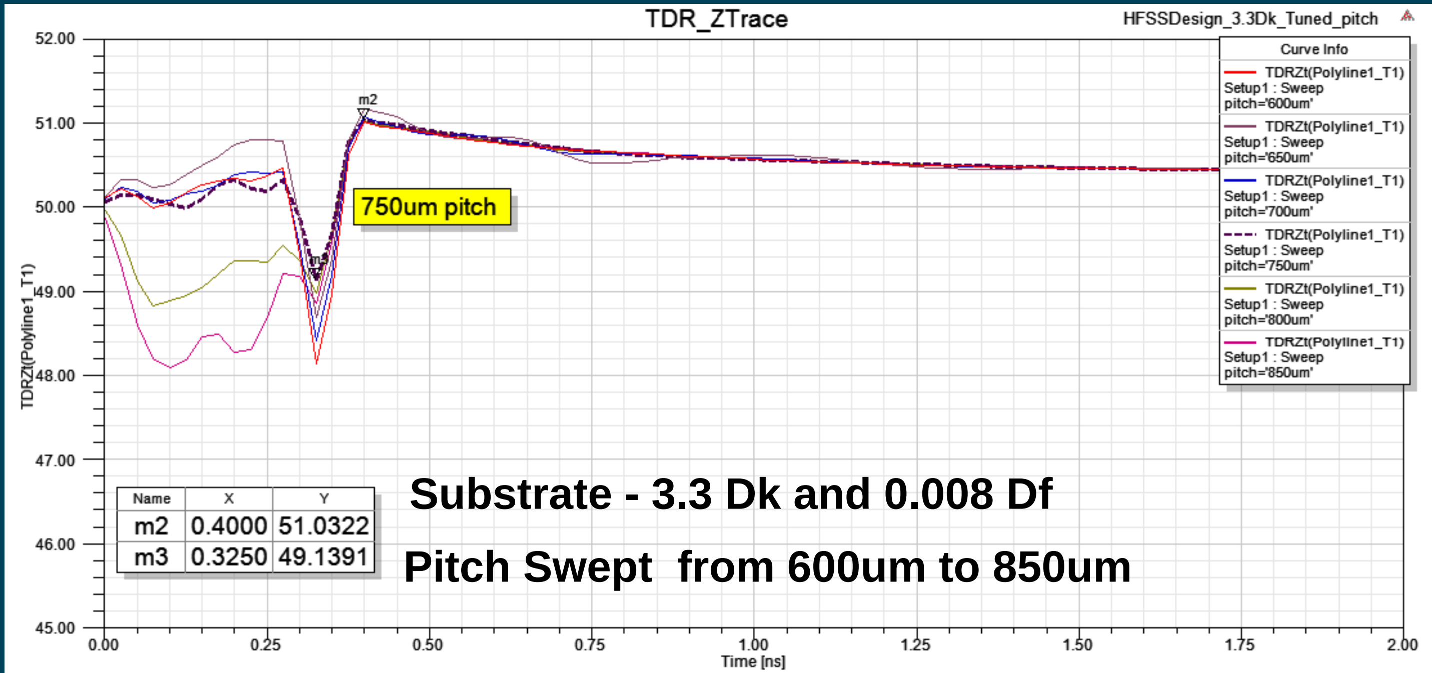
Optimize the Part of the model that remains constant – Trace and 3 x 3 Vias



N4800-20 Substrate - 3.3 Dk and 0.008 Df
Distance between Ground Planes – 223um
50Ω StripLine width – 86um, neck down to 50um between 350um pitch via

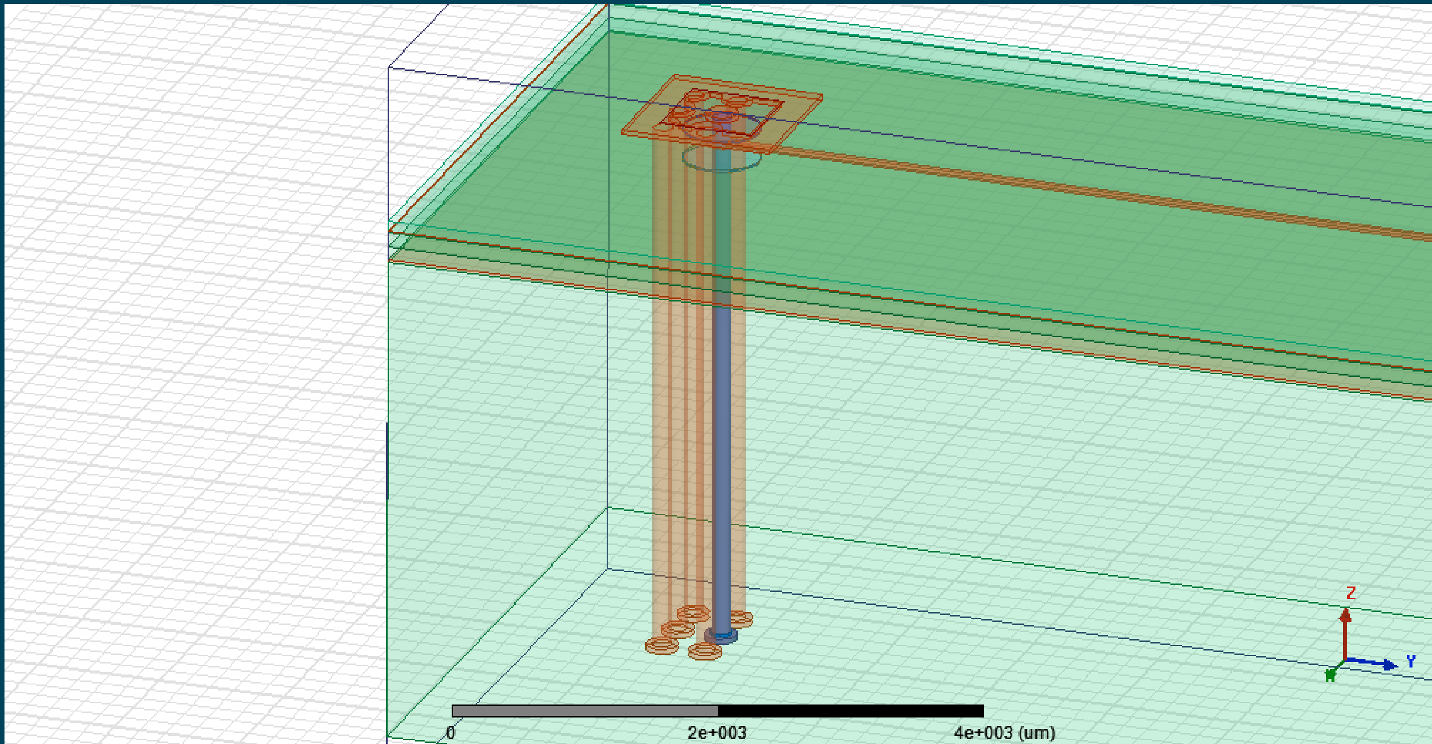
TDR_Z looking into end of 25 mm long *Removed the 350um Via Pattern*

Chose pitch of 750um for best 50 Ohm match



Name	X	Y
m2	0.4000	51.0322
m3	0.3250	49.1391

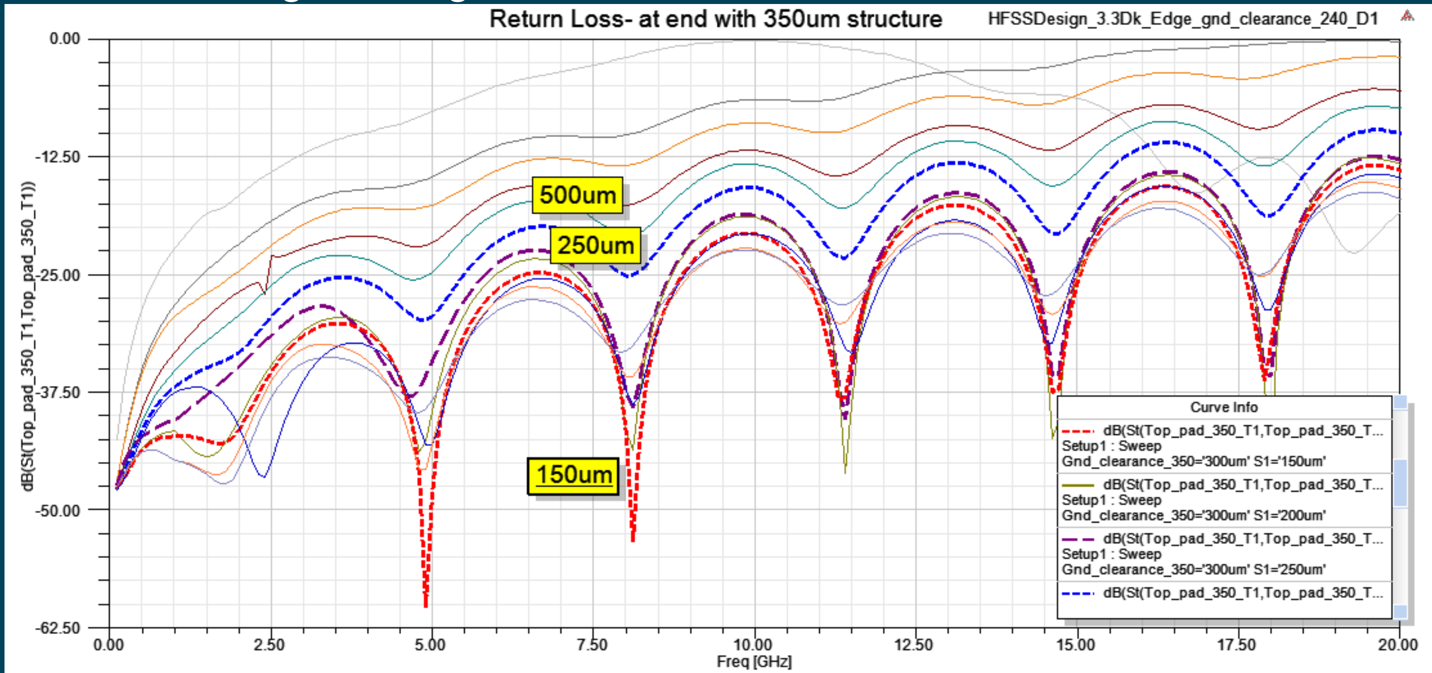
Now, onto the 350um Pitch Study- 1st Depth of Trace D1 = 240 um



1st Trace Depth 240um –
Showing all Via Stub Lengths, S1, 1 um to 2000um

"Edge"

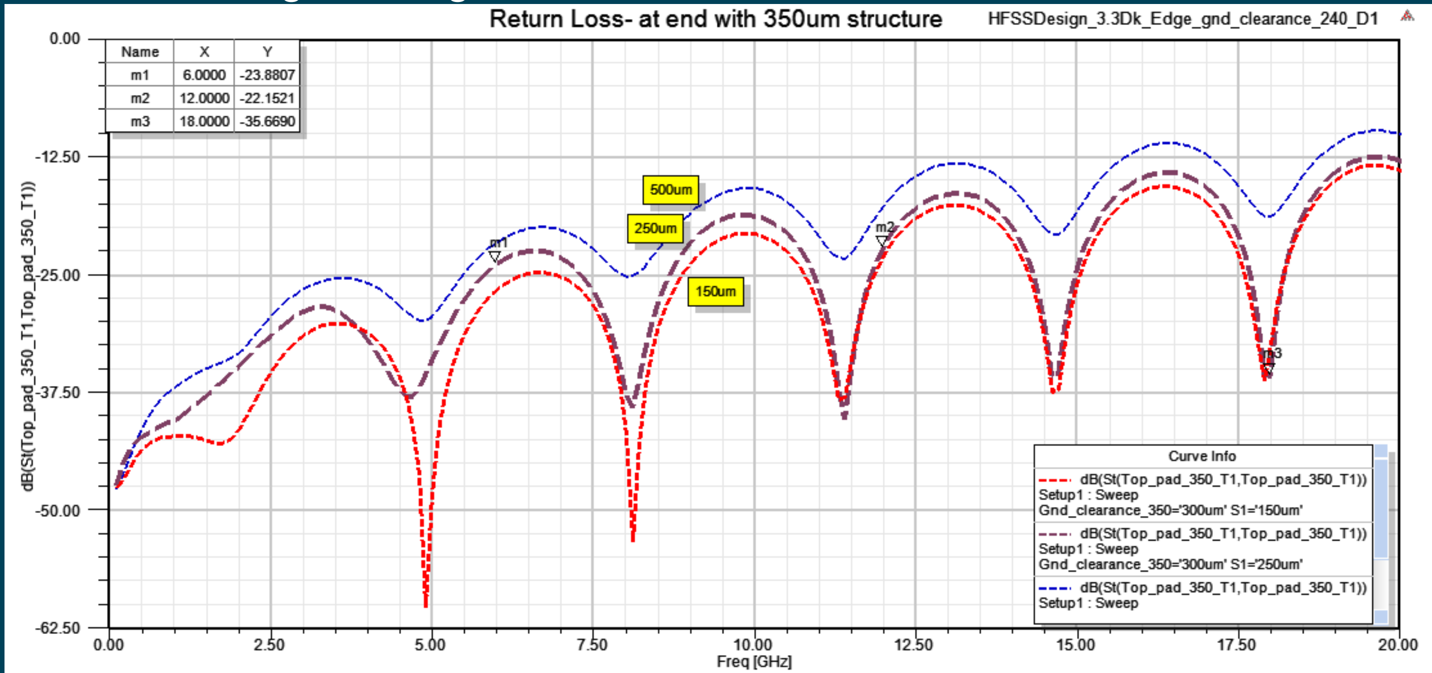
Manufacturing S1 range: 150um to 350um, 250um nominal



1st Trace Depth – D1=240um

"Edge"

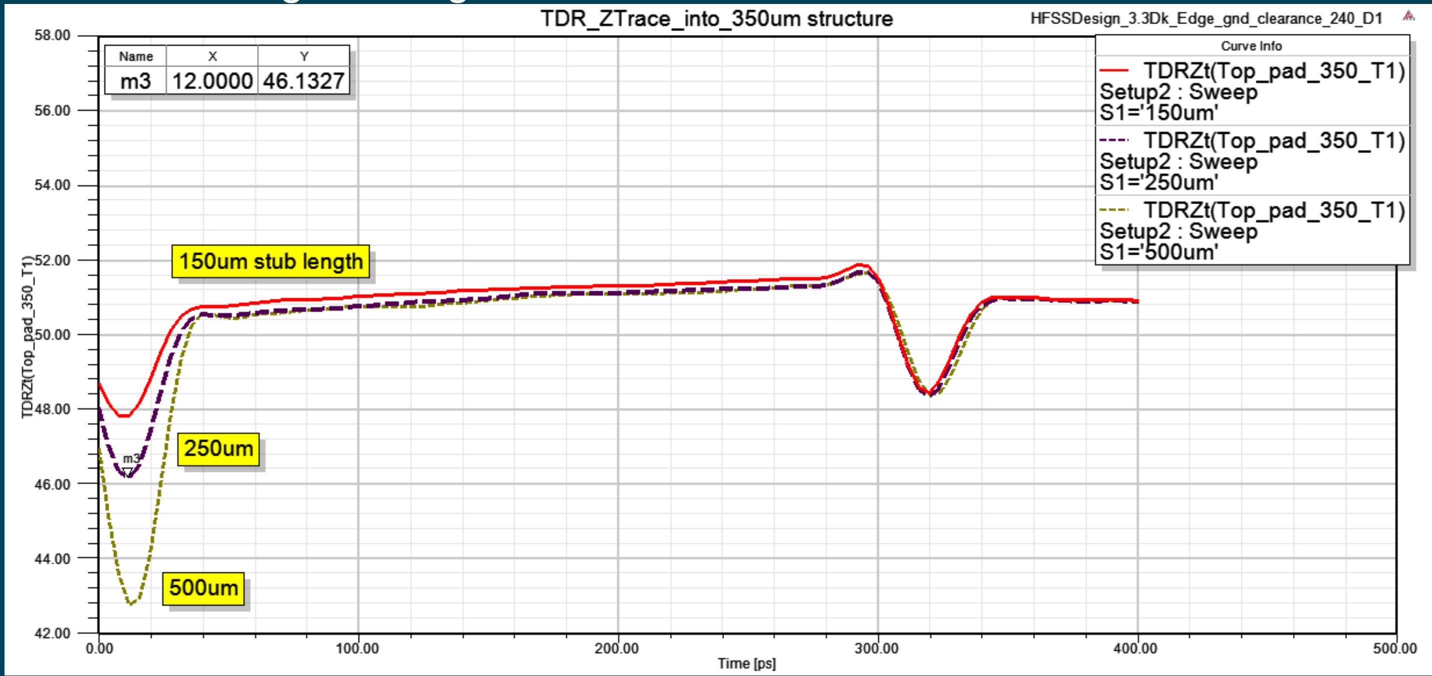
Manufacturing S1 range: 150um to 350um, 250um nominal



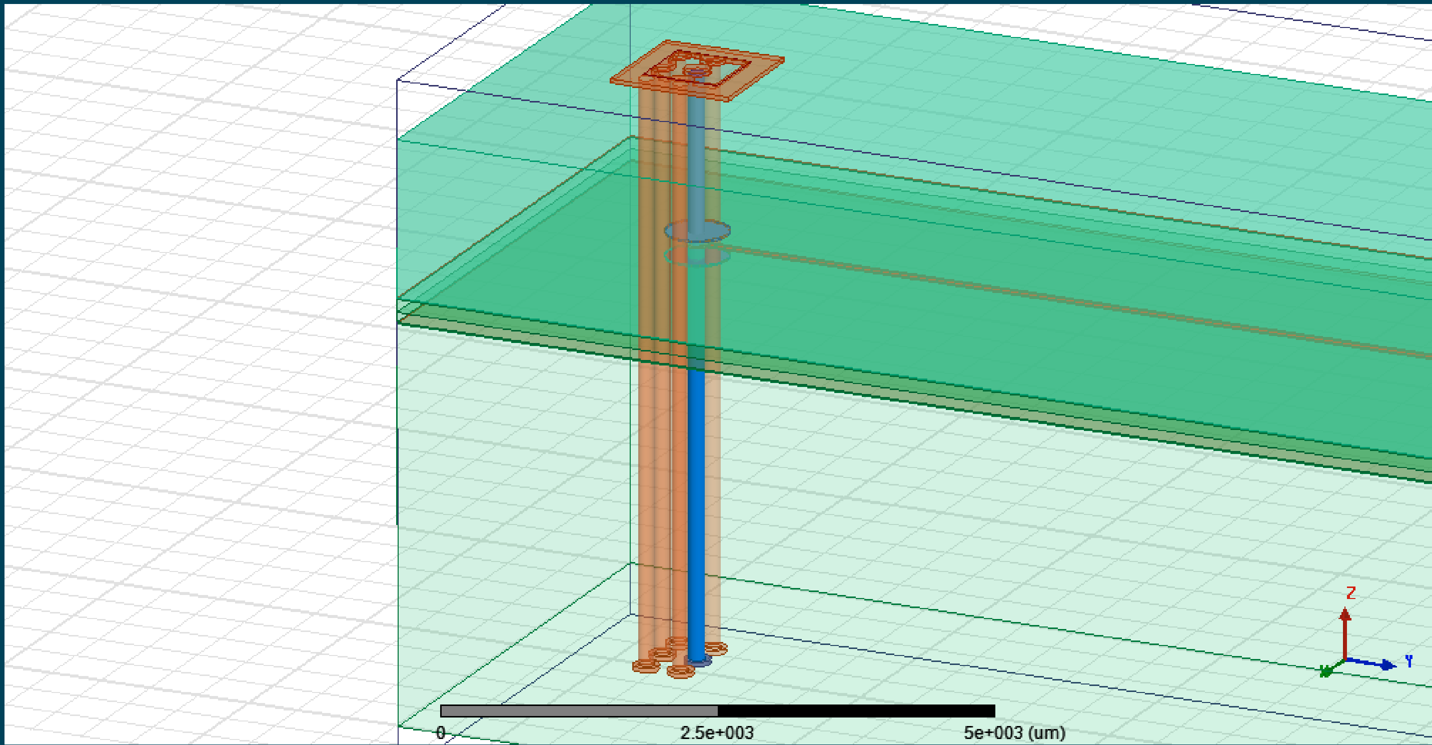
1st Trace Depth – D1=240um
Showing the effect of Stub on TDR_Z

"Edge"

Manufacturing S1 range: 150um to 350um, 250um nominal

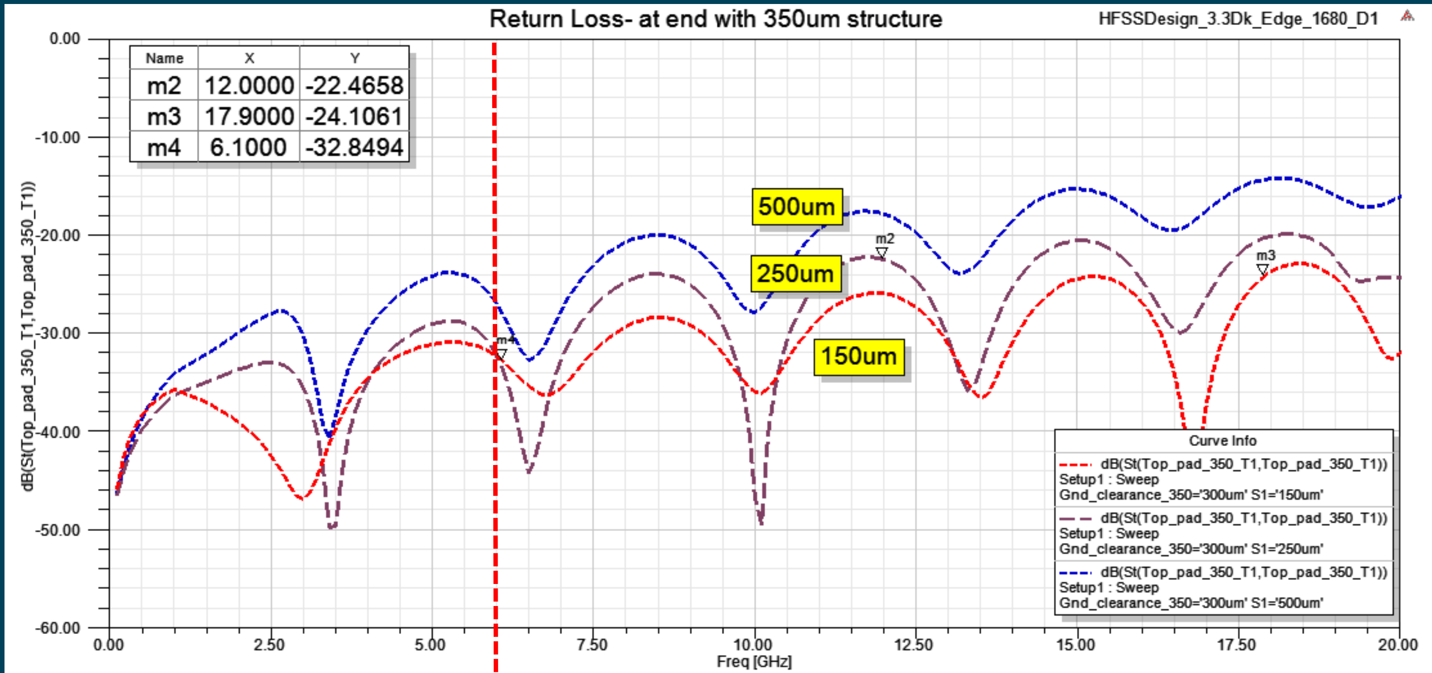


2nd Depth of Trace D1 = 1680 um



2nd Trace Depth – D1=1680um

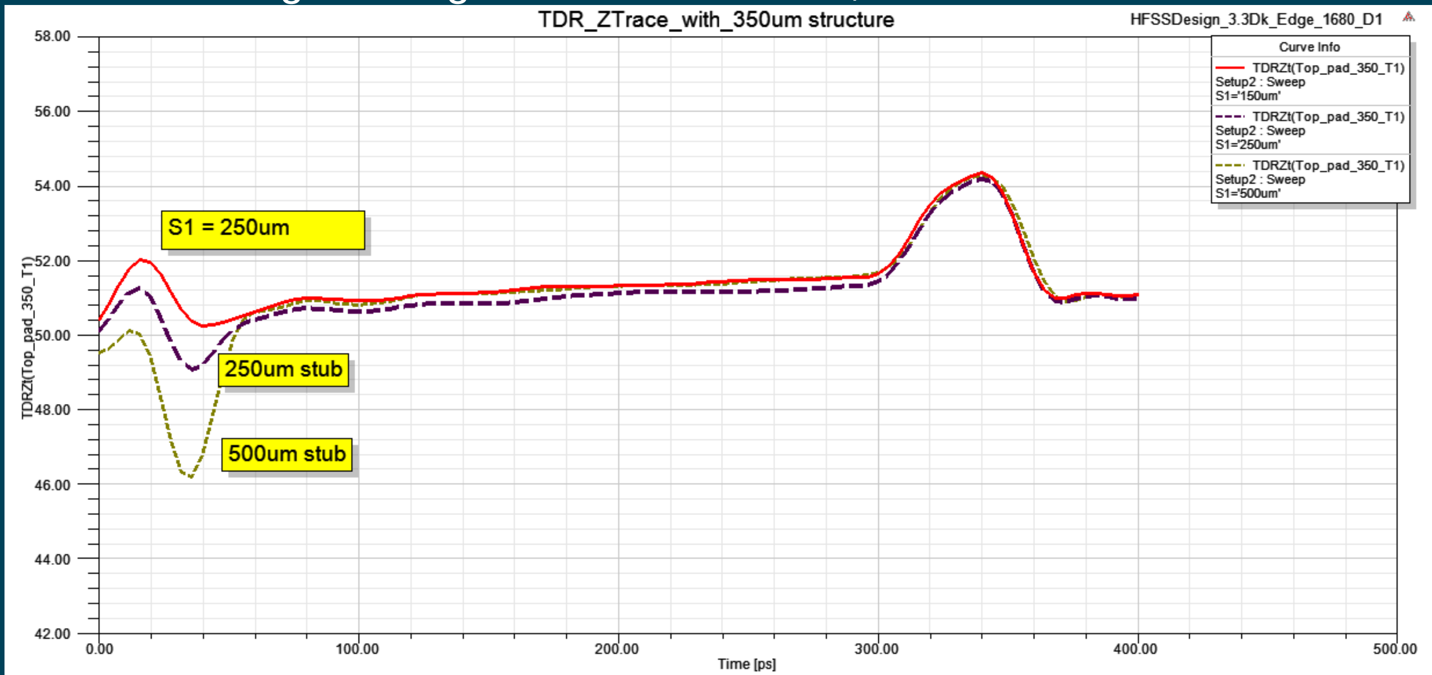
"Edge"
Manufacturing S1 range: 150um to 350um, 250um nominal



1st Trace Depth – D1=1680um Showing the effect of Stub on TDR_Z

"Edge"

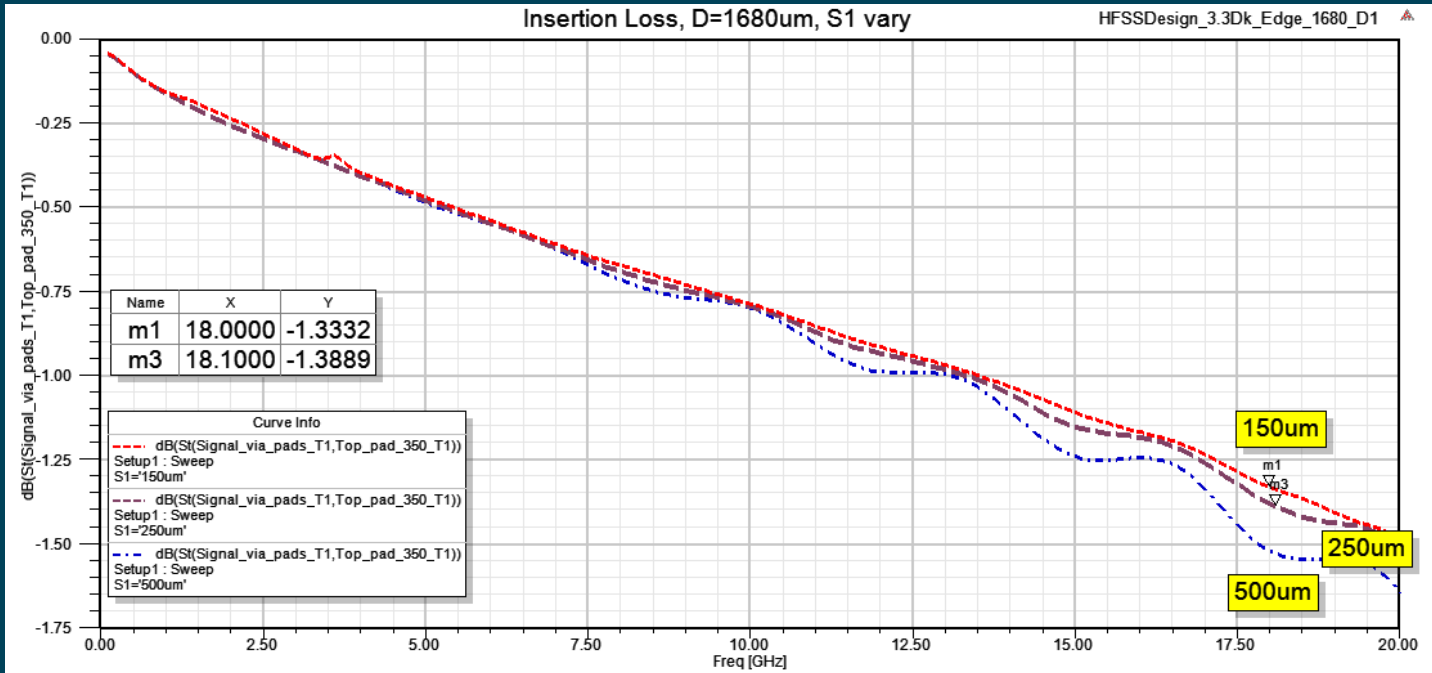
Manufacturing S1 range: 150um to 350um, 250um nominal



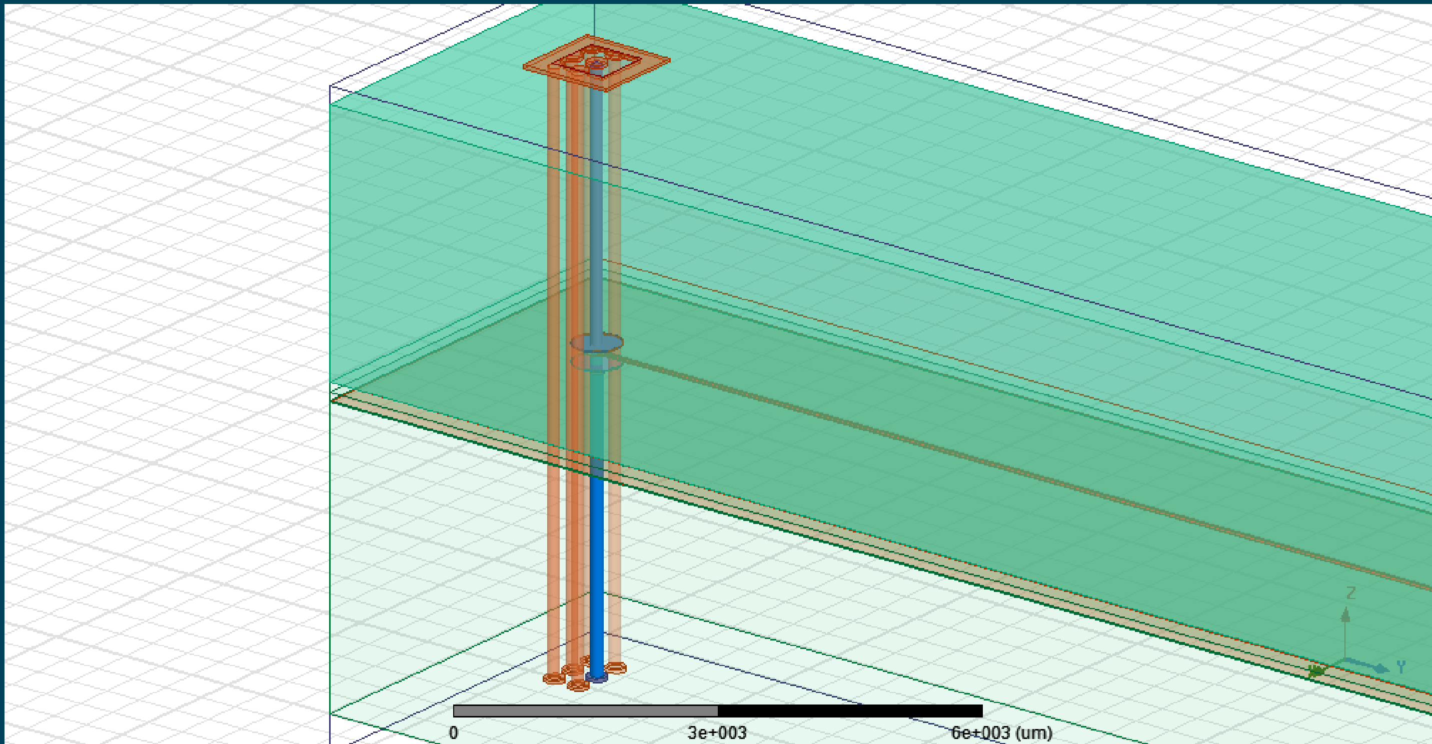
2nd Trace Depth – D1=1680um

"Edge"

Manufacturing S1 range: 150um to 350um, 250um nominal

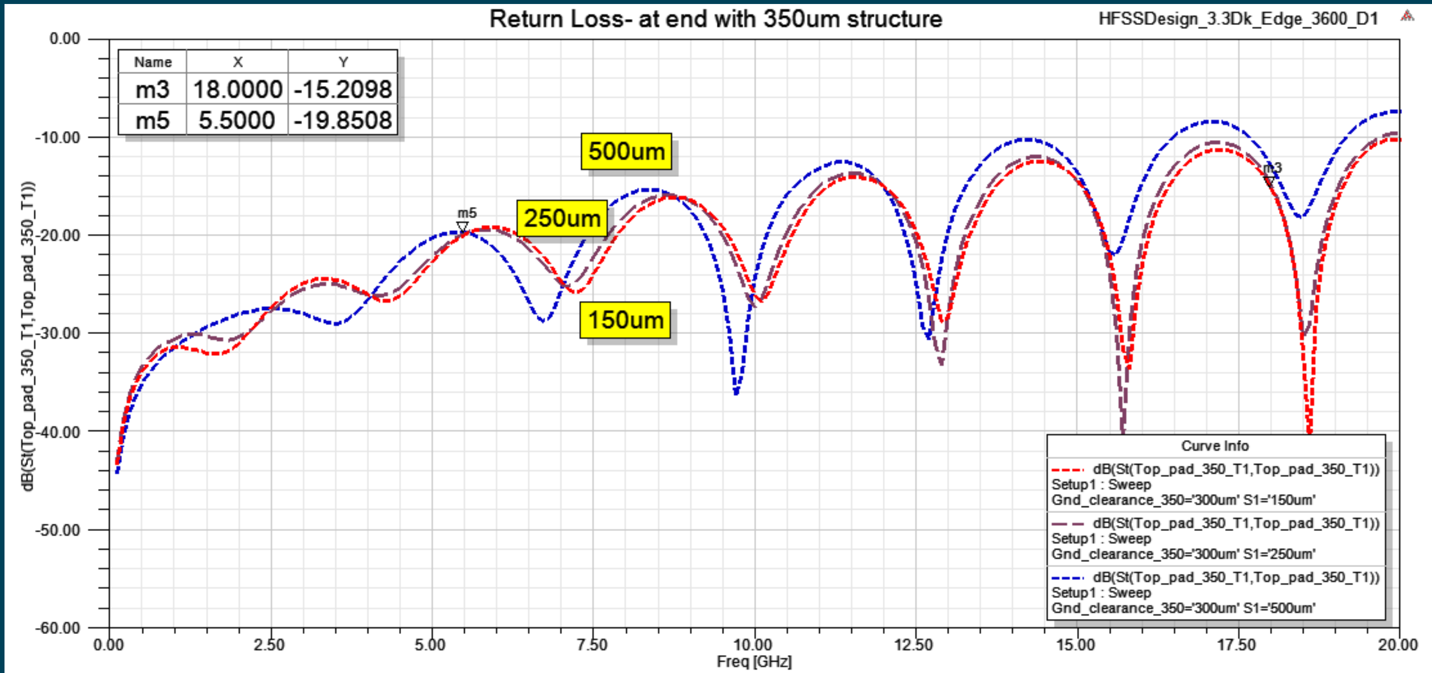


3rd Depth of Trace D1 = 3600 um



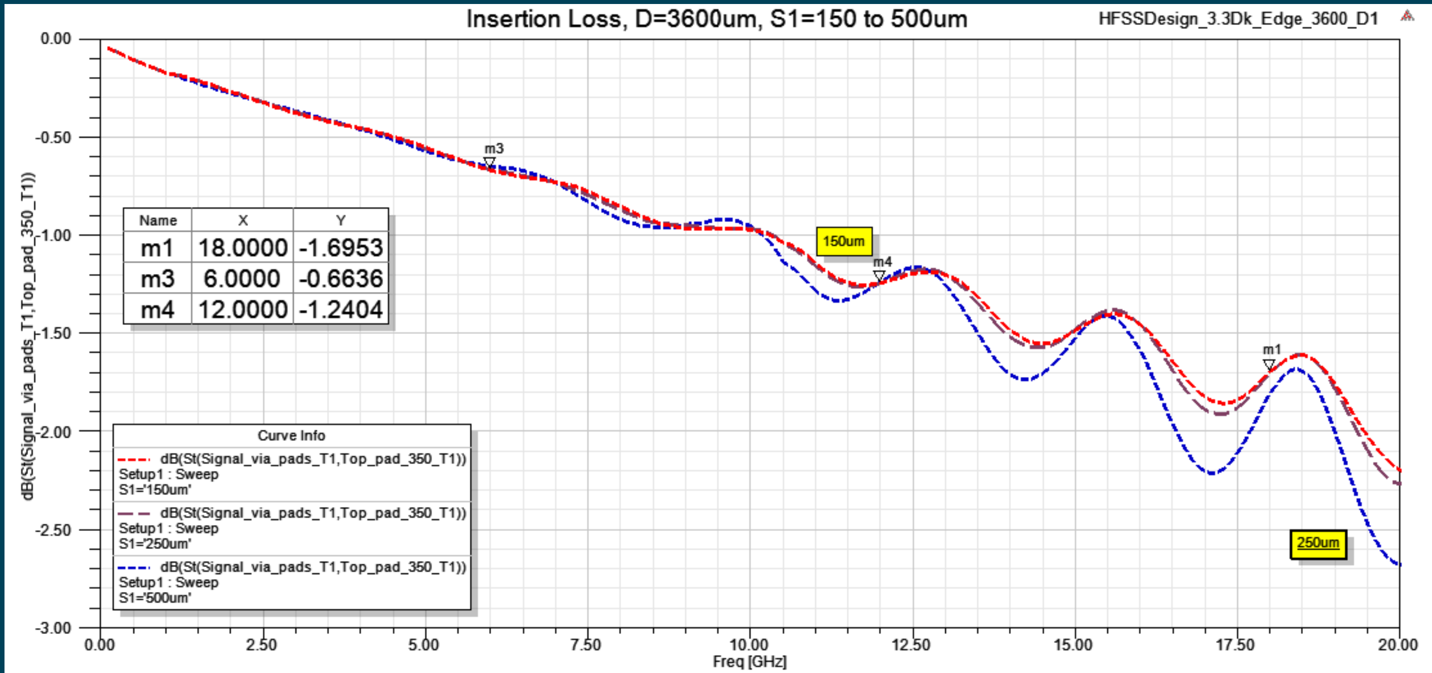
3^{rd} Trace Depth – D1=3600um

"Edge"
Manufacturing S1 range: 150um to 350um, 250um nominal

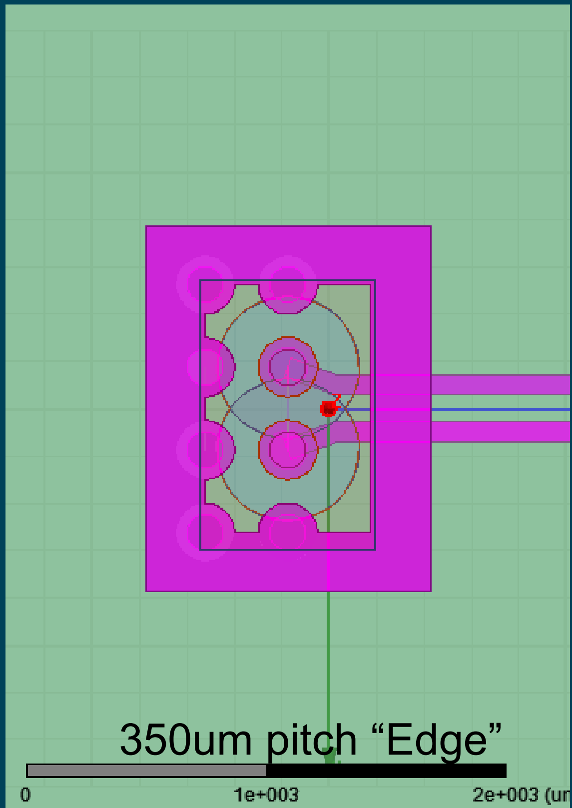


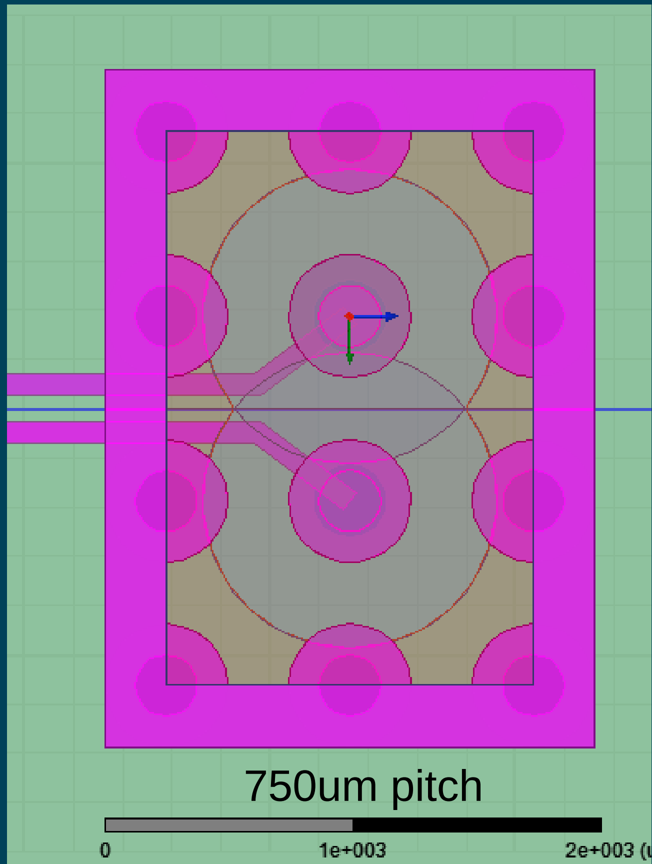
3rd Trace Depth – D1=3600um

"Edge"
D1 = 3600um, S1 = Manufacturing range of 150um to 350um.

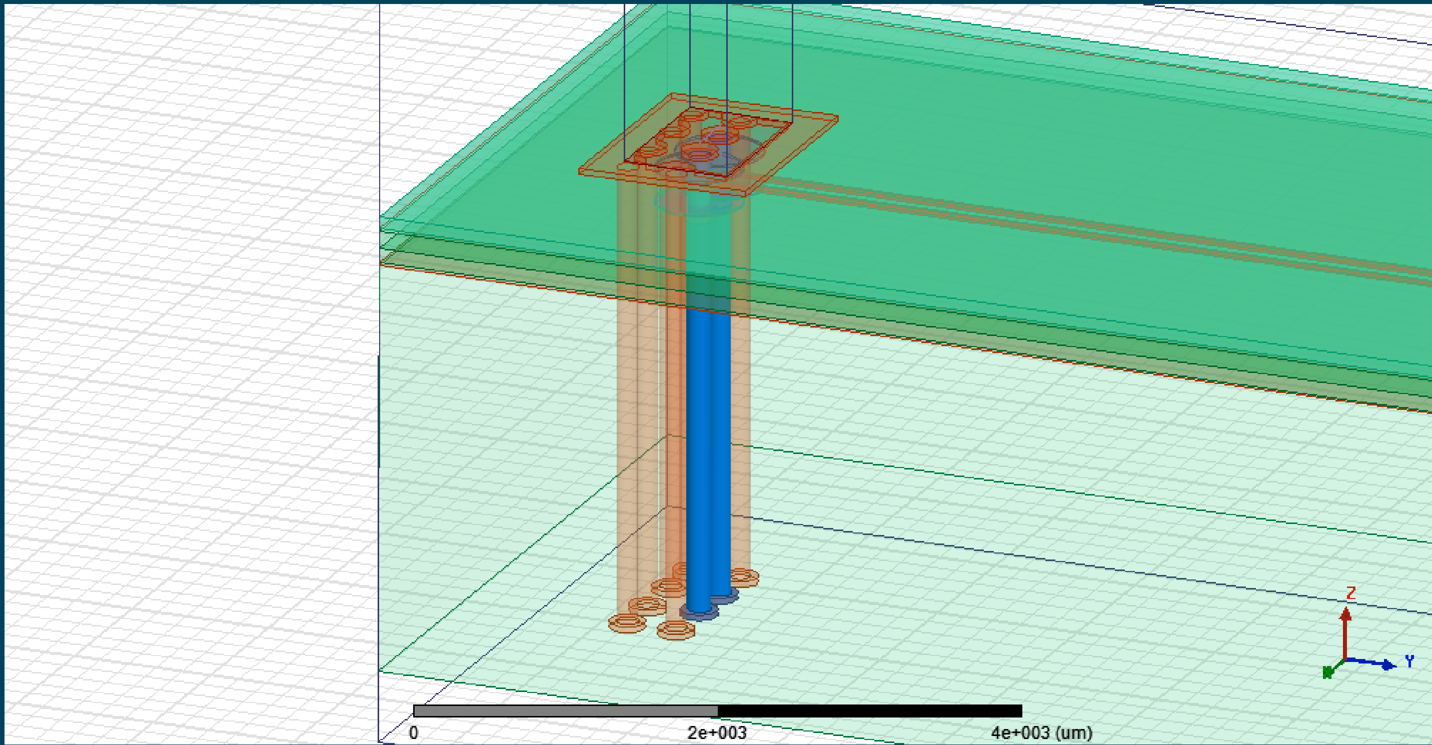


Differential Trace and Ground pattern for top of PCB





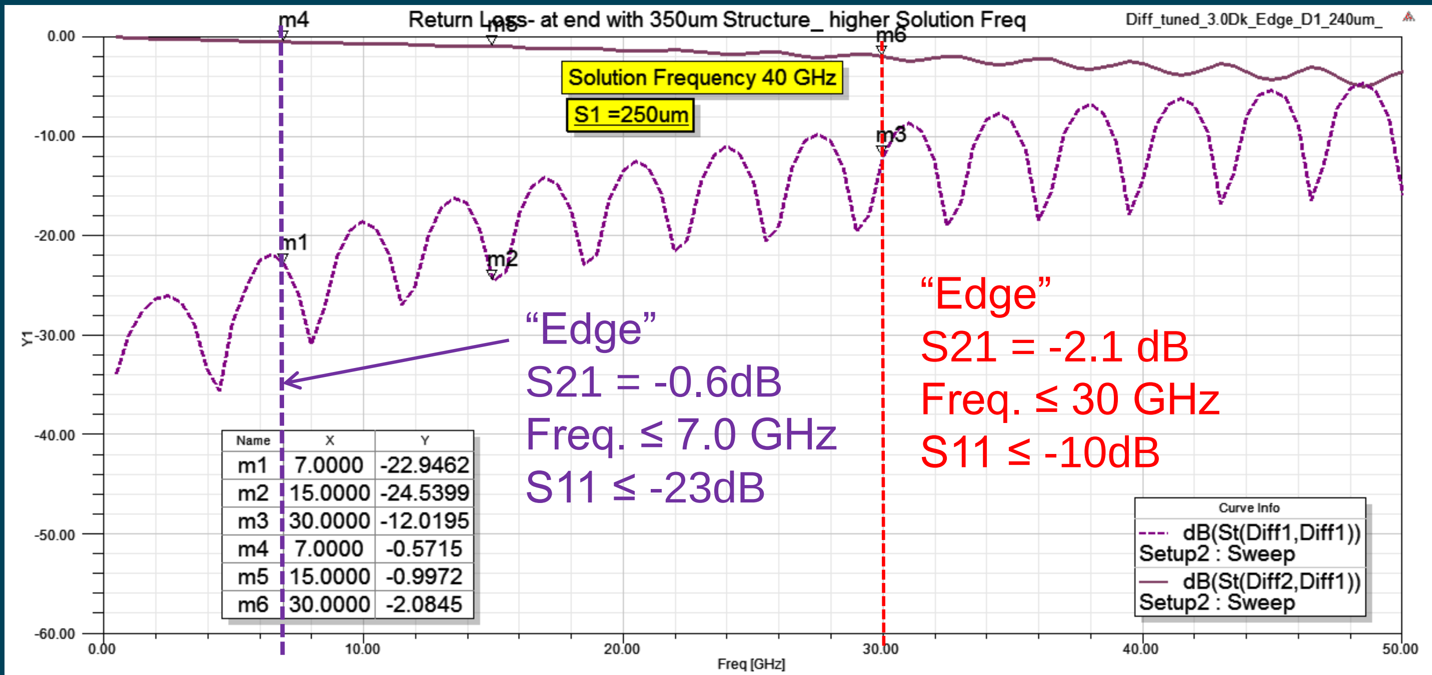
1st Depth of Differential Trace D1 = 240um



1st Trace Depth 240um – Differential

“Edge”

D1 = 240um, S1 = Manufacturing range of 150um to 350um.

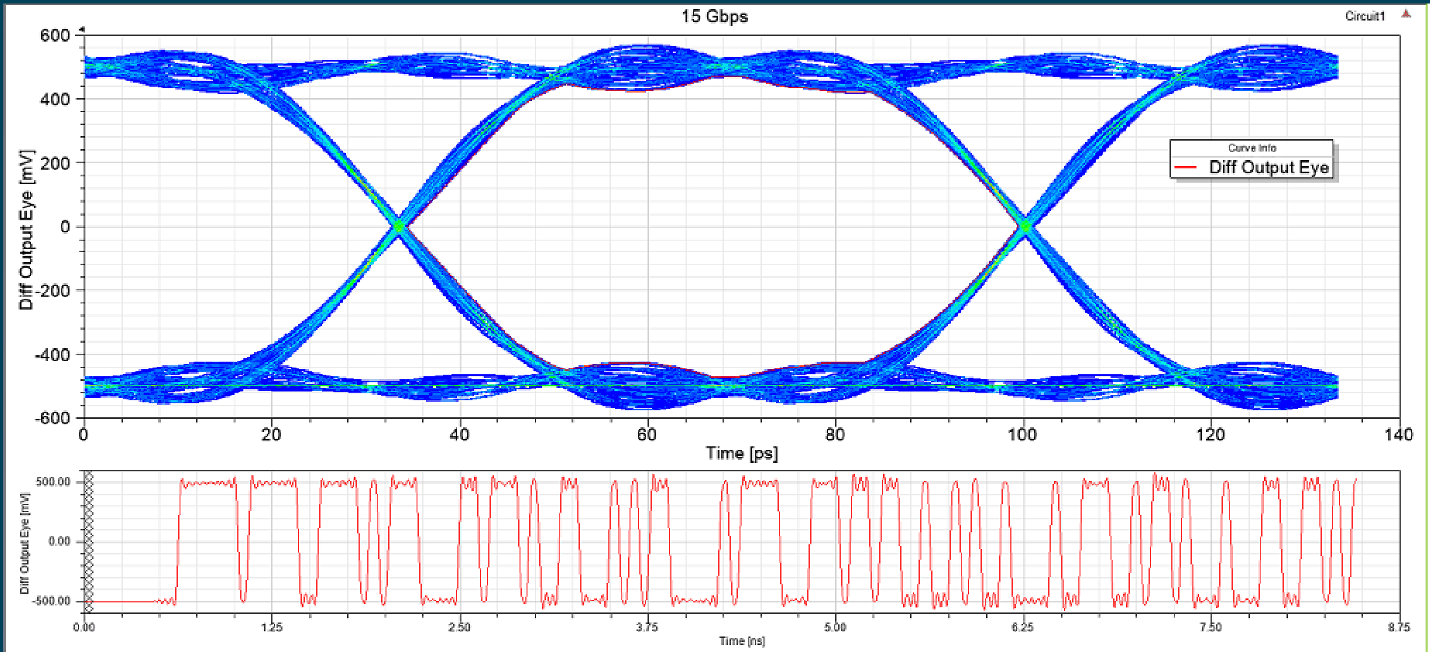


Increase Frequency Sweep – 50GHz

1st Trace Depth 240um – Differential

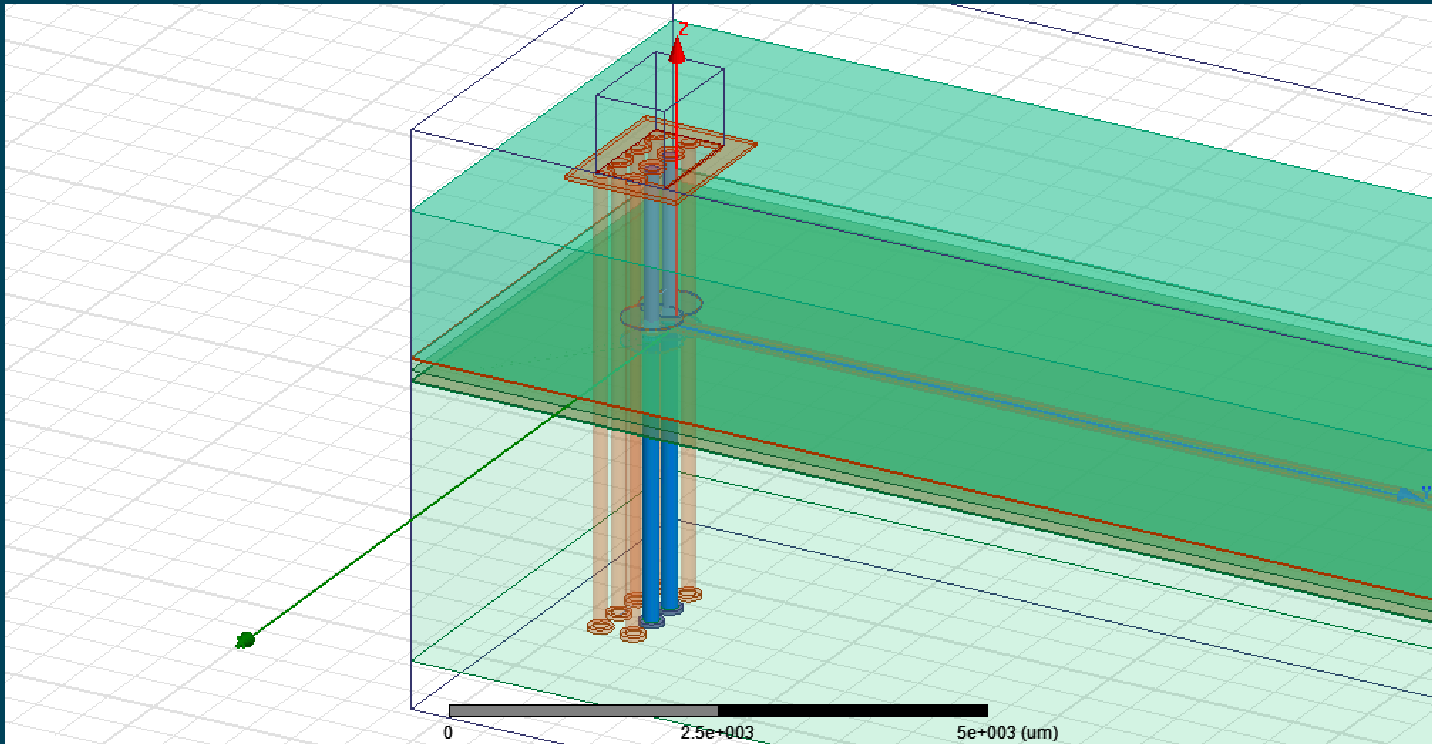
15 Gbps PRBS7 Eye Diagram

S1 = 250um, nominal



Not the Highest Possible Data Rate for this via pattern

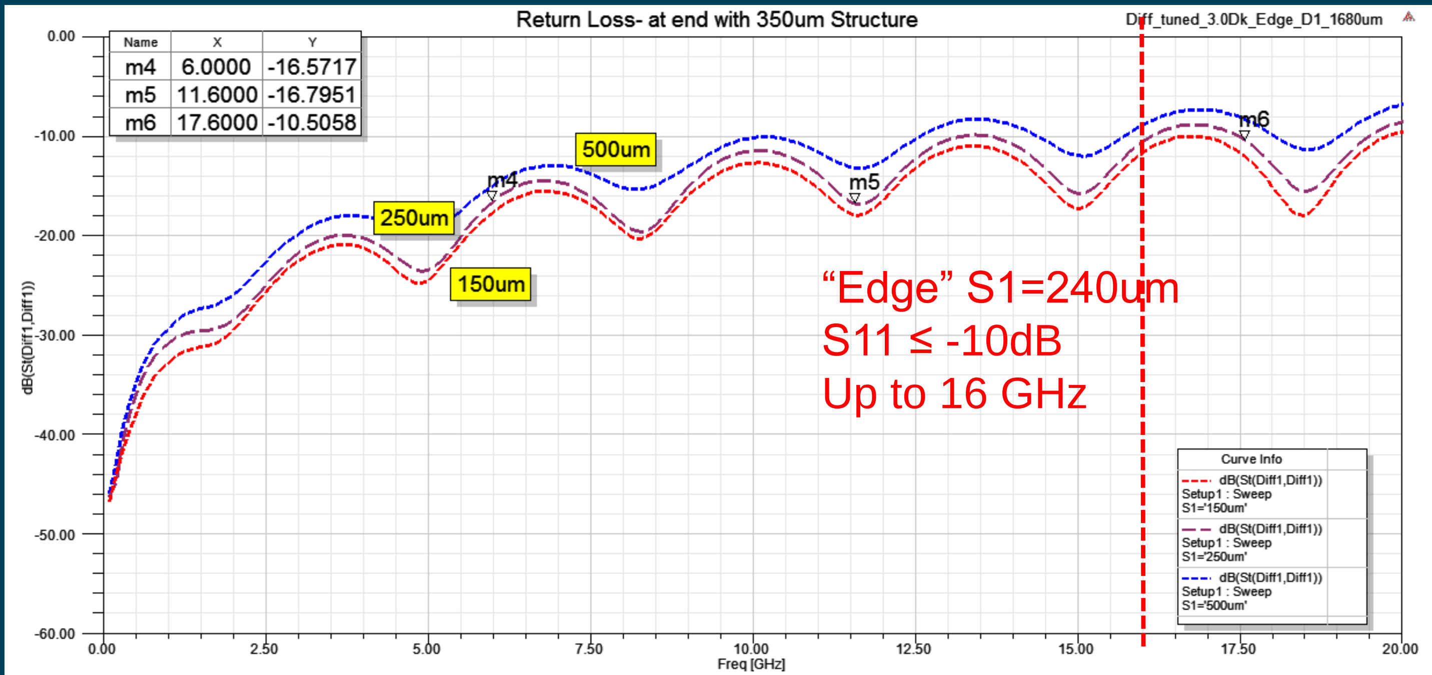
2nd Depth of Differential Trace D1 = 1680um



2nd Trace Depth 1680um – Differential

"Edge"

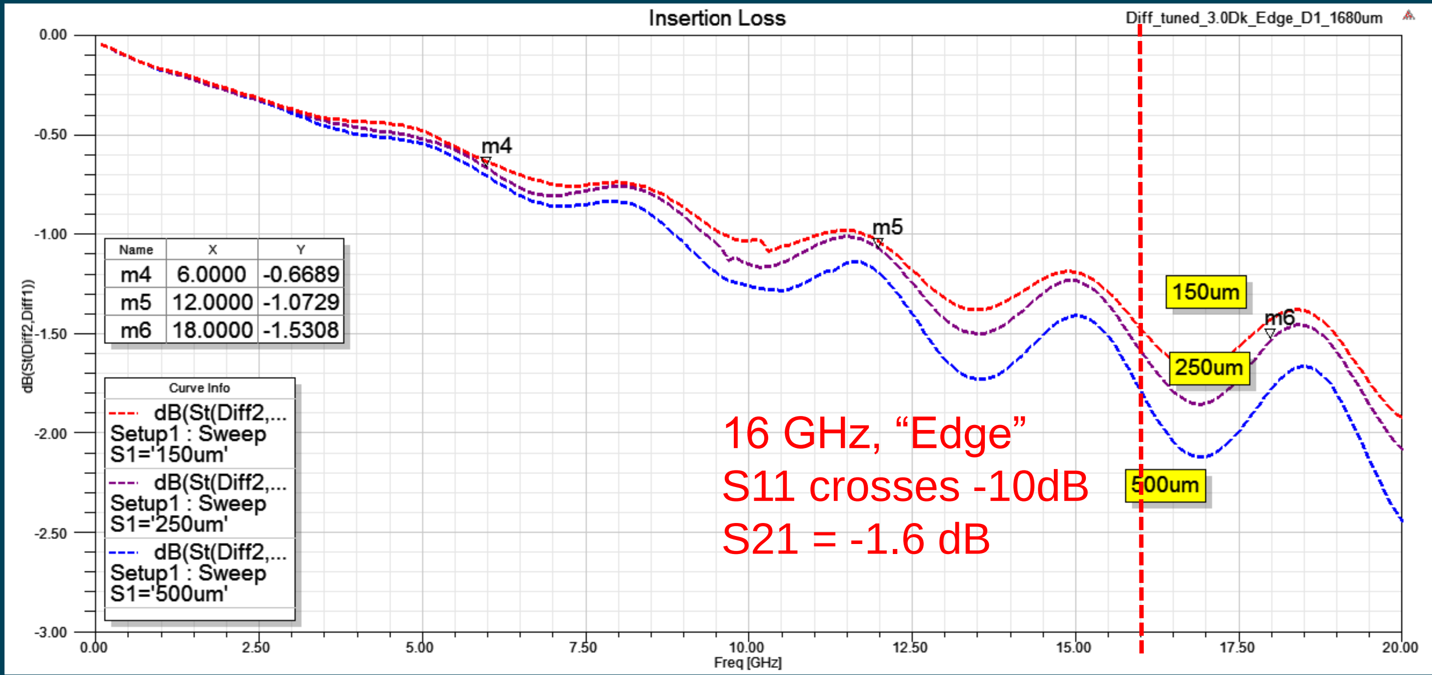
D1 = 1680um, S1 = Manufacturing range of 150um to 350um.



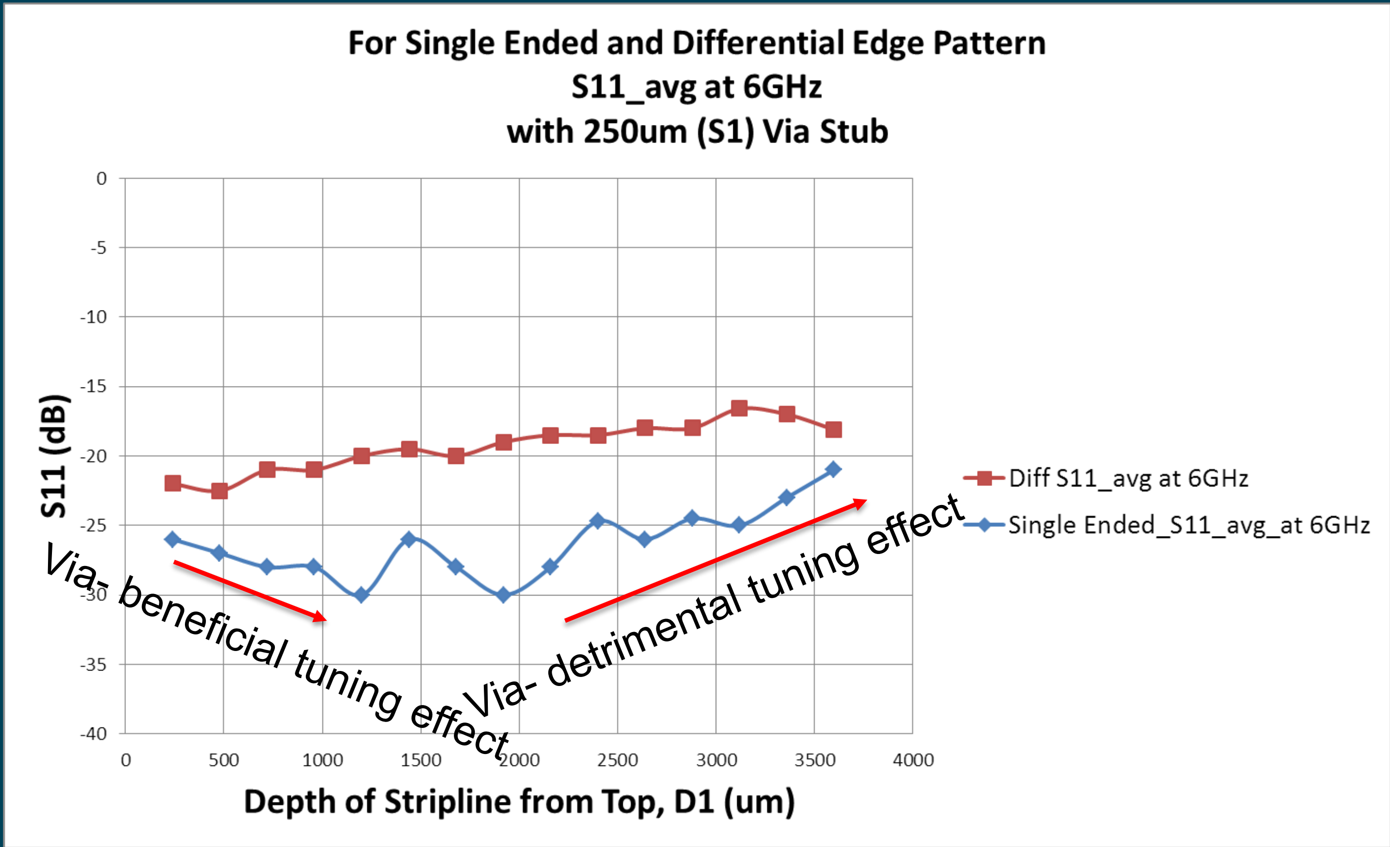
2nd Trace Depth 1680um – Differential

"Edge"

D1 = 1680um, S1 = Manufacturing range of 150um to 350um.



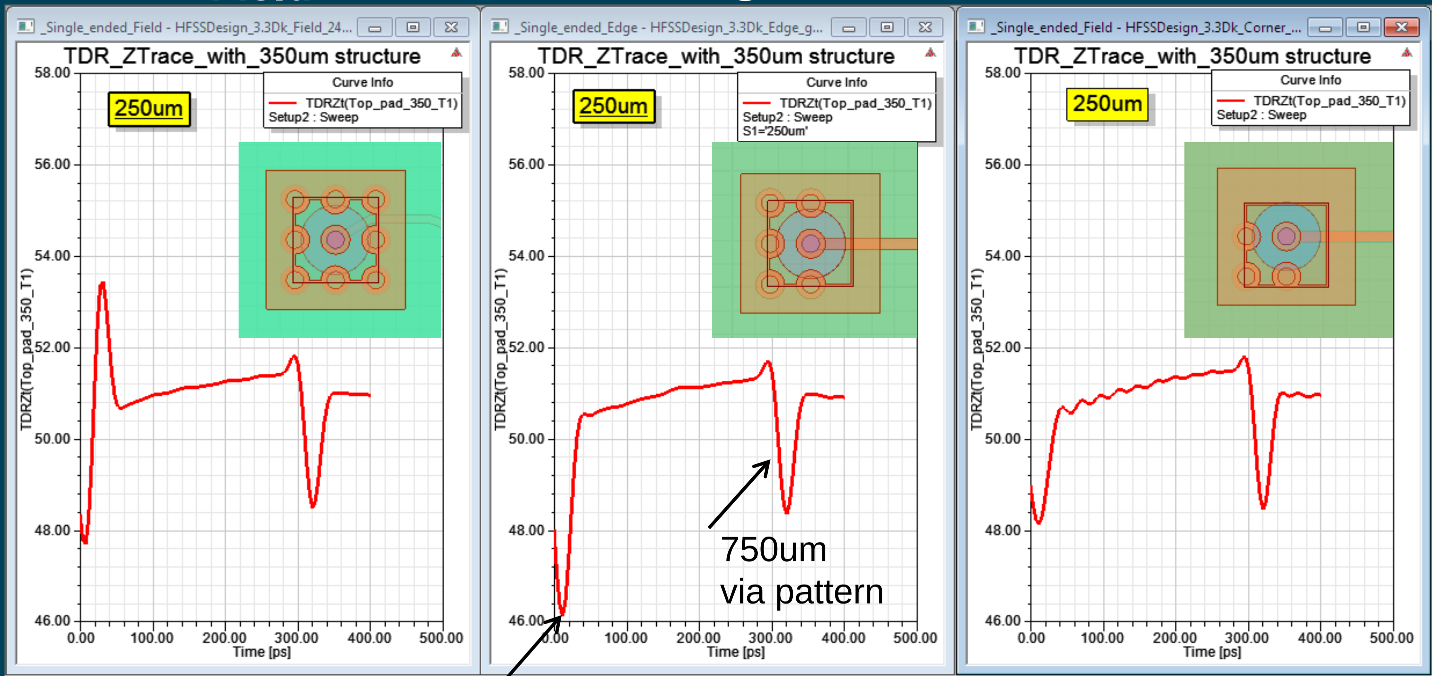
Collect All Trace Depths for SE Edge @ 6GHz Holding the Via Stub at 250um



Compare TDR_Z SE Via Patterns

Trace Depth (240um) and Via Stub S1 = 250um.

"Field" "Edge" "Corner"



Gnd Clearance Diameter - 600um

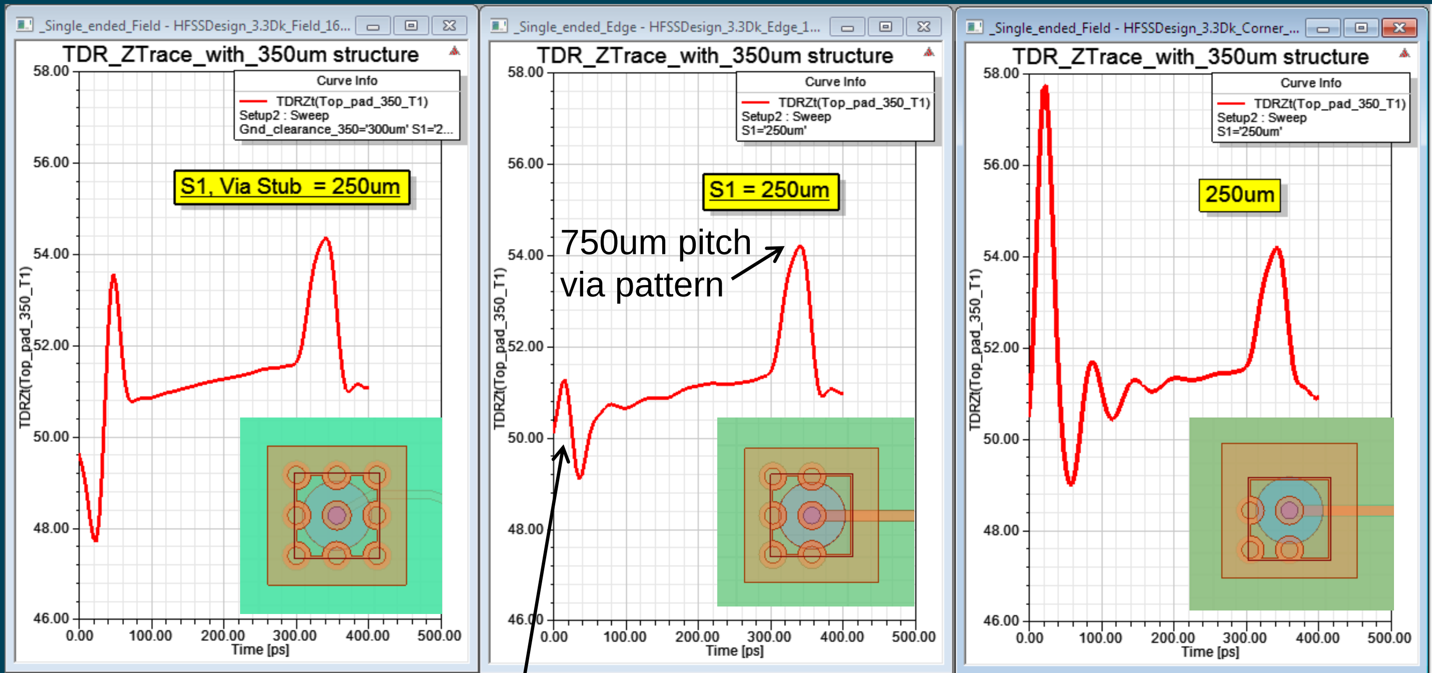
350um pitch via pattern

TDR_Z from simulations with higher Sweep frequency

Compare TDR_Z SE Via Patterns

Trace Depth (1680um) and Via Stub S1 =250um

“Field” “Edge” “Corner”

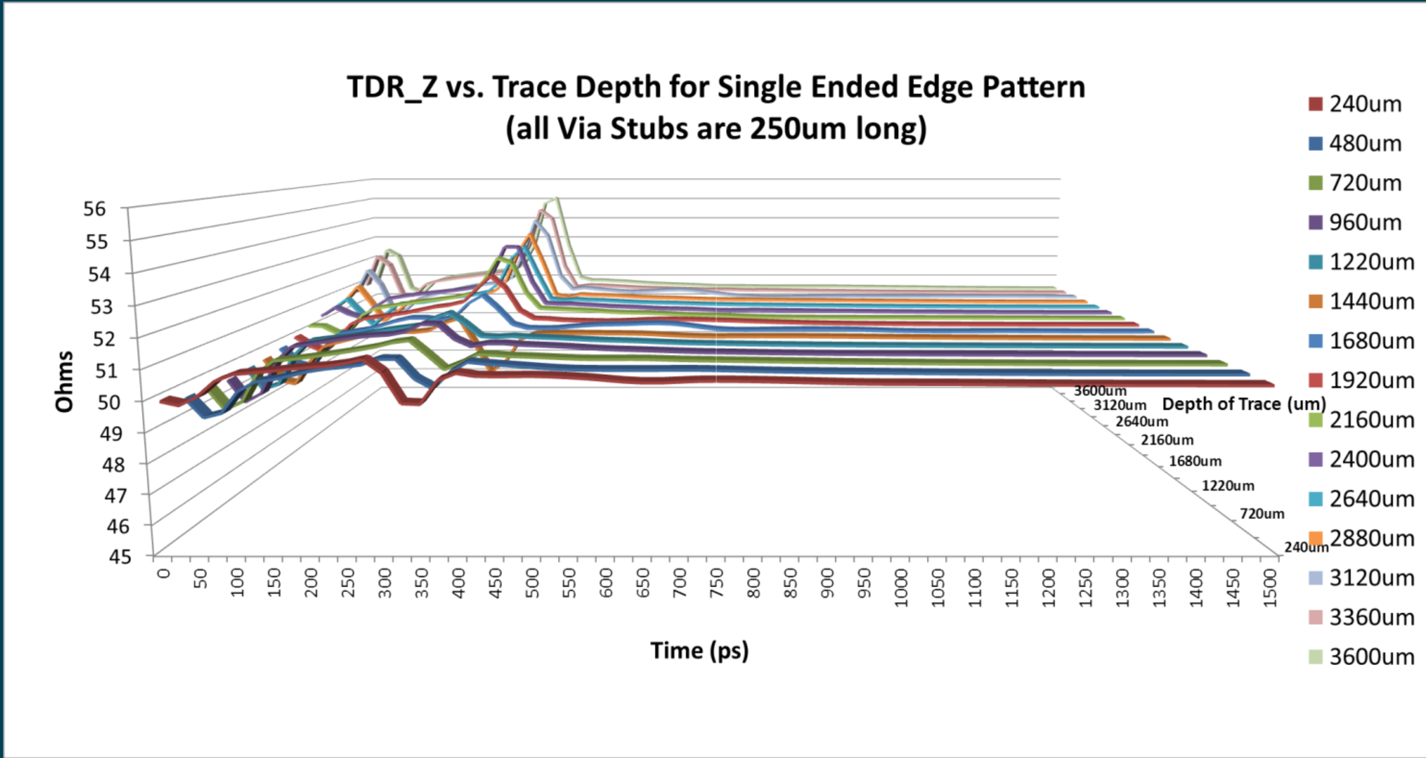


Gnd Clearance Dia. 600um - Red

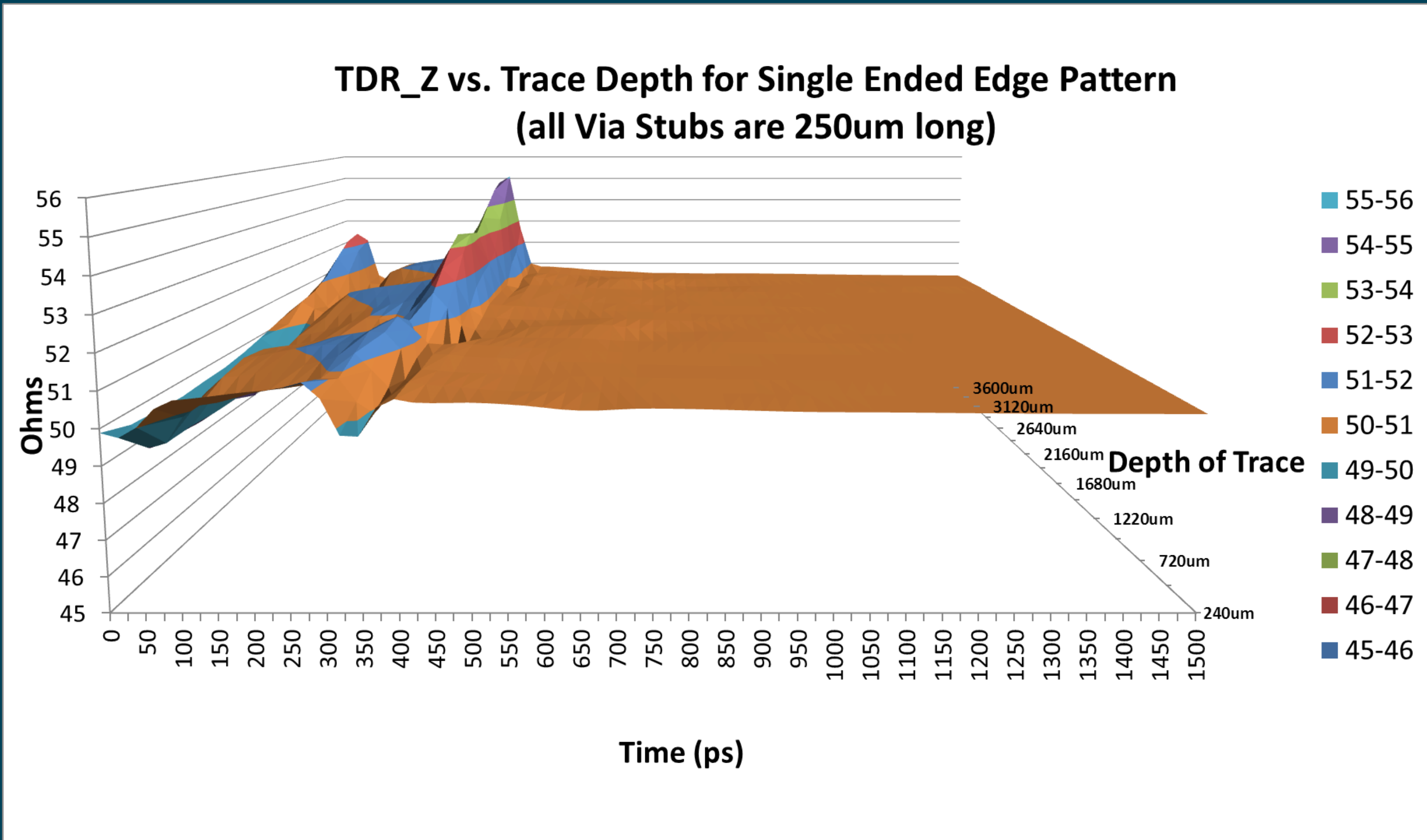
350um pitch via pattern

TDR_Z from simulations with higher Sweep frequency

Showing the effects of Trace Depth on TDR_Z

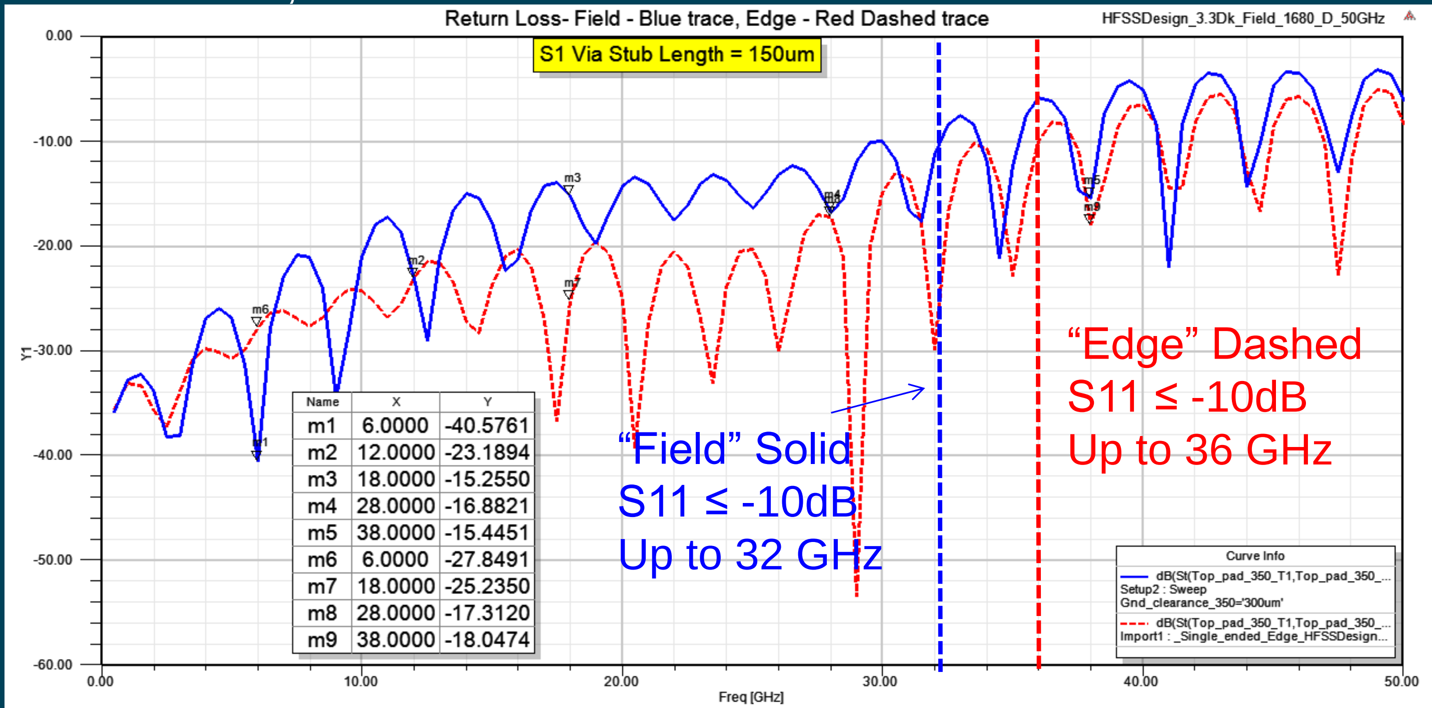


Showing the effects of Trace Depth on TDR_Z



Best Case – Compare "Field" and "Edge" Trace Depth – D1=1680um

"Field" and "Edge"
D1 = 1680um, S1 = 150um.



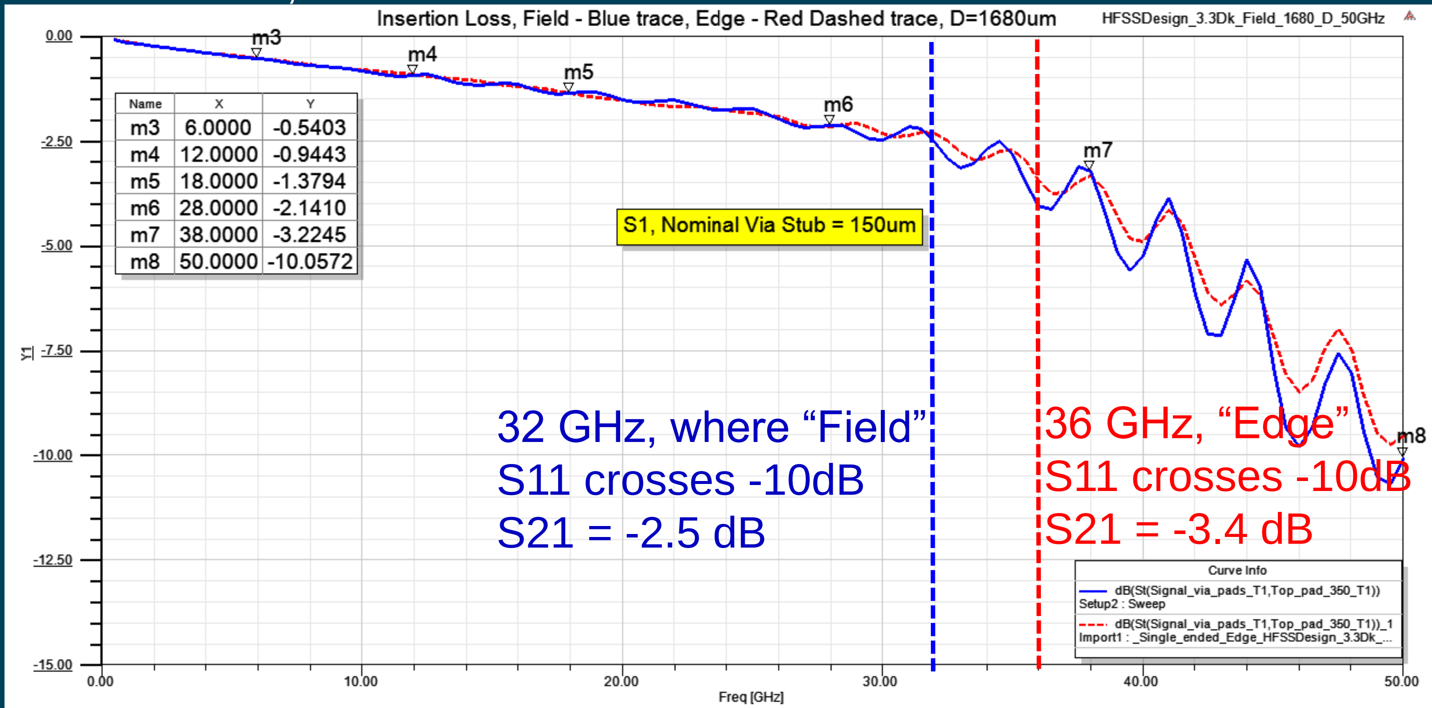
Name	X	Y
m1	6.0000	-40.5761
m2	12.0000	-23.1894
m3	18.0000	-15.2550
m4	28.0000	-16.8821
m5	38.0000	-15.4451
m6	6.0000	-27.8491
m7	18.0000	-25.2350
m8	28.0000	-17.3120
m9	38.0000	-18.0474

Increase Frequency Sweep– 50GHz

Best Case – Compare “Field” and “Edge” Trace Depth – D1=1680um

“Field” and “Edge”

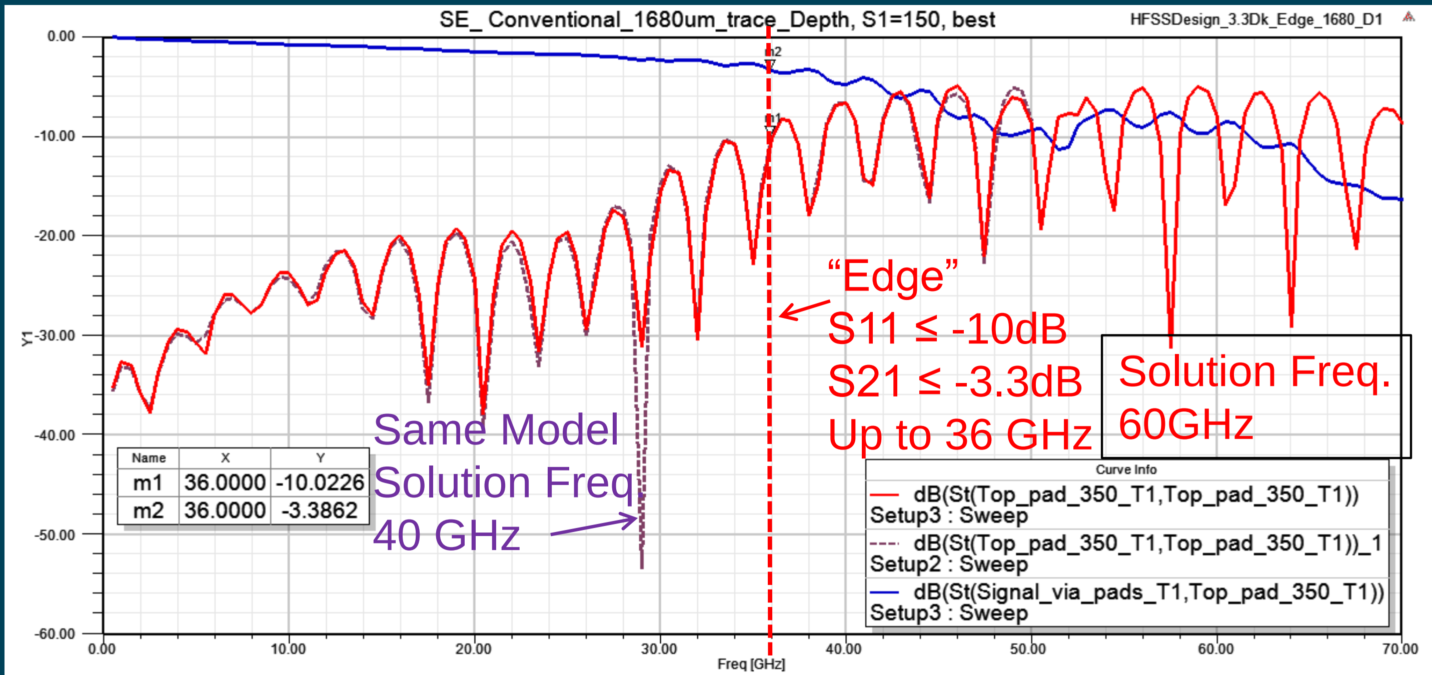
D1 = 1680um, S1 = 150um.



Increase Frequency Sweep– 50GHz

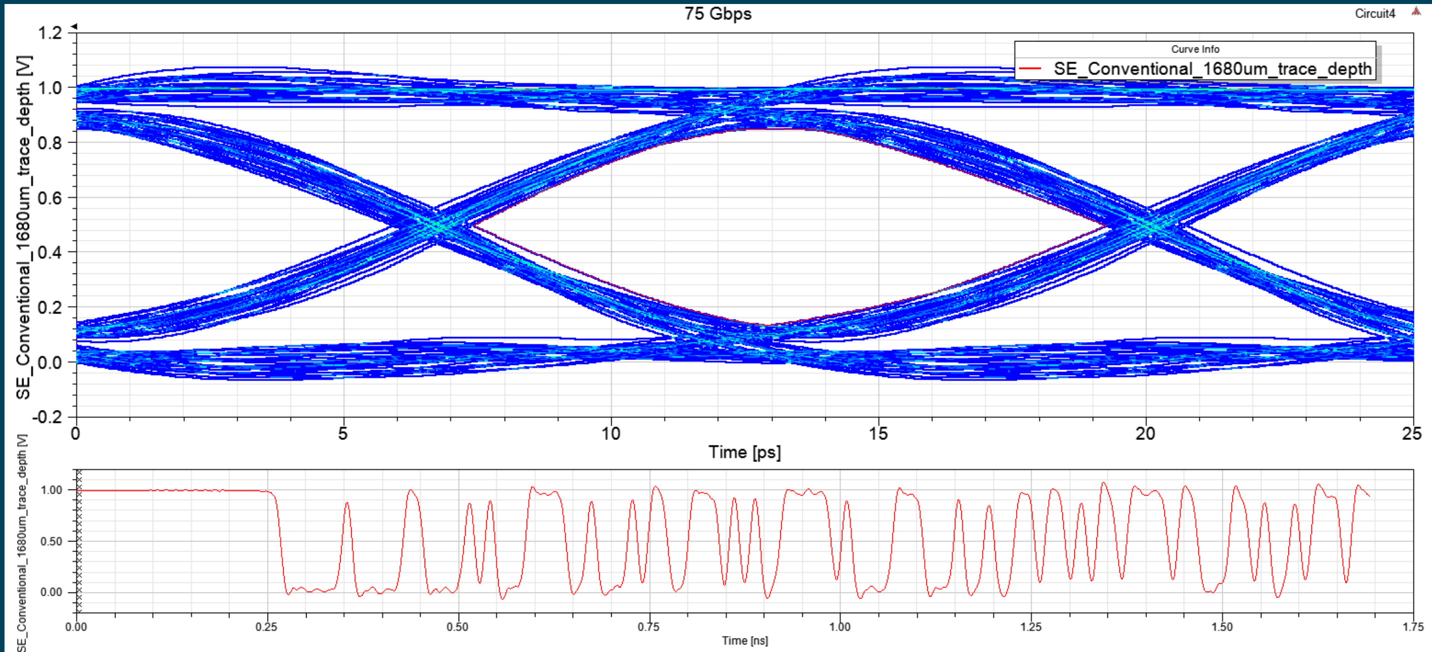
Best "Edge" - Increase Sweep to 70 GHz Trace Depth – D1=1680um

"Edge"
D1 = 1680um, S1 = 150um.



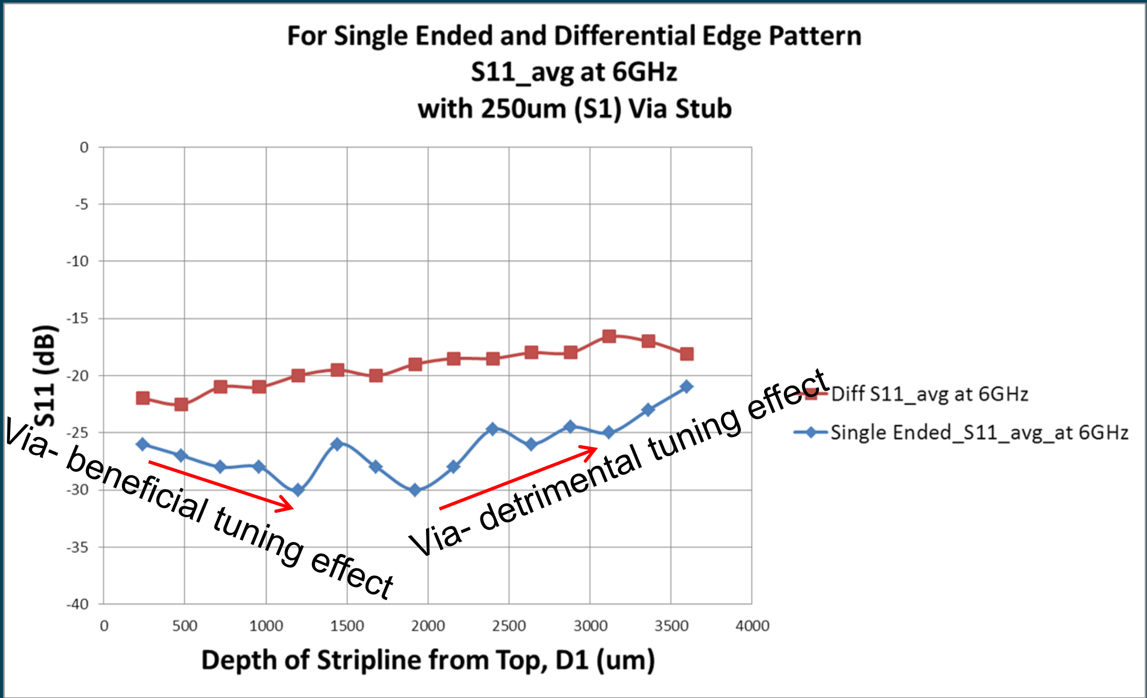
Increase Frequency Sweep– 70GHz

Best "Edge", Trace Depth – D1=1680um
PRBS7 Eye Diagram at 75Gbps



Trace Depth or Signal Via Length– Summary

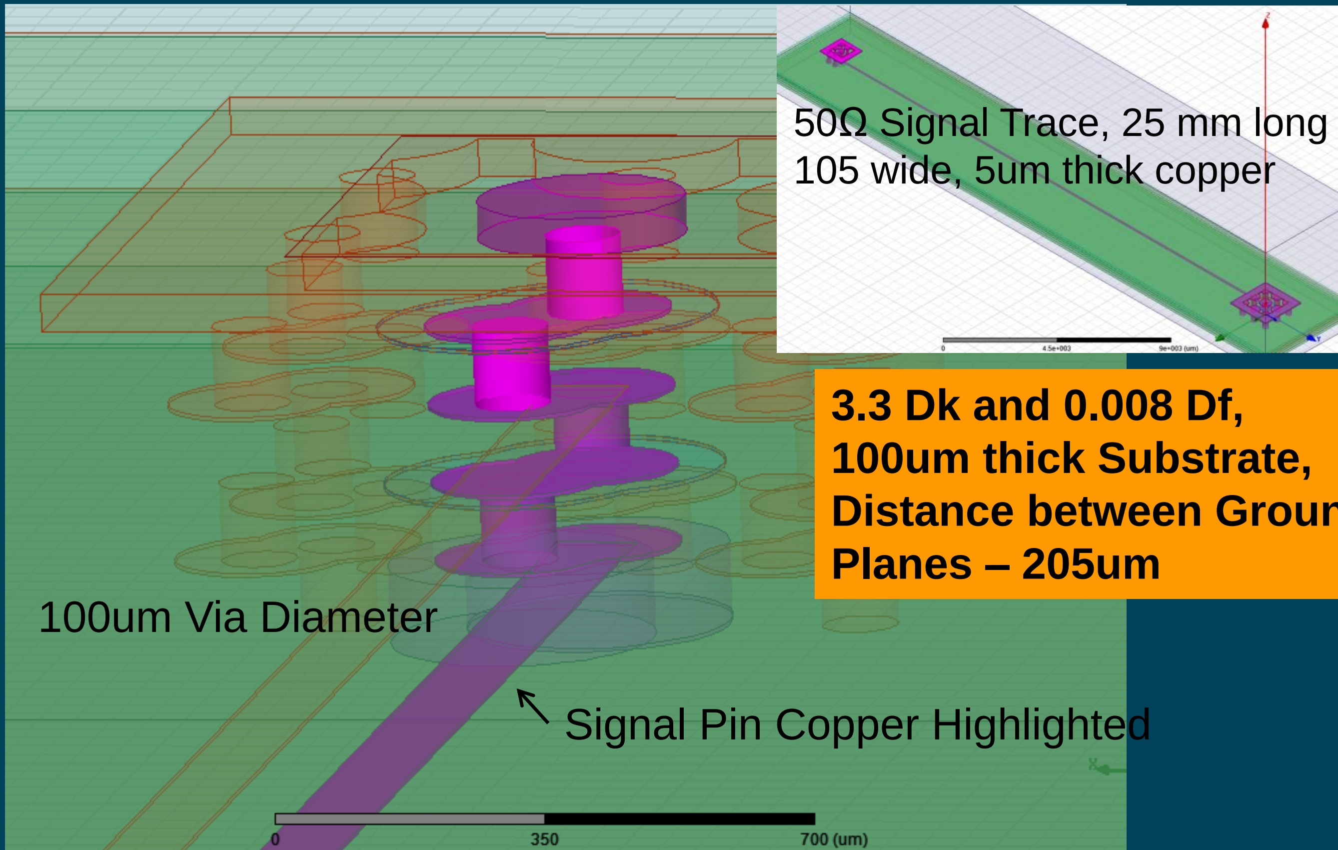
- The smaller the Depth of the Trace, D1, generally improves S11.
  - However, starting at the 240um depth trace, there is a steady improvement in S11 until 1680um depth.



Build-Up Technologies

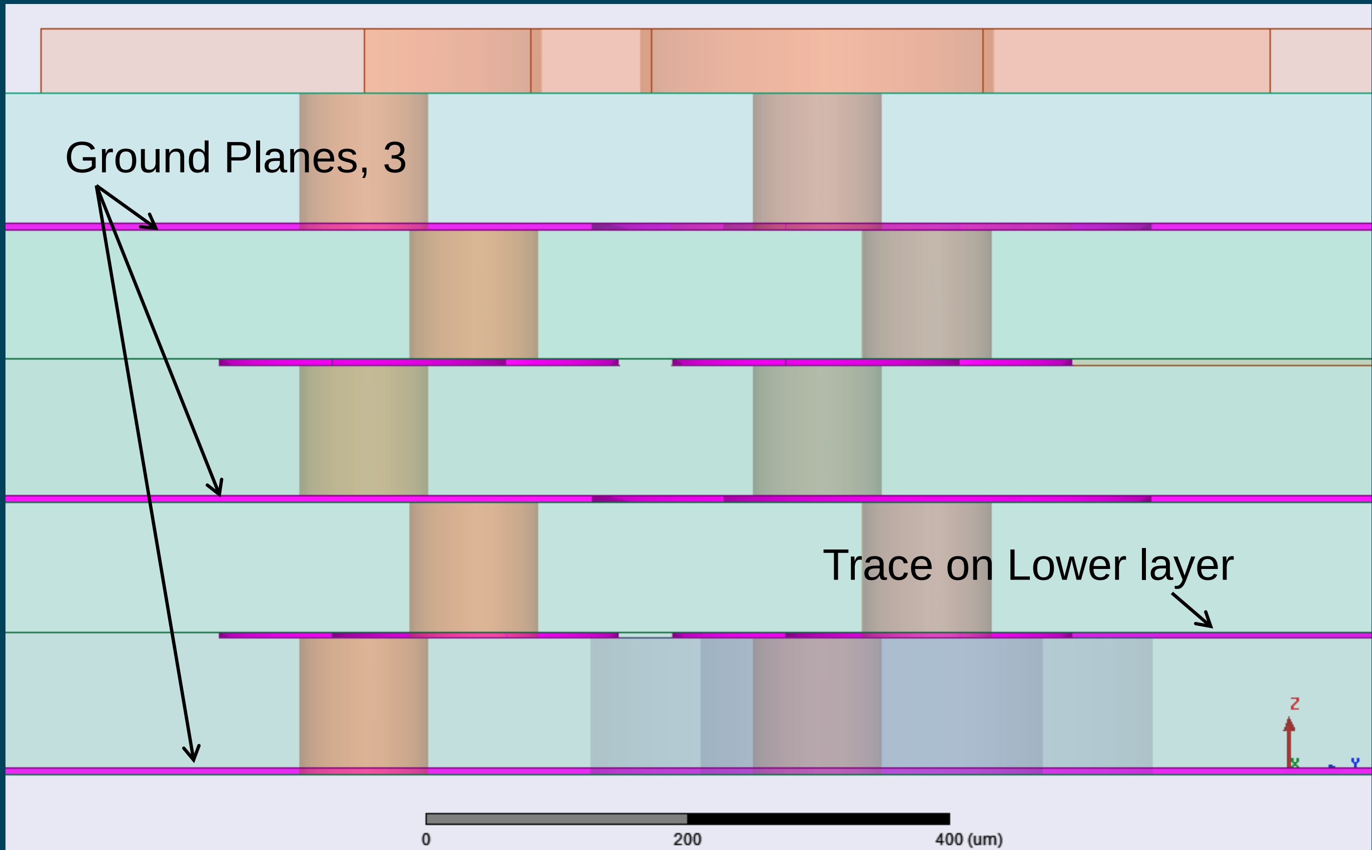
- Build-Up Technologies
  1. Use of Spun Dielectrics (= homogeneous material)
  2. Stubless Vias
  3. Padless Vias
  - Traditional Staggered (Offset vias) pads on every layer
  - Traditional Aligned vias, pads on every layer
  - Damascene, Padless vias, deposition then planarization after every layer

Traditional Build-Up, Two Layers Down, Edge Pattern, Staggered Vias

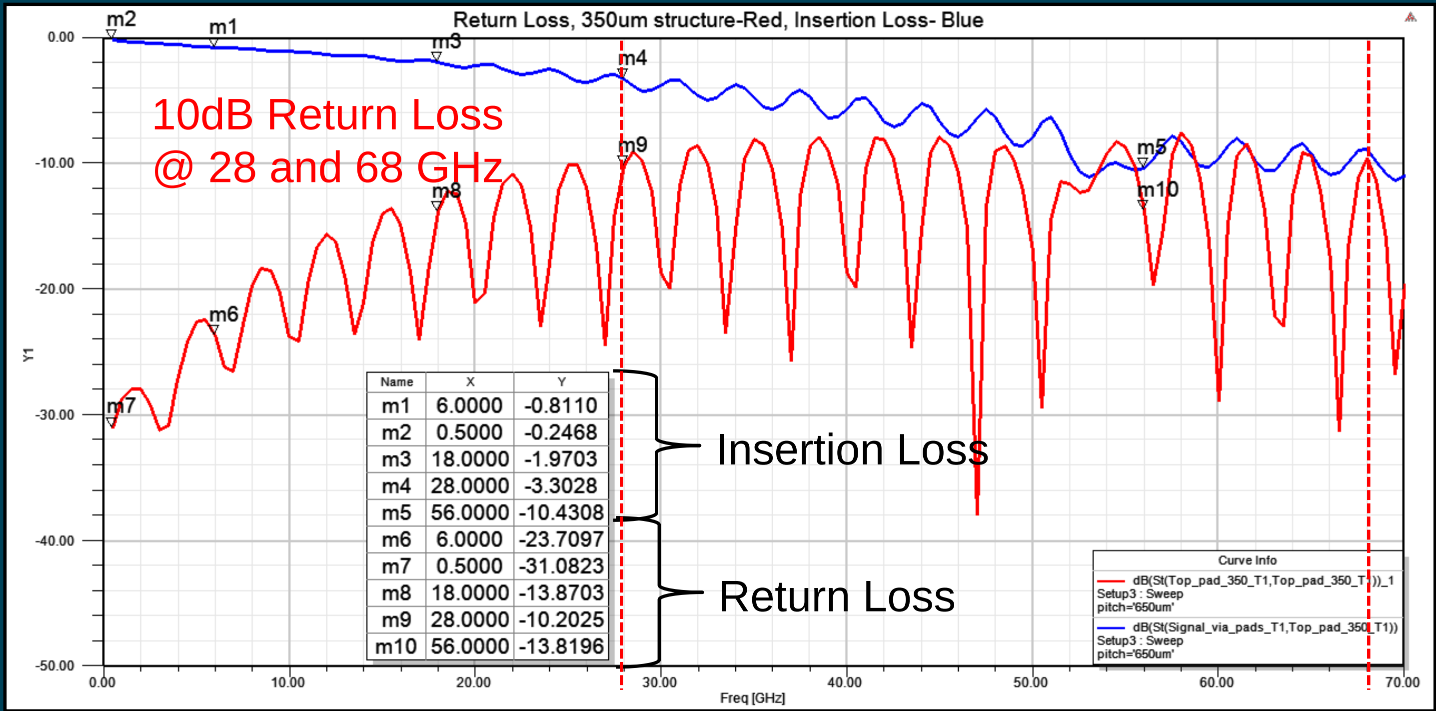


3.3 Dk and 0.008 Df, 100um thick Substrate, Distance between Ground Planes – 205um

Traditional Build-Up, Two Layers Down, Edge Pattern, Staggered Vias



Traditional Build-Up, Two Layers Down, Edge Pattern, Staggered Vias

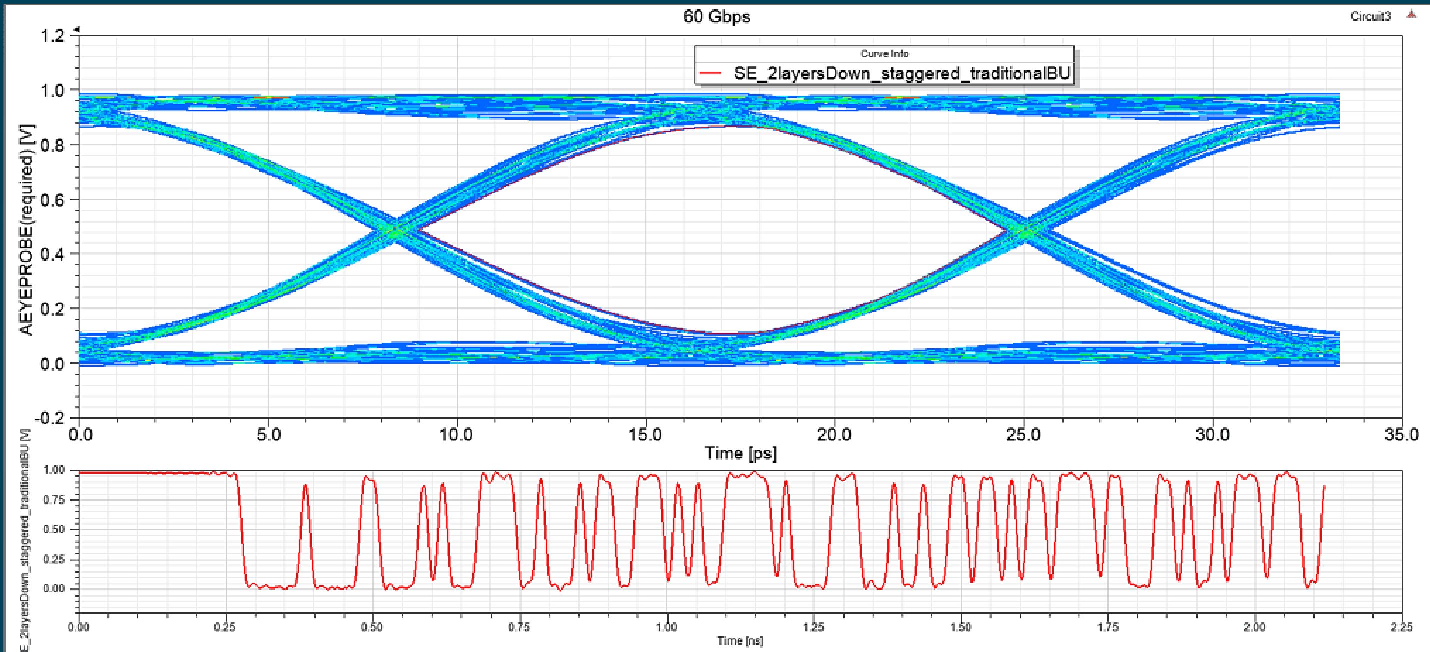


Name	X	Y
m1	6.0000	-0.8110
m2	0.5000	-0.2468
m3	18.0000	-1.9703
m4	28.0000	-3.3028
m5	56.0000	-10.4308
m6	6.0000	-23.7097
m7	0.5000	-31.0823
m8	18.0000	-13.8703
m9	28.0000	-10.2025
m10	56.0000	-13.8196

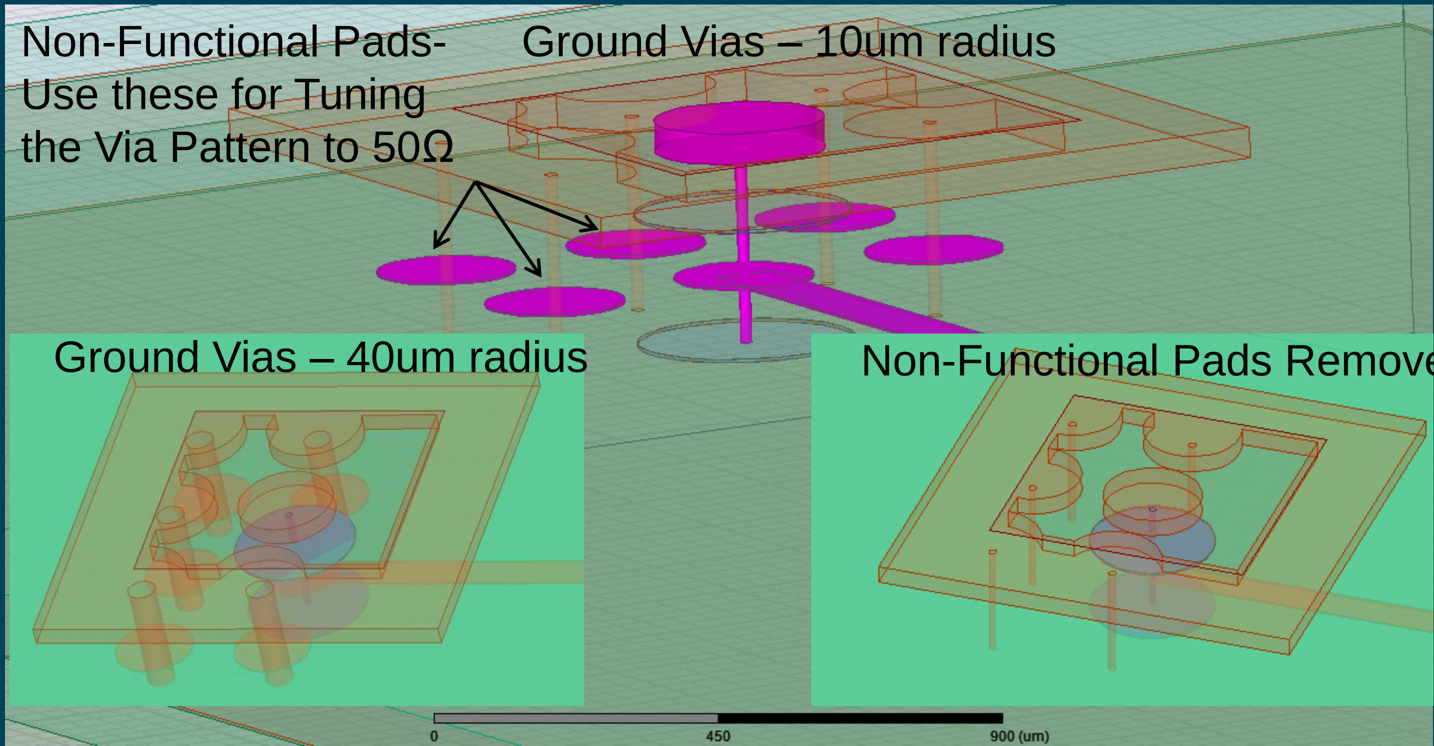
Increase Frequency Sweep– 70GHz

Traditional Build-Up, Two Layers Down, Edge Pattern, Staggered Vias

60 Gbps PRBS7 Eye Diagram

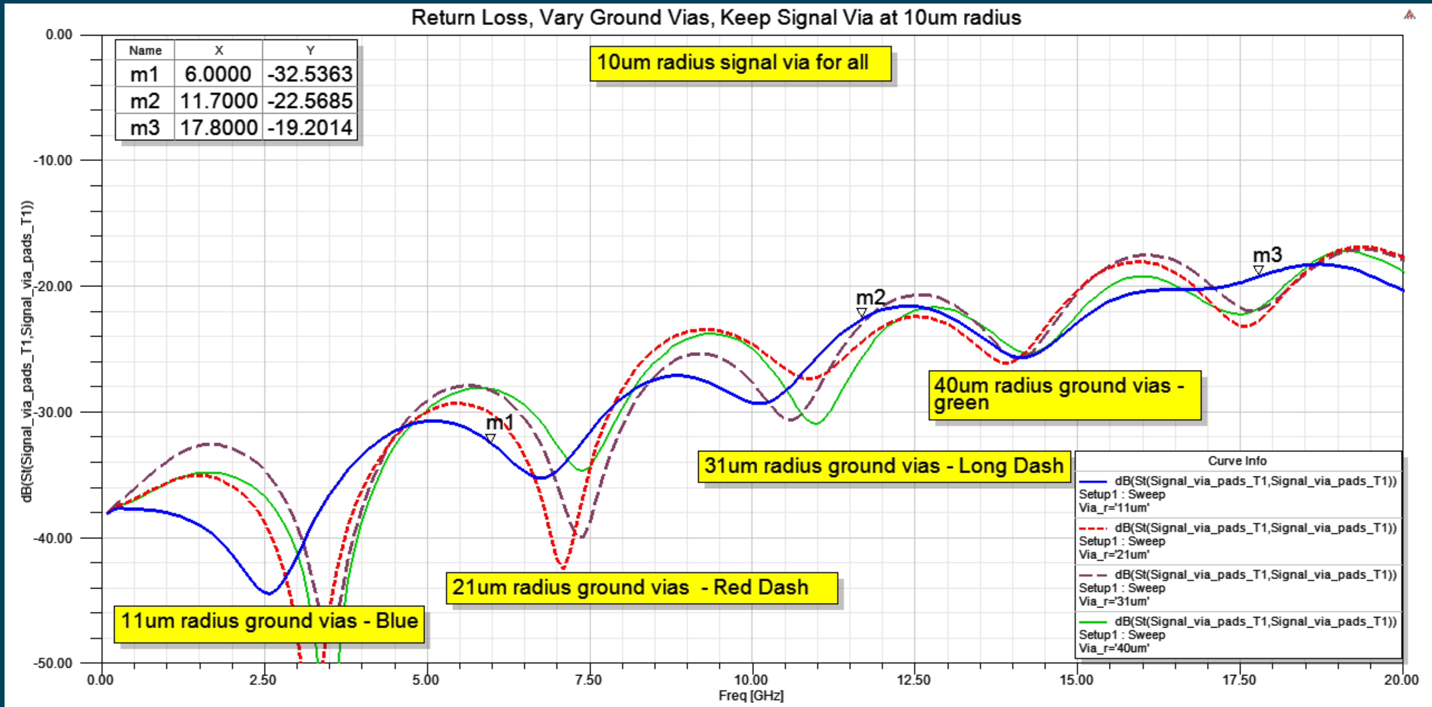


Damascene Process, 1 Layer Down, Different Vias Diameters, down to 20um



Damascene Process, 1 Layer Down, Sweep Vias Diameters, 22um to 80um

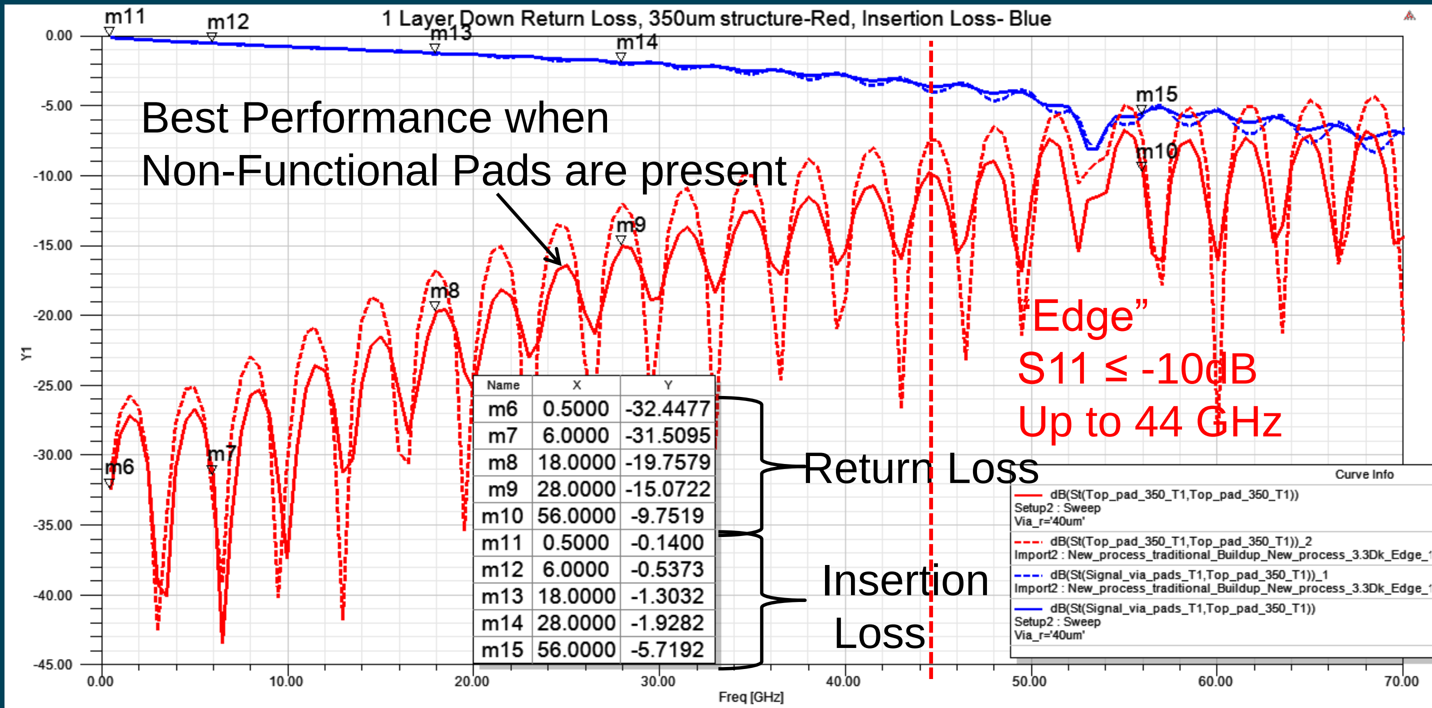
with non-functional pads



Choose Signal Via Dia. 20um & Gnd Vias Dia. 80um for higher Freq. Sweep

Damascene Process, 1 Layer Down,
Signal Via – 20um, Gnd Vias – Diameter 80um

Non-functional pads- With (solid) and without (dashed)

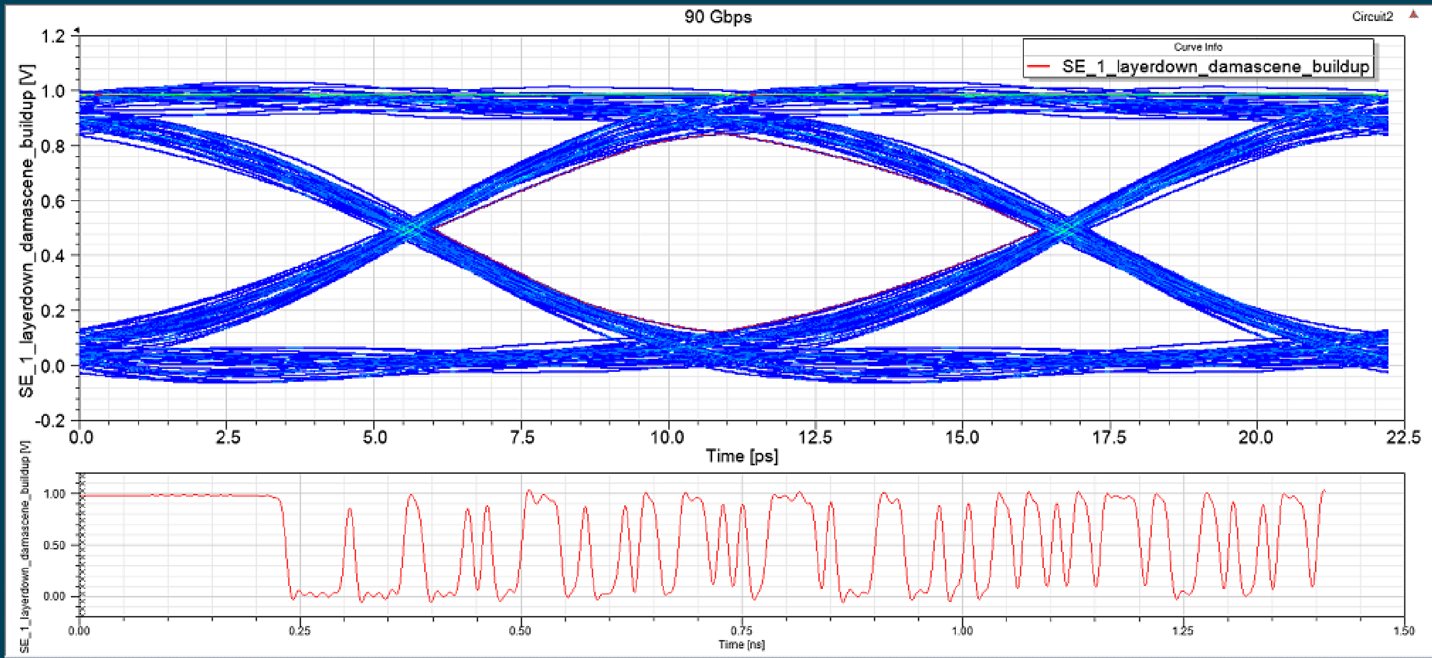


Name	X	Y
m6	0.5000	-32.4477
m7	6.0000	-31.5095
m8	18.0000	-19.7579
m9	28.0000	-15.0722
m10	56.0000	-9.7519
m11	0.5000	-0.1400
m12	6.0000	-0.5373
m13	18.0000	-1.3032
m14	28.0000	-1.9282
m15	56.0000	-5.7192

Increase Frequency Sweep– 70GHz

Damascene Process, 1 Layer Down, Signal Via – 20um, Gnd Vias – Diameter 80um

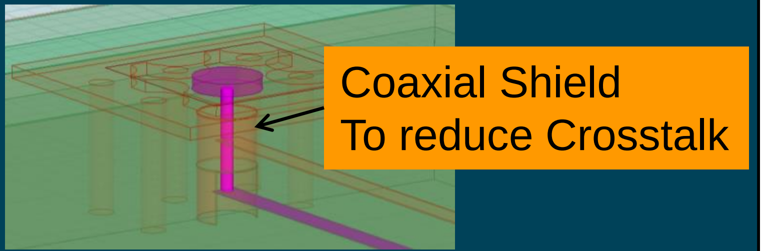
90 Gbps PRBS7 Eye Diagram



With the Non-functional pads

Conclusion

- **Highest Frequency of Use- Based on Return Loss of 10dB**
  - 36 GHz (75 Gbps Eye Diag.) - Conventional Fine Pitch, Edge Pattern, 1680um deep trace, Heterogeneous material
  - 28 GHz (60 Gbps Eye Diag.) - Traditional Build-Up, Two Layers Down, Edge Pattern, Staggered Vias, Homogeneous material
  - 44 GHz (90 Gbps Eye Diag.) - Damascene, One Layers Down, Edge Pattern, Optimize Vias and Non-Functional Pads, Homogeneous
- **Continued Development**
  1. Vertical Transmission Lines
  2. Vias down to 10um
  3. +/-1um tolerance for “W”
  4. +/-2um tolerance for “H”: *We are currently averaging better than +/-0.2um.*



Acknowledgements

- **Phil Warwick**, of R & D Altanova, for developing the study and providing technical and industry expertise.

- **Sandeep Sankararaman,** of R & D Altanova, for taking my S-parameter files and running the Eye Diagram Analysis in HFSS Electronics Desktop.