
EIGHTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 5 - 8, 2017
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Market Session
© 2017 BiTS Workshop – Image: tonda / iStock

Copyright Notice

Market Session

BiTS Workshop 2017 Schedule

Tutorial Day

Sunday March 5 - 8:30 pm

Marketplace Report

Ira Feldman

Feldman Engineering Corp.

Market Connections – Semiconductors to Sockets

John West

Managing Director

VLSI Research Europe

BiTS 2017 Burn-in & Test Strategies Workshop

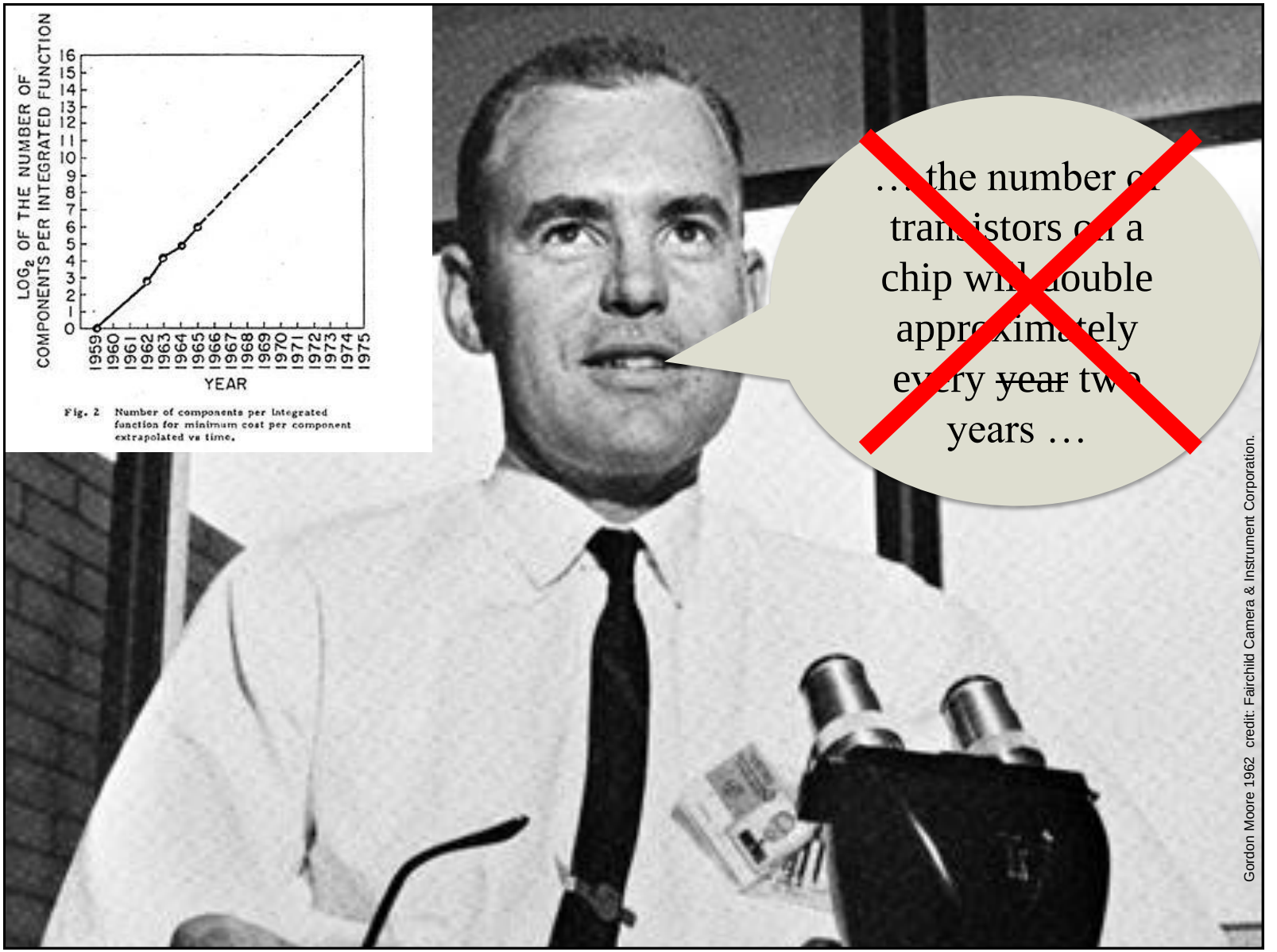
Marketplace Report

Ira Feldman
Feldman Engineering Corp.

BiTS Workshop
March 5 - 8, 2017

Outline

- Fundamentals
  - How did we get here?
- Test Today
- Integrated “Ecosystems”
- Socket Market Data


LOG2 OF THE NUMBER OF COMPONENTS PER INTEGRATED FUNCTION
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975
YEAR
Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.
… the number of transistors on a chip will double approximately every ~~year~~ two years …
Gordon Moore 1962 credit: Fairchild Camera & Instrument Corporation.

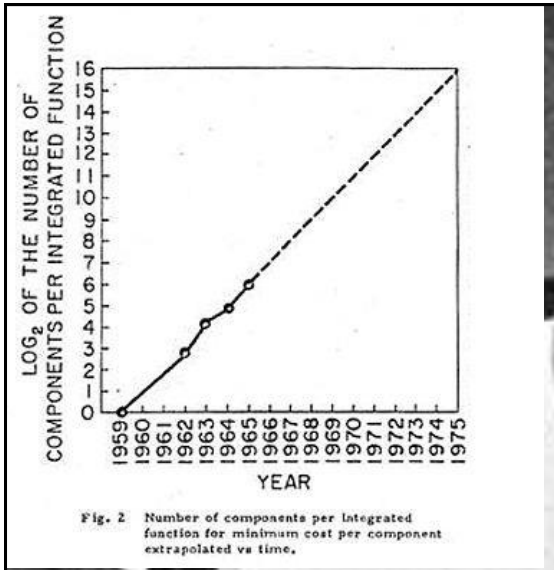


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

Minimum cost per transistor is achieved by doubling the number of transistors every two years.
Gordon Moore
1965*

* Revised in 1972 from every 12 to 24 months.

Gordon Moore 1962 credit: Fairchild Camera & Instrument Corporation.

Electronics, Volume 38, Number 8, April 19, 1965

The experts look ahead

Cramming more components onto integrated circuits

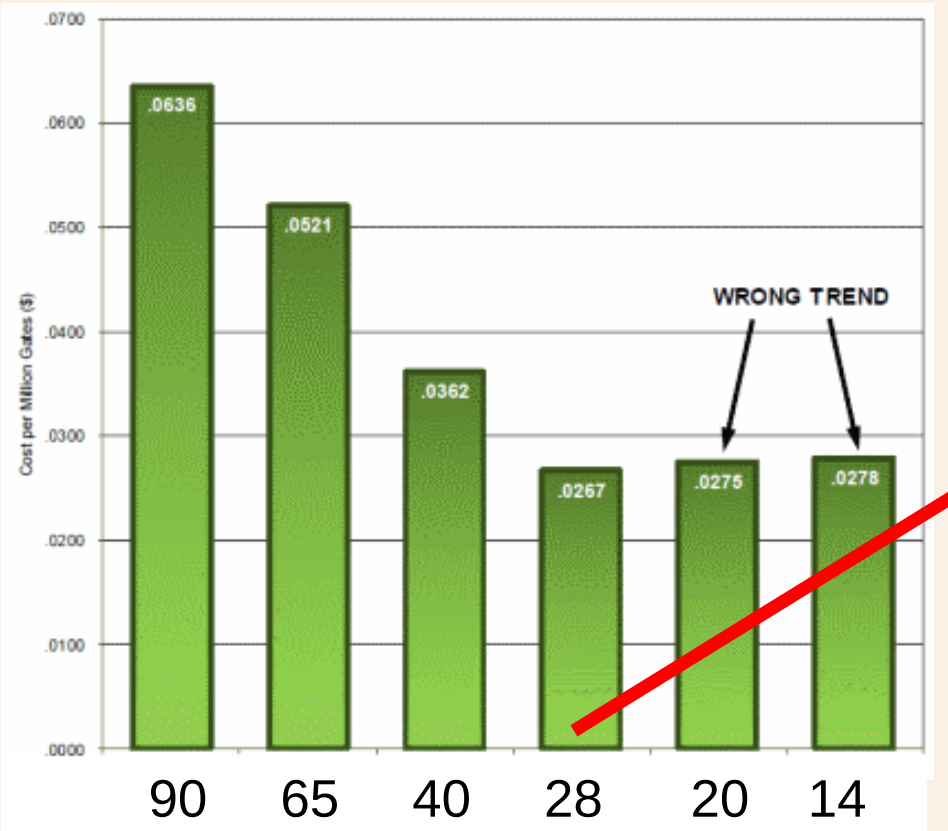
With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

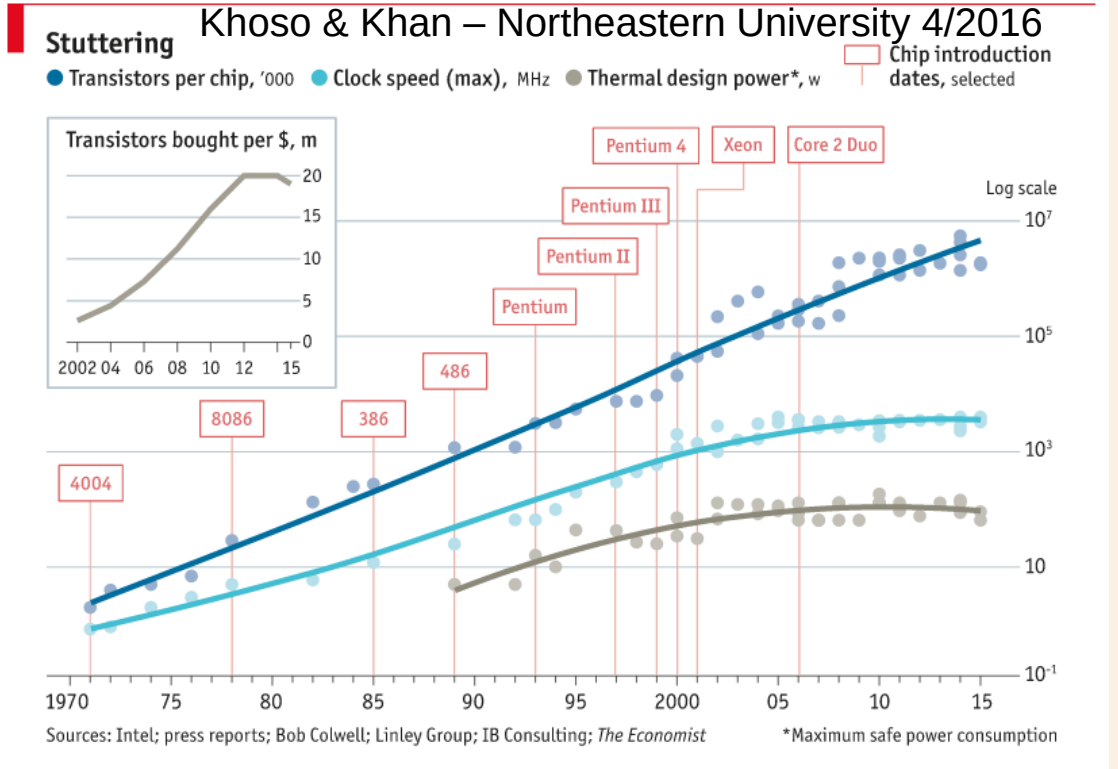
The complexity for minimum component costs has increased at a rate of roughly a factor of two per year (see graph on next page). Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000.

Moore's Law is "Dead"



Handel Jones, 2012
http://www.eetimes.com/author.asp?section_id=36&doc_id=1287737

Khoso & Khan – Northeastern University 4/2016



"Populist view: Any parameter related to semiconductors must form a straight line when plotted on exponential graph paper."

– Prof. Subramanian Iyer (UCLA, former IBM Fellow)

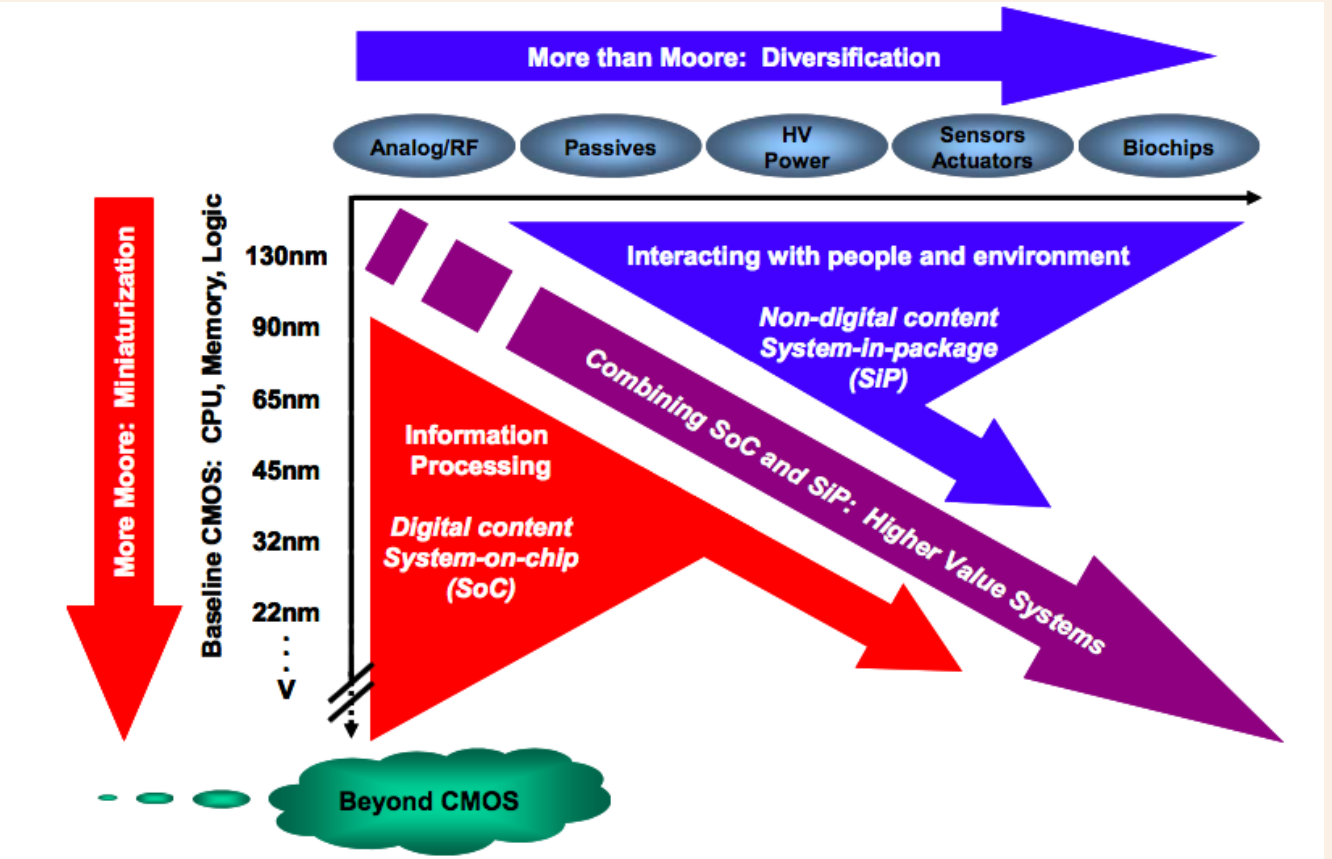
"Knobs" to reduce product cost

Transistor Scaling
Materials
Device Structure

Substrate Size
cost / area

More than Moore
Architecture
Packaging

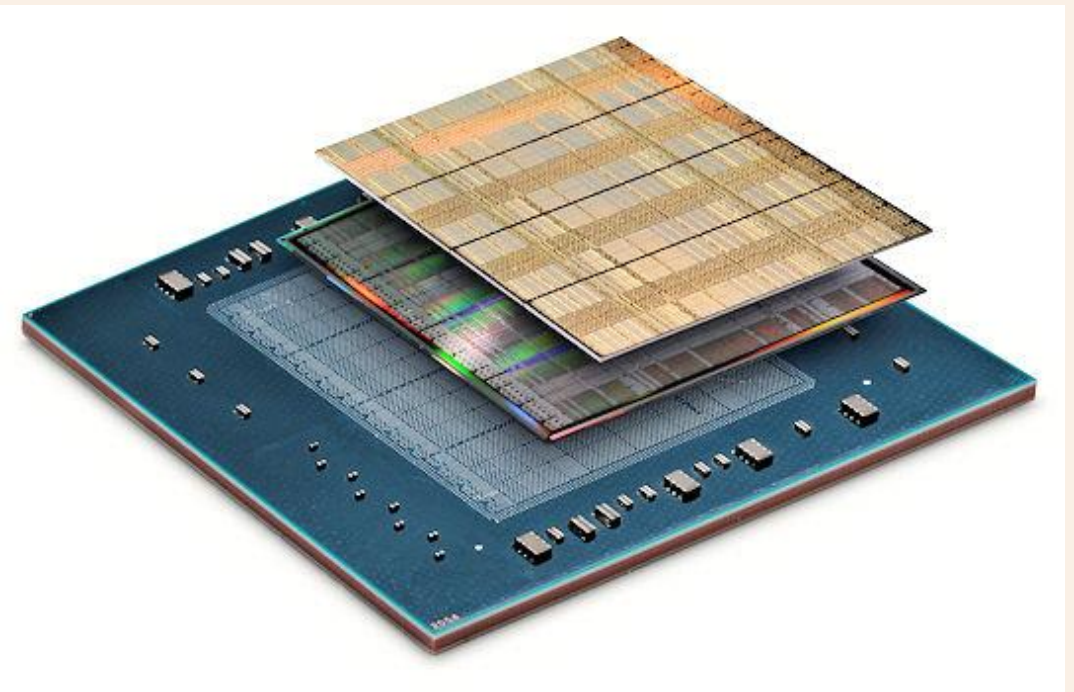
More than Moore (MtM)



ITRS "More than Moore" Whitepaper

MtM System in Package (SiP)

2.5D/3D/5.5D Packaging – First to Market



Xilinx Virtex-7 FPGA (Oct ’11)

High Performance SiP

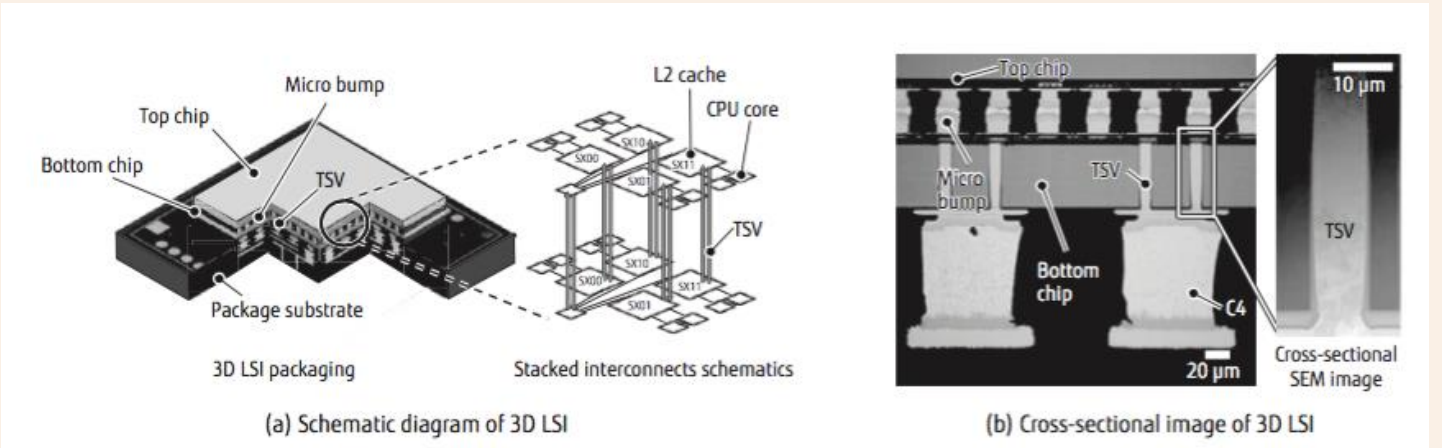
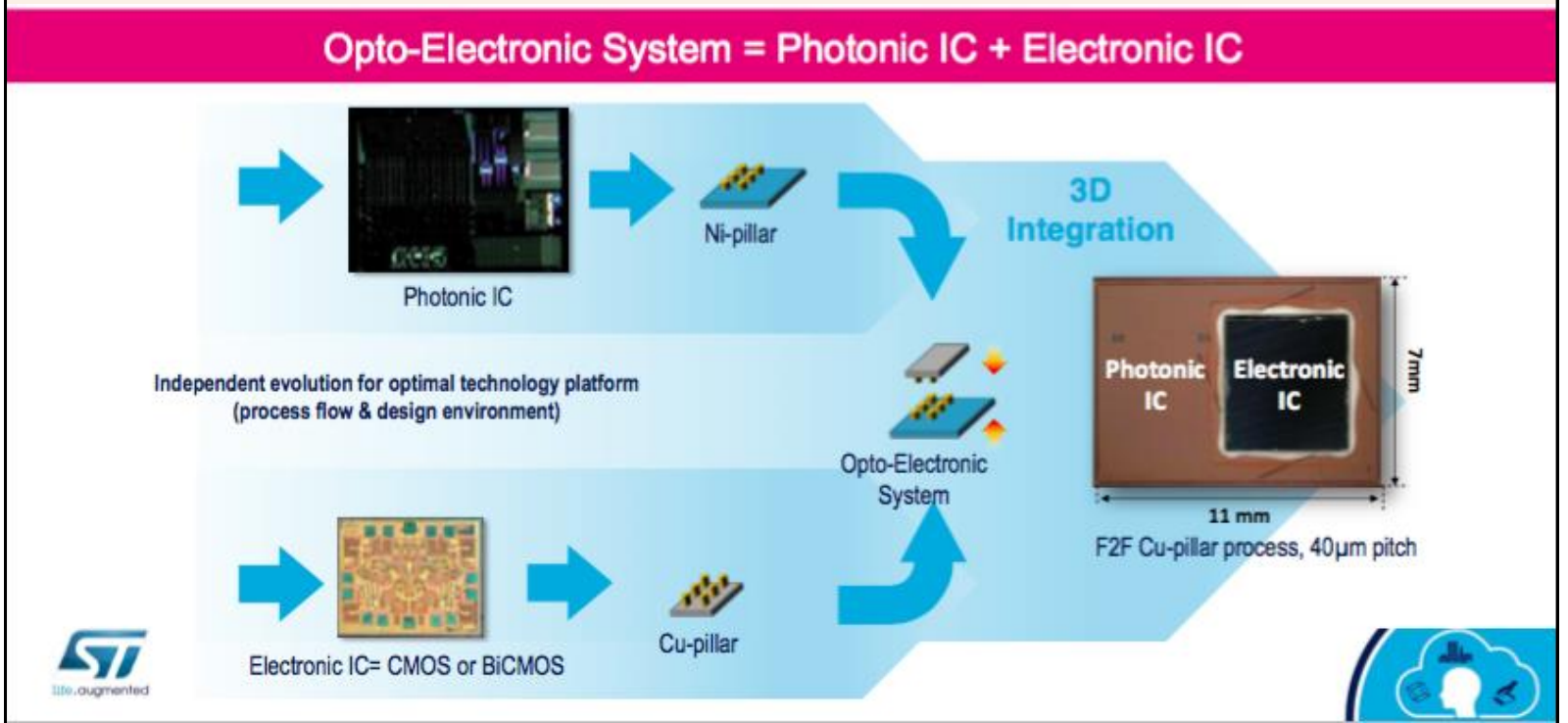


Table 1
Element technology items for 3D LSI and comparison of conventional technology and development target.

Element technology items	Conventional technology	Development target
TSV backside process	>300 µm: 23 mm square chip	<100 µm: 23 mm square chip
C4 bump tolerable current	25 mA	>100 mA
Micro bump material	<10 mA/bump: SnAgmaterial	>50 mA/bump: Intermetallic compounds junctions
Stacked die area	100 mm^2	>500 mm^2
Number of micro bumps	150,000	300,000
TSV transmission performance	20 GHz	40 GHz

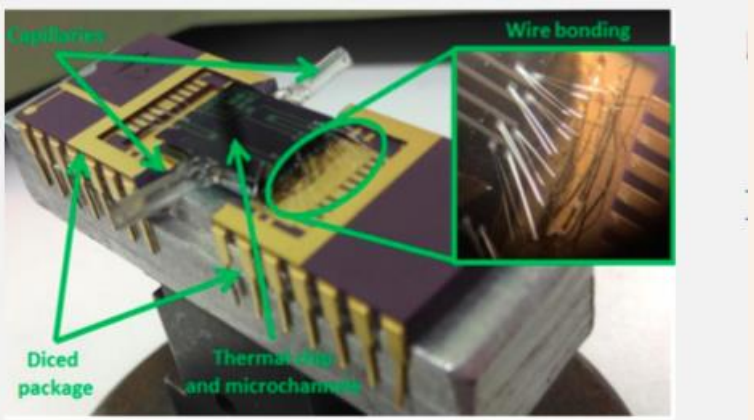
Kitada, et. al / Fujitsu – February 2017

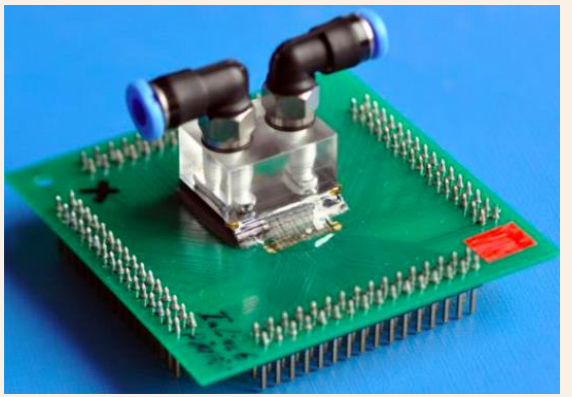
Silicon Photonics

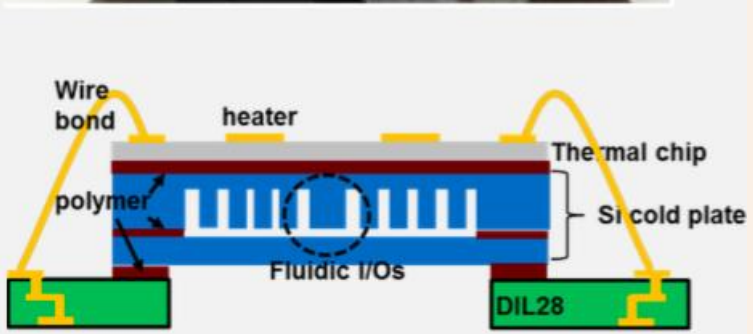


ST 100G PSM4 QSFP 28 (STsP10028) October 2016

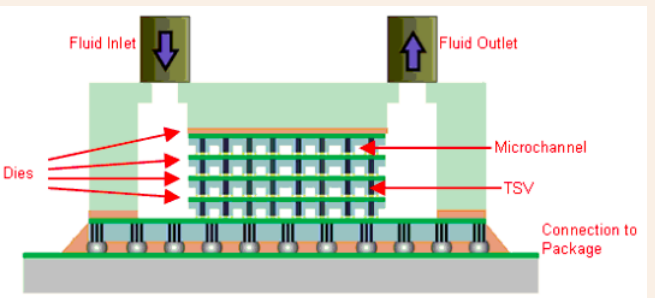
Microfluidics







Fréchette - Université de Sherbrooke

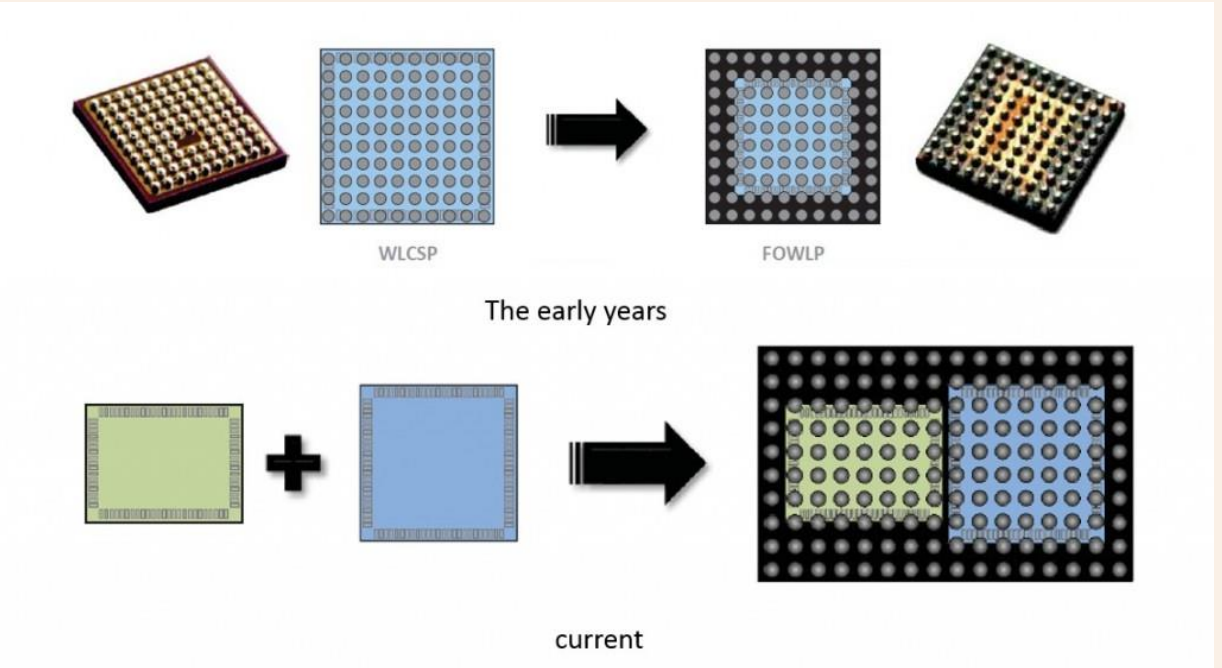


Zapater - École Polytechnique Fédérale de Lausanne (EPFL)

SEMI European 3D Summit – January 2017

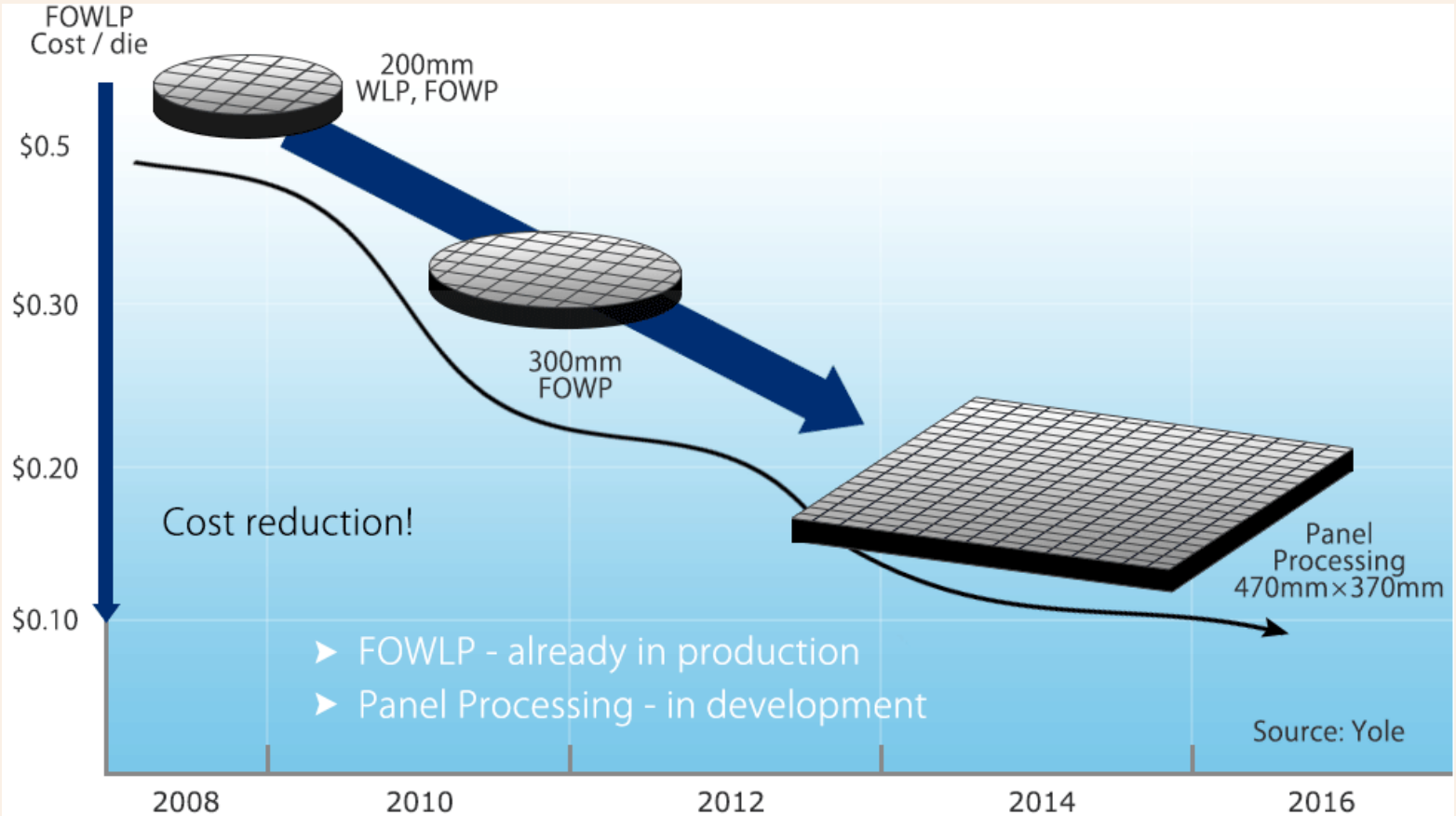
MtM System in Package (SiP)

Fan Out Wafer Level Packaging



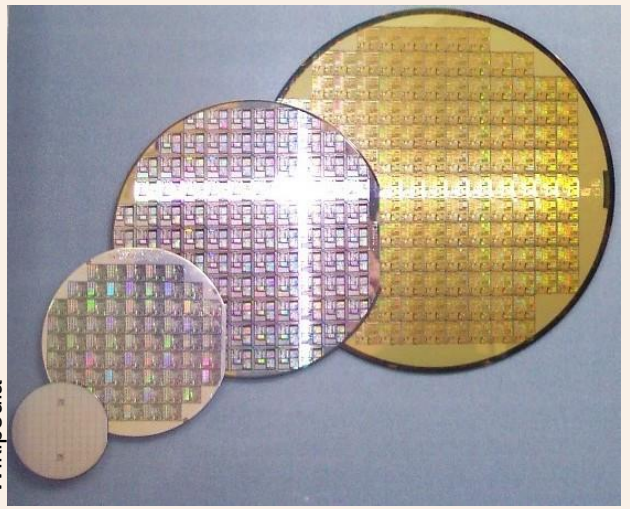
ASE / IFTLE 295 - Phil Garrou – July 2016

Transition to FO-PLP



Historical Test Approach

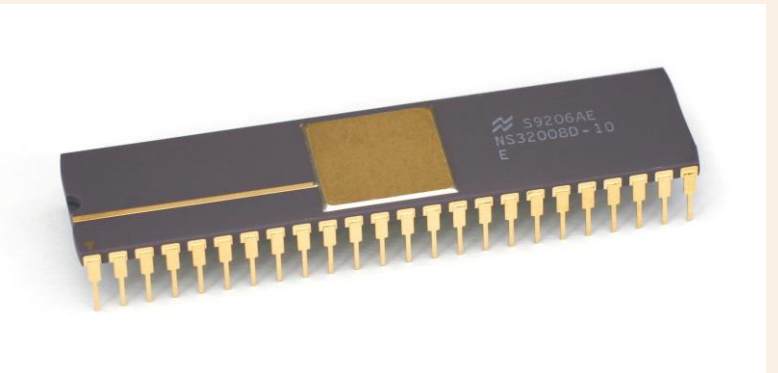
Wafer Sort



Wikipedia

Is it good enough to package?

Final Test



Wikipedia

Does it meet specification?

↓

Can I sell it for more?
Higher performance bin

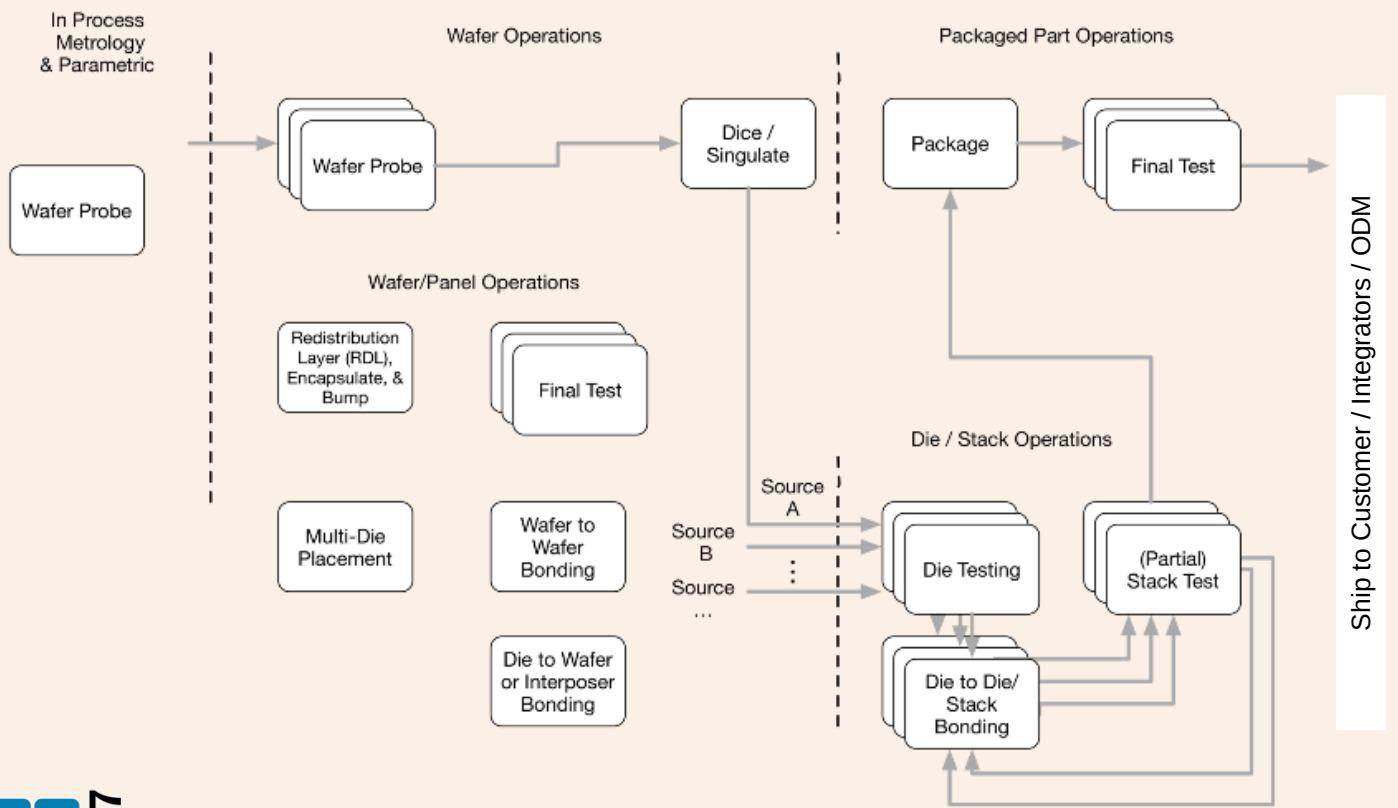
Paradigm Shift – Value Creation

- Yield Management
  - Process Improvement Feedback
  - Die “matching”
- Repair
  - Switch off defective “cores”
  - Swapping in spares (memory, etc.)
- Performance Tuning
  - Calibration
- Personalization
  - Serialization
  - Security & Keys

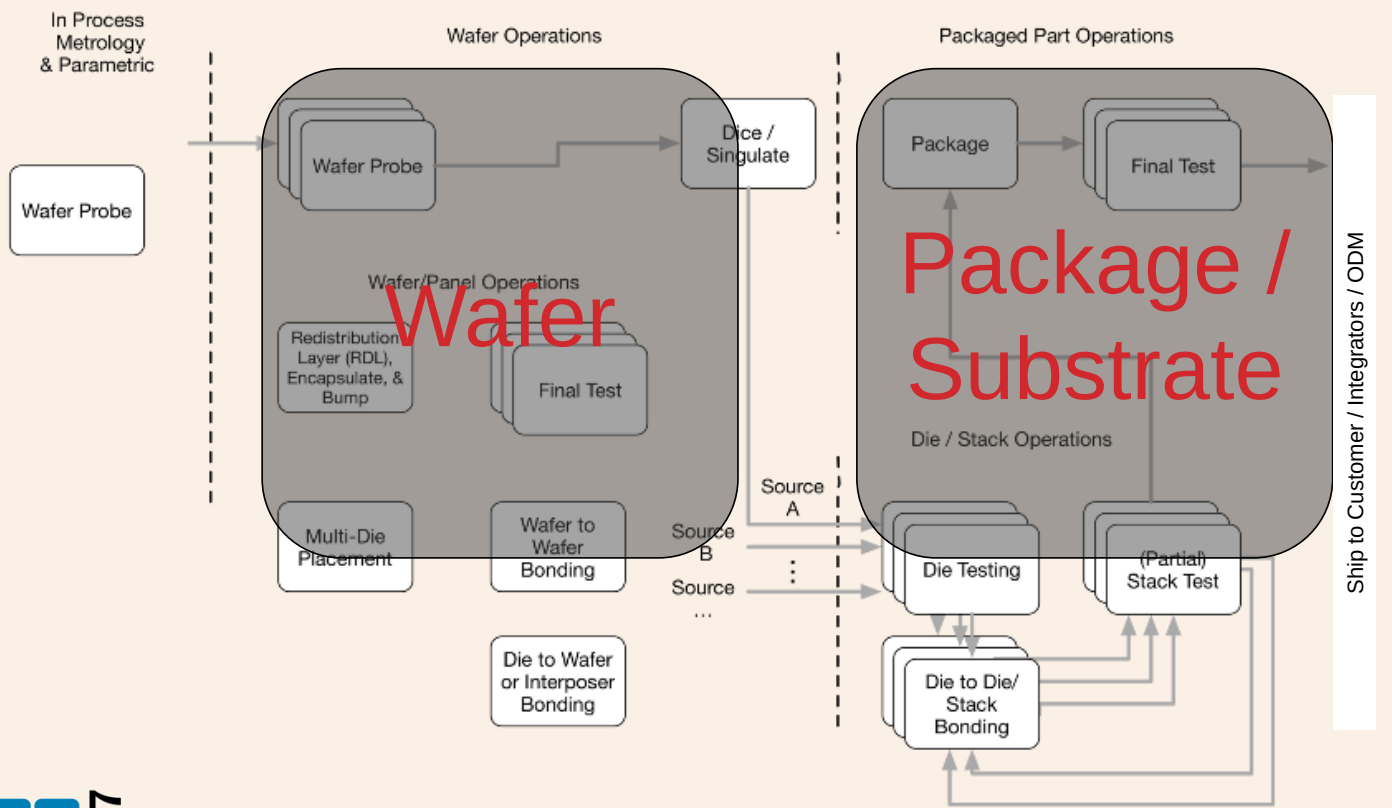
Plus much more …

Test Today

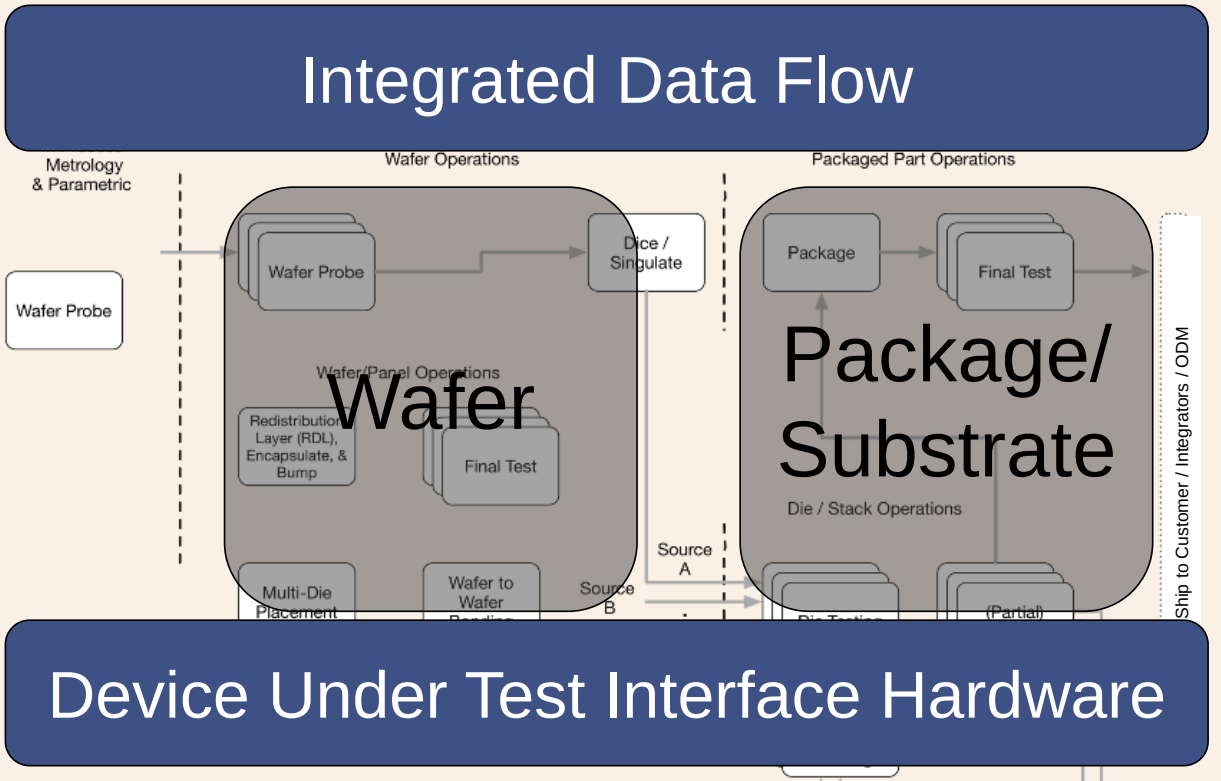
Typical 2.5/3D Heterogeneous Integration Flow



Test Today

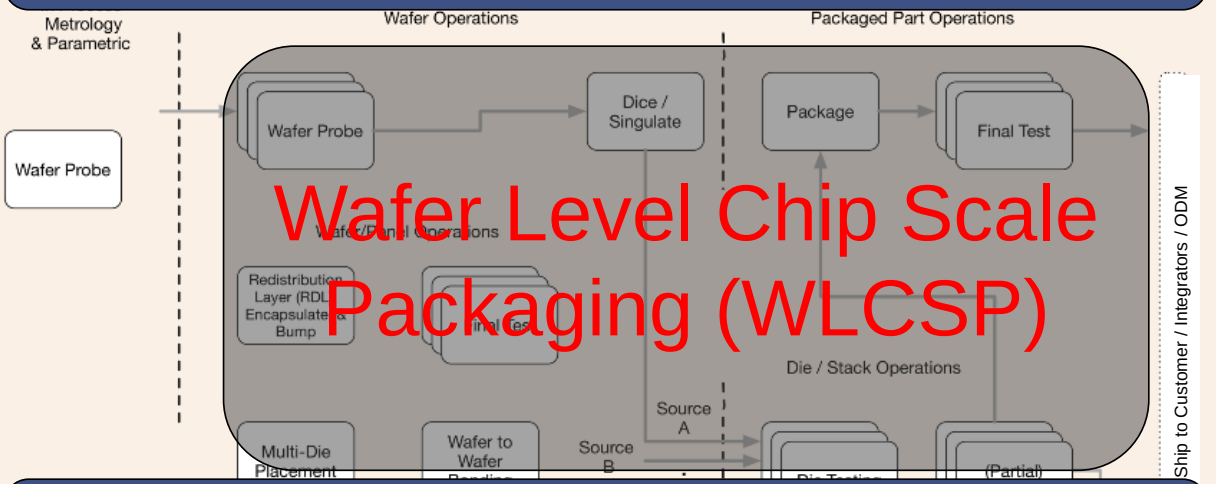

In Process Metrology & Parametric
Wafer Probe
Wafer Operations
Wafer Probe
Dice / Singulate
Wafer/Panel Operations
Redistribution Layer (RDL), Encapsulate, & Bump
Final Test
Wafer
Multi-Die Placement
Wafer to Wafer Bonding
Die to Wafer or Interposer Bonding
Source A
Source B
Source
...
Packaged Part Operations
Package
Final Test
Package / Substrate
Die / Stack Operations
Die Testing
(Partial) Stack Test
Die to Die/ Stack Bonding
Ship to Customer / Integrators / ODM

Test "Convergence"



Simplest Example

Integrated Data Flow



Wafer Level Chip Scale Packaging (WLCSP)

Device Under Test Interface Hardware

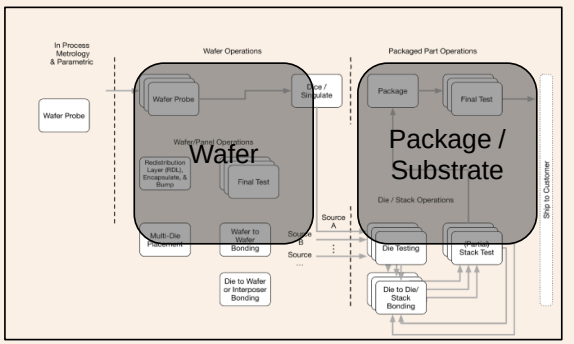
Test Strategy + Hardware + Software

Die / Package Activities

Ramp

Characterization

Validation



Failure Analysis

Reliability

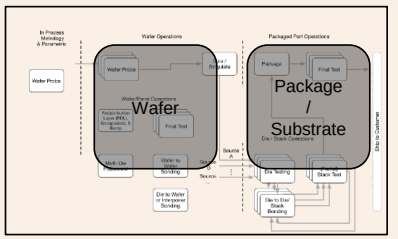
Future Environment

Integrated Data Flow

Ramp

Characterization

Validation



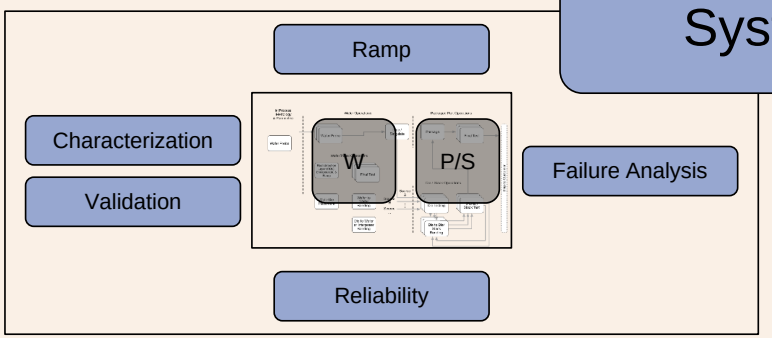
Failure Analysis

Reliability

Device Under Test Interface Hardware

Test Strategy + Hardware + Software

Adjacent "Test Markets"



System Level Test

Module Level Test

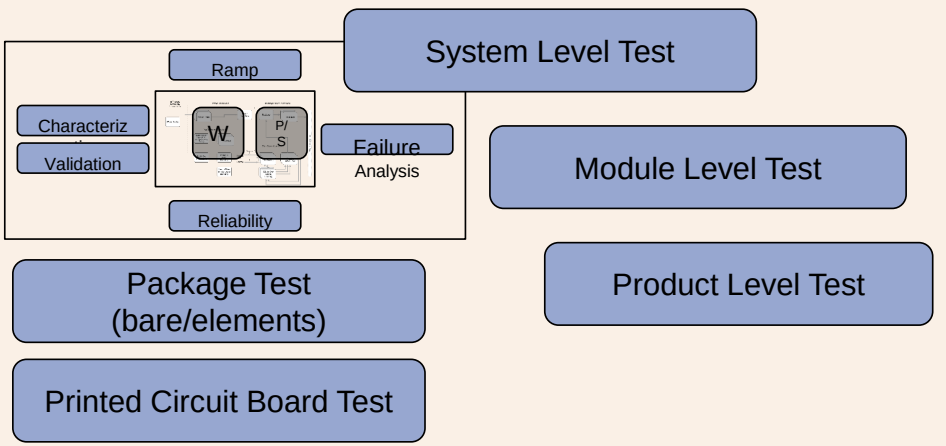
Product Level Test

Package Test (bare/elements)

Printed Circuit Board Test

Integrated Ecosystem?

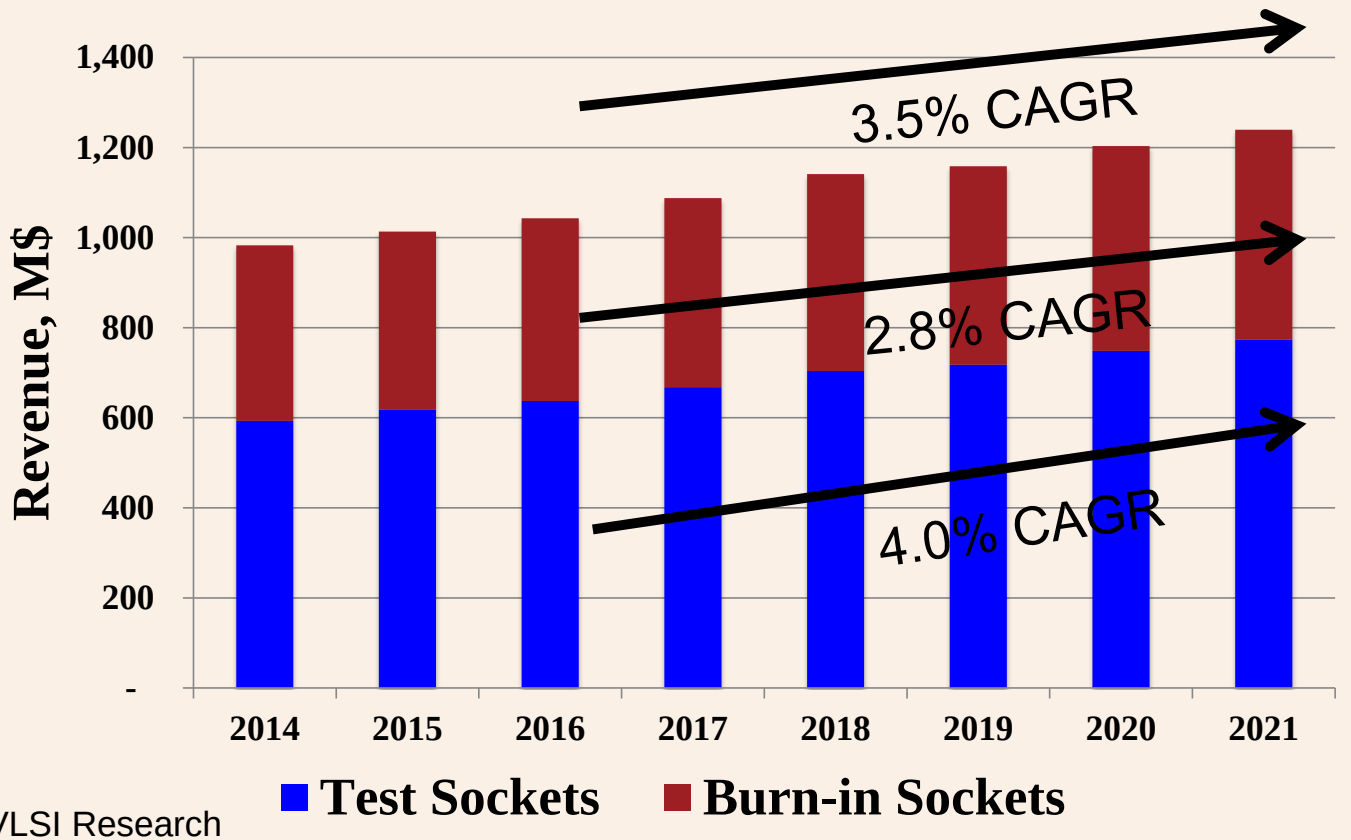
Integrated Data Flow



Device Under Test Interface Hardware

Test Strategy + Hardware + Software

Test and Burn-In Socket Market

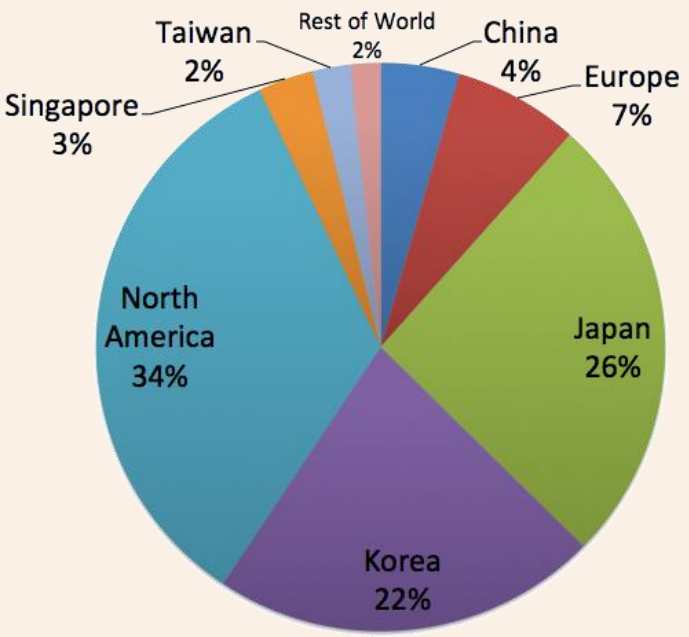


VLSI Research
2016 Preliminary

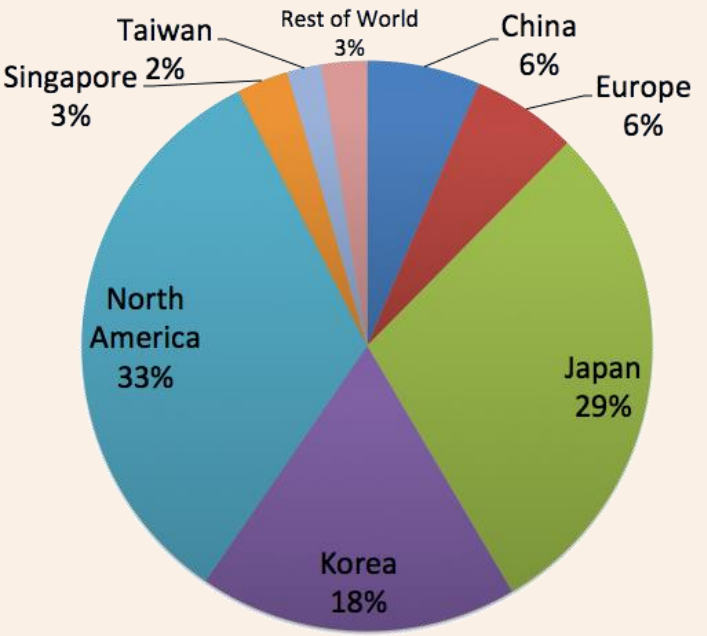
Marketplace Report

Socket Supplier Revenue by Headquarter Region

2015 - $1,013M



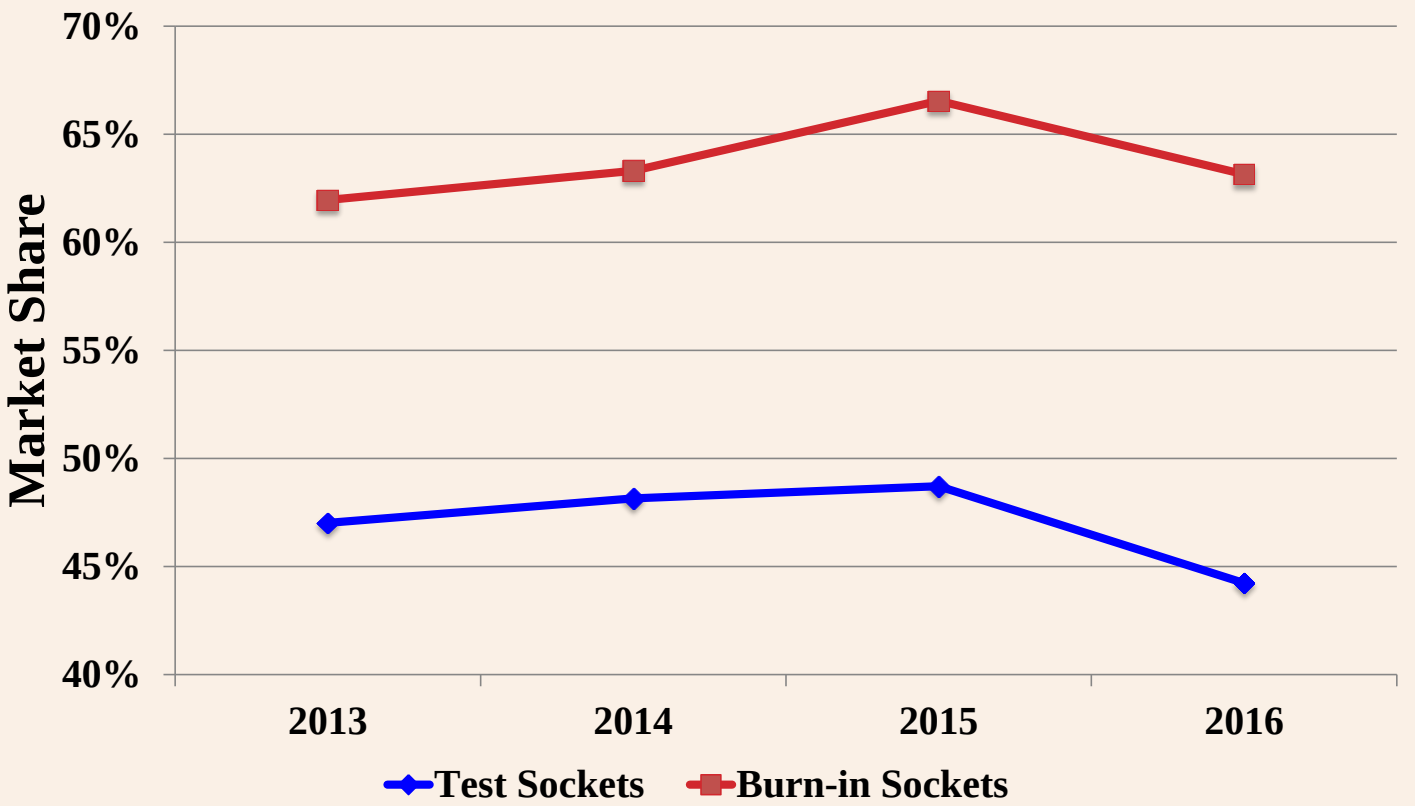
2016 - $1,043M



VLSI Research
2016 Preliminary

Marketplace Report

Top 5 Market Share



VLSI Research
2016 Preliminary

Marketplace Report

Top Test & Burn-in Socket Vendors

Rank	2014	2015	2016 Preliminary
1	Yamaichi Electronics	Yamaichi Electronics	Yamaichi Electronics
2	Enplas	Enplas	Enplas
3	Sensata Technologies	Smiths Connectors	Smiths Connectors
4	Smiths Connectors	ISC	ISC
5	LEENO Industrial	Sensata Technologies	LEENO Industrial

VLSI Research
2016 Preliminary

Acknowledgements

- Test Socket & Burn-in Socket data courtesy of John West at VLSI Research