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STATISTICAL METHOD FOR SETTING UP SAFE SCREEN VOLTAGE FOR PRODUCTS

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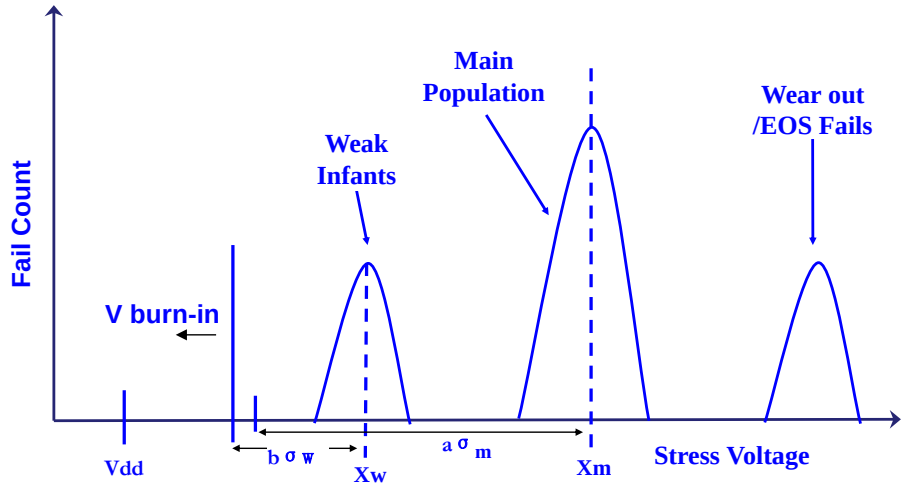
ABSTRACT: Statistics based methodology for establishing a **"Safe Screen Voltage"** for wafer level screening. This methodology has several advantages: it can be easily implemented at wafer level, can be used for quick assessments for Defect Density or Early Life Failure Rate during development stage, to use as continuous wafer level screening at sort, can be translated to Package Level for Pre-shipment Burn-In, can be implemented across any technology node.

Wafer Level Run Procedure

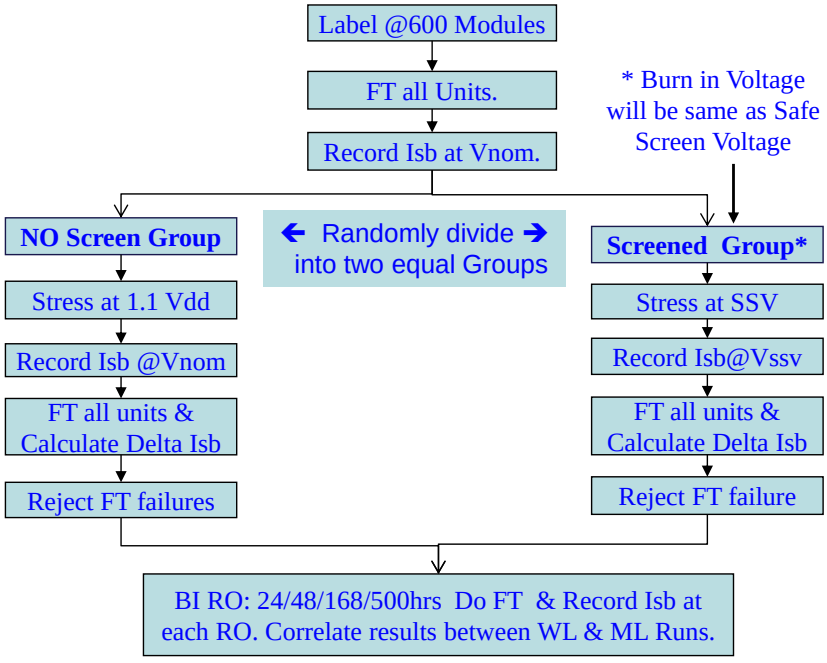
- ✓ Select one wafer or @300 devices.
- ✓ Perform Full FT & Data Log all params.
- ✓ Step Ramp Vdd: start with Vdd, steps 0.1 to 0.2V (0.1xVdd) upward.
  - ✓ At each step stress all devices: 0.5 to 5secs.
- ✓ After each step repeat FT note # of fails.
- ✓ Data log for all devices at each step.
- ✓ Increment stress voltage until all devices fail.
- ✓ Plot histogram of # of fails Vs stress voltage.
- ✓ 2-3 Fail populations per Bathtub will be seen
  - ✓ Low voltage => Early Fails - Defective parts
  - ✓ High voltage => Useful life - Defect free parts.
  - ✓ Very High voltage => Wear out/EOS fails.



Mean of Main Population kill voltage	=	X_m
Mean of Weak Infant population kill voltage	=	X_w
Standard deviation of Main Population kill voltage	=	σ_m
Weak Infant population kill voltage Std. Dev	=	σ_w

- ✓ Choose Vscreen ➔ **Vsafe 2 steps < Vkill**.
- ✓ Extrapolate to -6σ for Vsafe based on incremental stress Gaussian of Vkill.
- ✓ After establishing kill Voltage, calculate Sigma (σ).
- ✓ Get maximum allowed Safe Screen Voltage (DVS)
  SSV = Vkill – 6 Sigma
- ✓ If not able to establish Sigma, use 0.2 V as sigma
- ✓ Calculate Maximum DVS test voltage.
- ✓ Vsafe should kill defects but leave main population.
- ✓ Use Packaged units to do DVS test and Burn in.
- ✓ Correlate Log Normal Isb plots of DVS & BI.

Package/Module Level Correlation Run:



Advantages of Safe Screen by SSV/DVS:

- SSV/DVS can be implemented at CP or at FT
- No additional H/W required if existing boards, probe cards, ovens and testers are used.
- Useful for Production or shipment BI or PRMs.
- Reduces burden on pre-BI screen and SLT.
- ELFR defects of **up to 10-20%** can be achieved.
- Reduce BI duration on IM/ELFR **upto 1-2days BI**.
- Cost Savings: On wafers, packaging, ovens & testing on weak parts that can be screened out:@**0.25-0.5M/yr**
- Faster feedback for process CIPs **by 8 to 10 weeks**.
- Faster Learning Cycles for yield & Quals: **@2months**