
2nd Annual
BiTS
CHINA 中国
September 13, 2016
Session 2
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Session 2
Frank Zhou
Session Chair

BiTS China

Socket Technology

"Study of Probe Pin Internal Resistance"
Takuto Yoshida - Test Tooling Solutions Group

"Monte Carlo Analysis for PoP Alignment"
DeXian (Frank) Liu - Smiths Connectors

"Conductive Elastomer vs Spring Probe: Performance & Application"
Jiachun (Frank) Zhou - Smiths Connectors

"Do Socket and Kits Design Matter for Die Cracking?"
Yuanjun Shi - TwinSolution Technology

Session 2
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Session Chair

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Socket Technology

"弹簧探针内部阻值的研究"
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"叠层封装测试插座设计中校直的蒙特卡洛分析法"
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Do Socket and Kit Designs Matter for Die Cracking?

Yuanjun Shi, Kane Liu
Twinsolution Technology (Suzhou) Ltd.

BiTS China Workshop
Suzhou
September 13, 2016

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- Background
- Possible reason analysis
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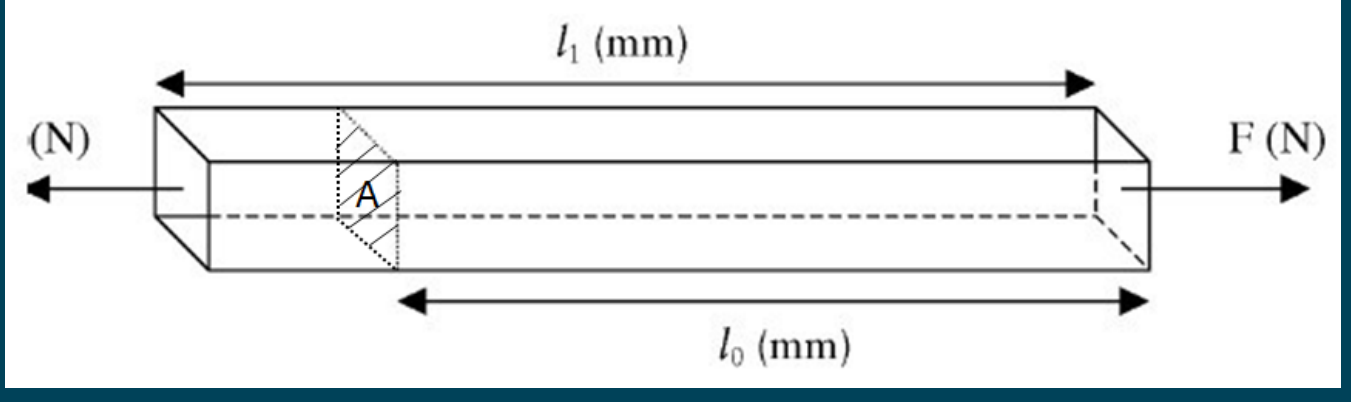
- Result Analysis & Summary

Basic Knowledge in Warpage /Deformation

Tensile Test



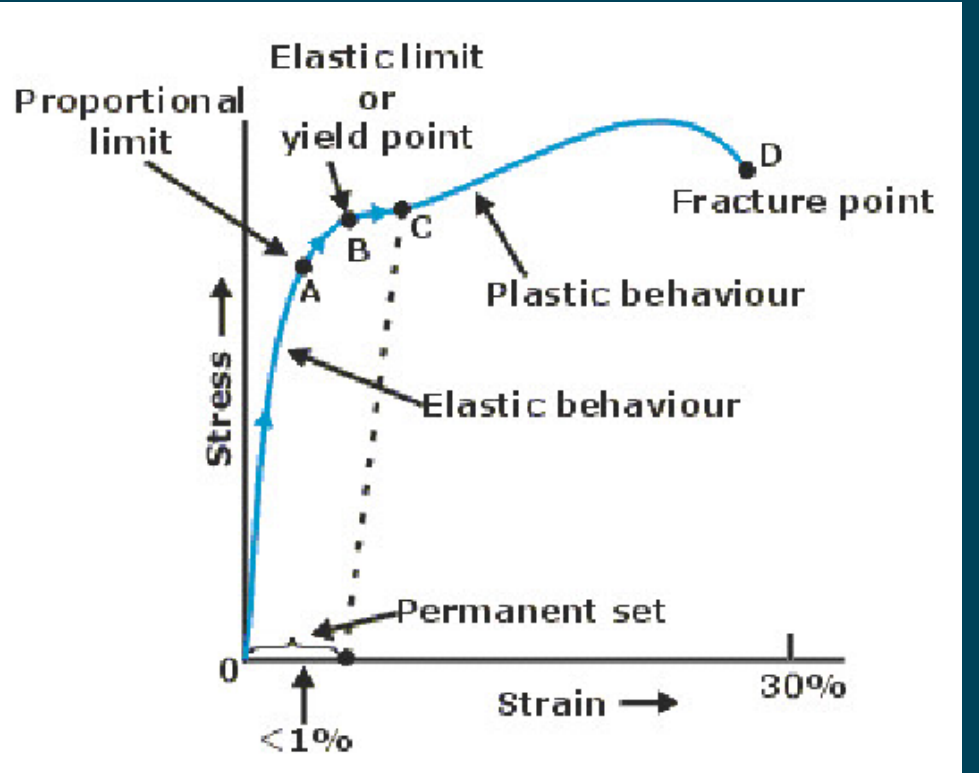
$$\sigma = F/A$$

$$\varepsilon = \ln (l / l_0)$$

when Δl small, $\varepsilon = \Delta l / l_0$

Basic Knowledge in Warpage /Deformation

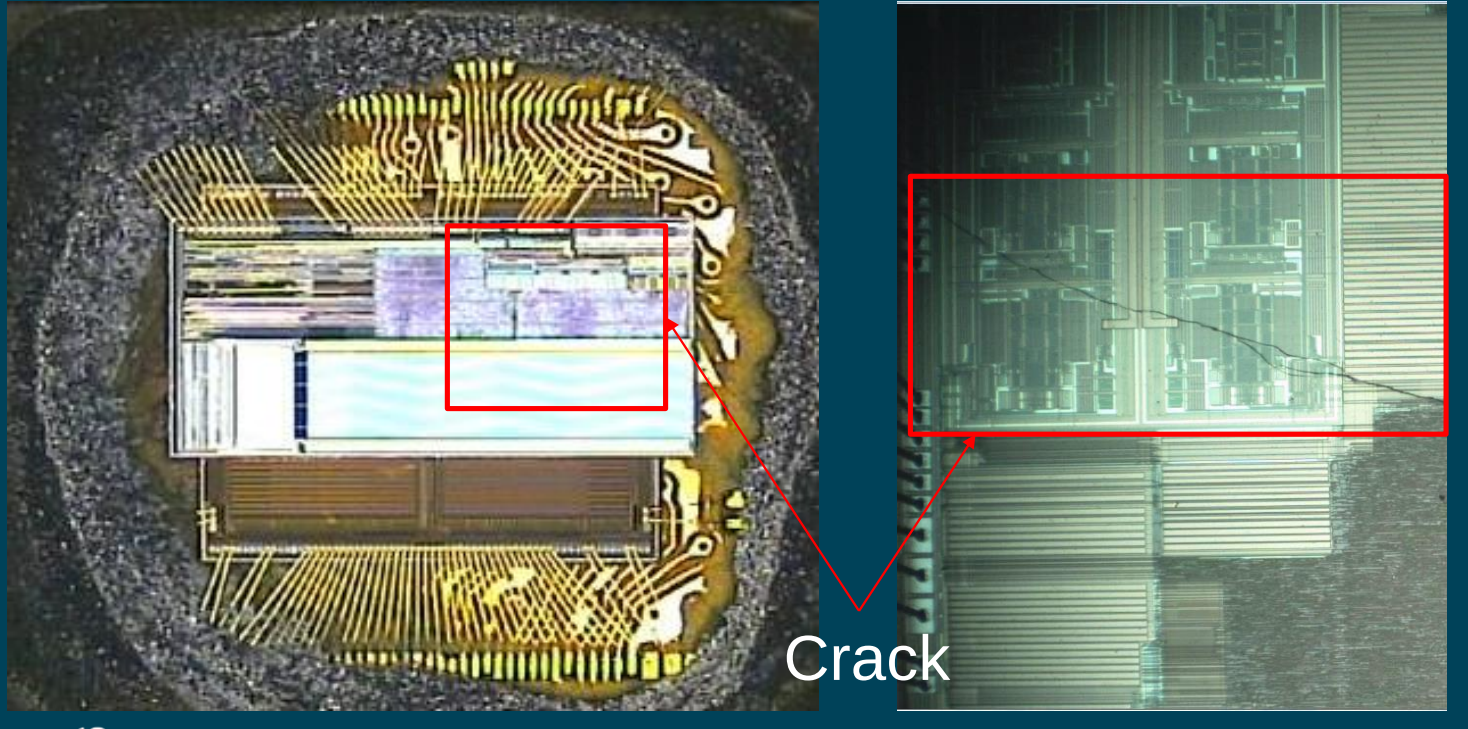
Typical stress vs strain curve



A typical stress-strain curve for a ductile metal

Background

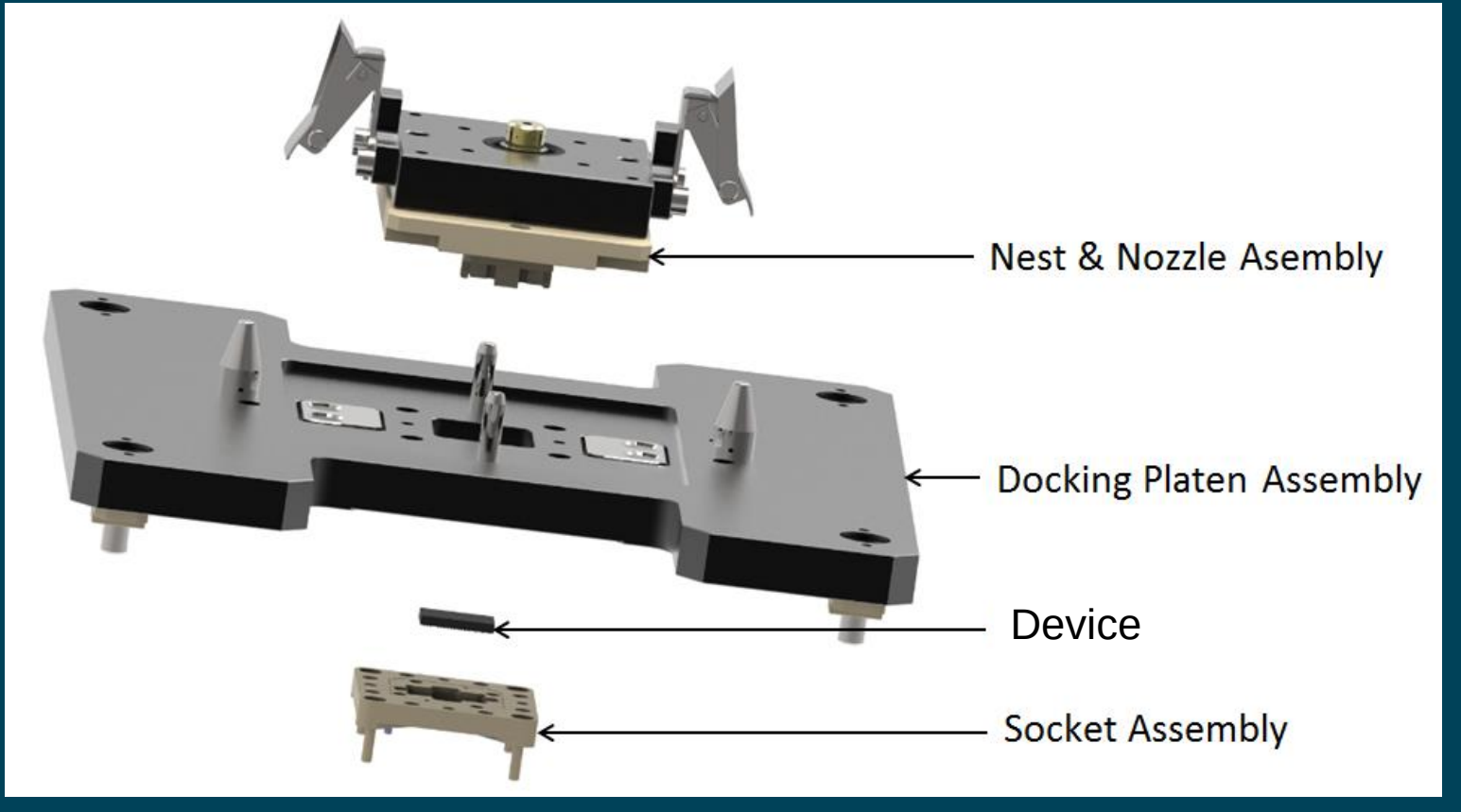
For FT stage, it is easily to detect die crack. It is very important to prevent die crack.



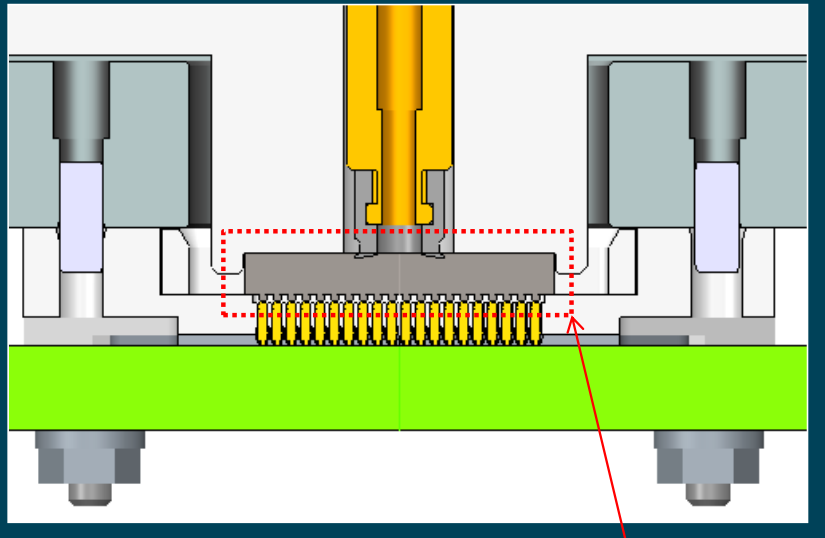
Possible Reason Analysis

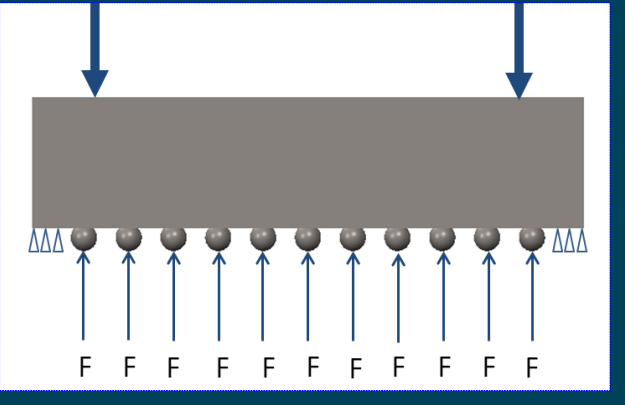
- Thermal Stress
- Low-Temperature Stress
- High and low temperature impact
- Mechanical Stress
- Moisture Absorption
- Molding
- ….

Socket & Change Kits



Die Stress State

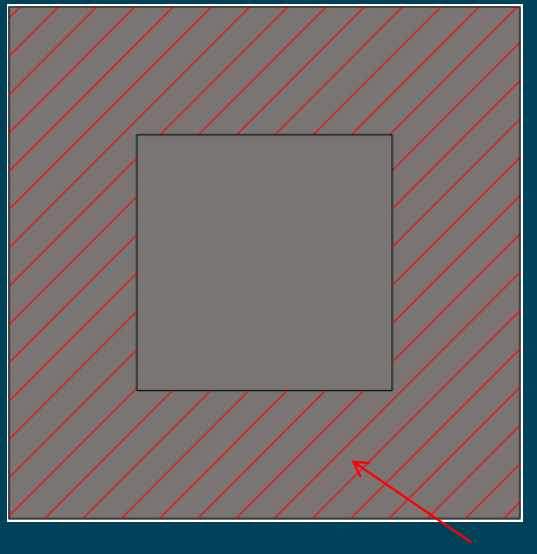


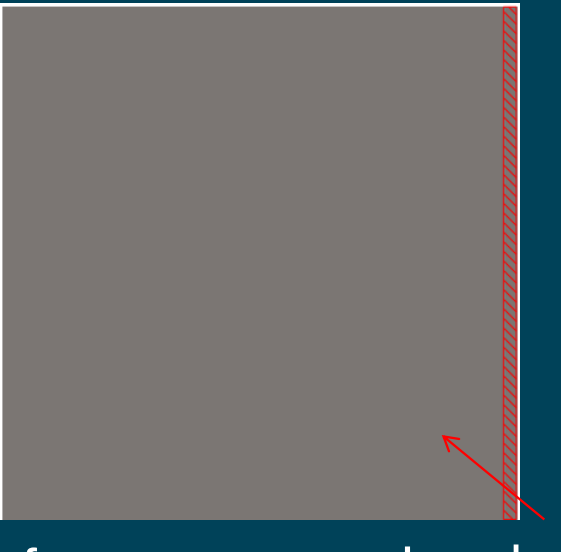


Ideally Die stress

Package

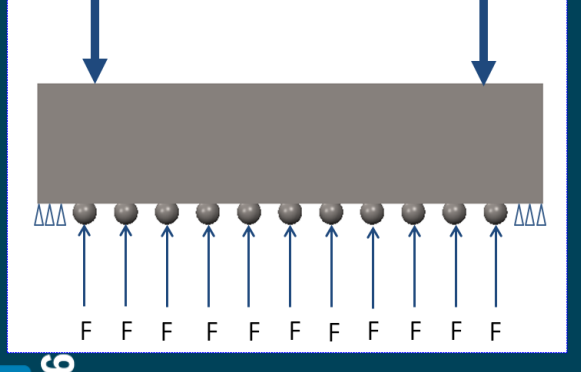
FEA Model

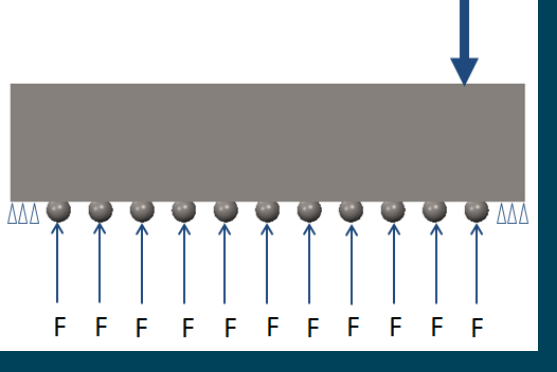




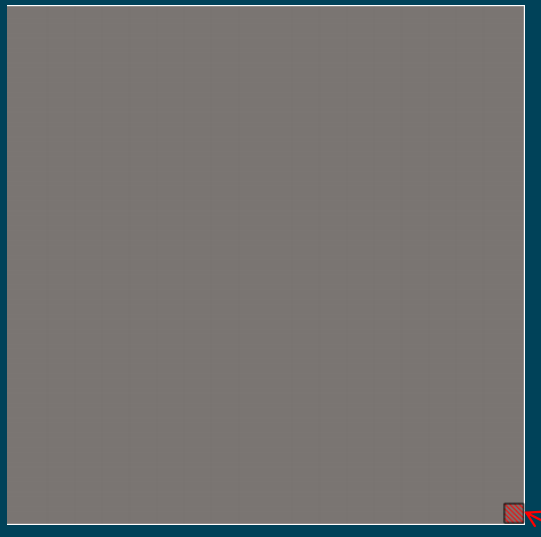
Load on surface

Load on edge

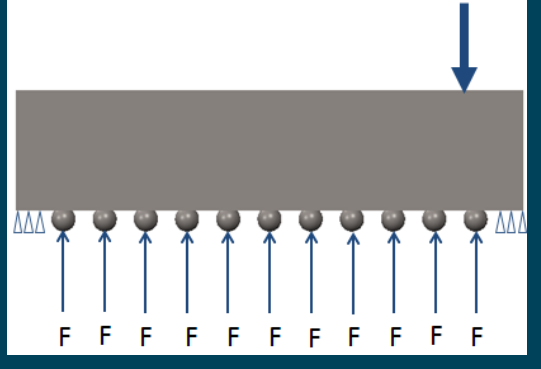




FEA Model

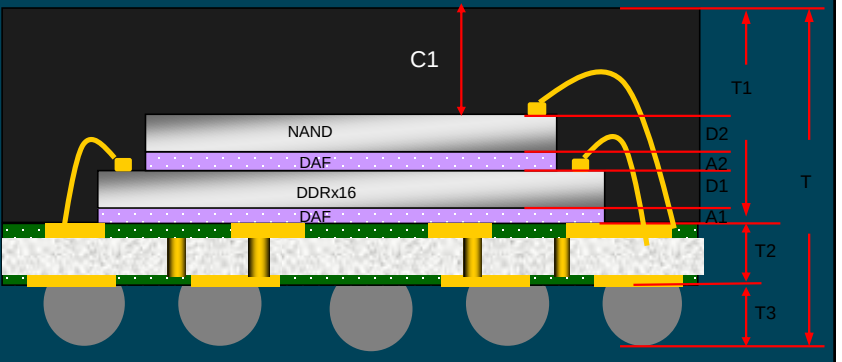


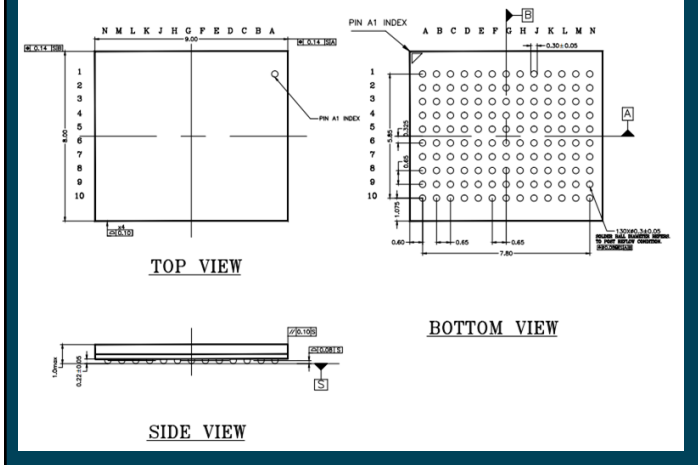
Load on point



FEA Model

- **Device information:**
  - PKG Size:9x8x1.0mm(max.)
  - Nand size: 5.488 x 2.686mm (with Scribe line x/y-70um)
  - DDR size: 4.794 x 4.192mm (with Scribe line x/y-89.93um)





POD

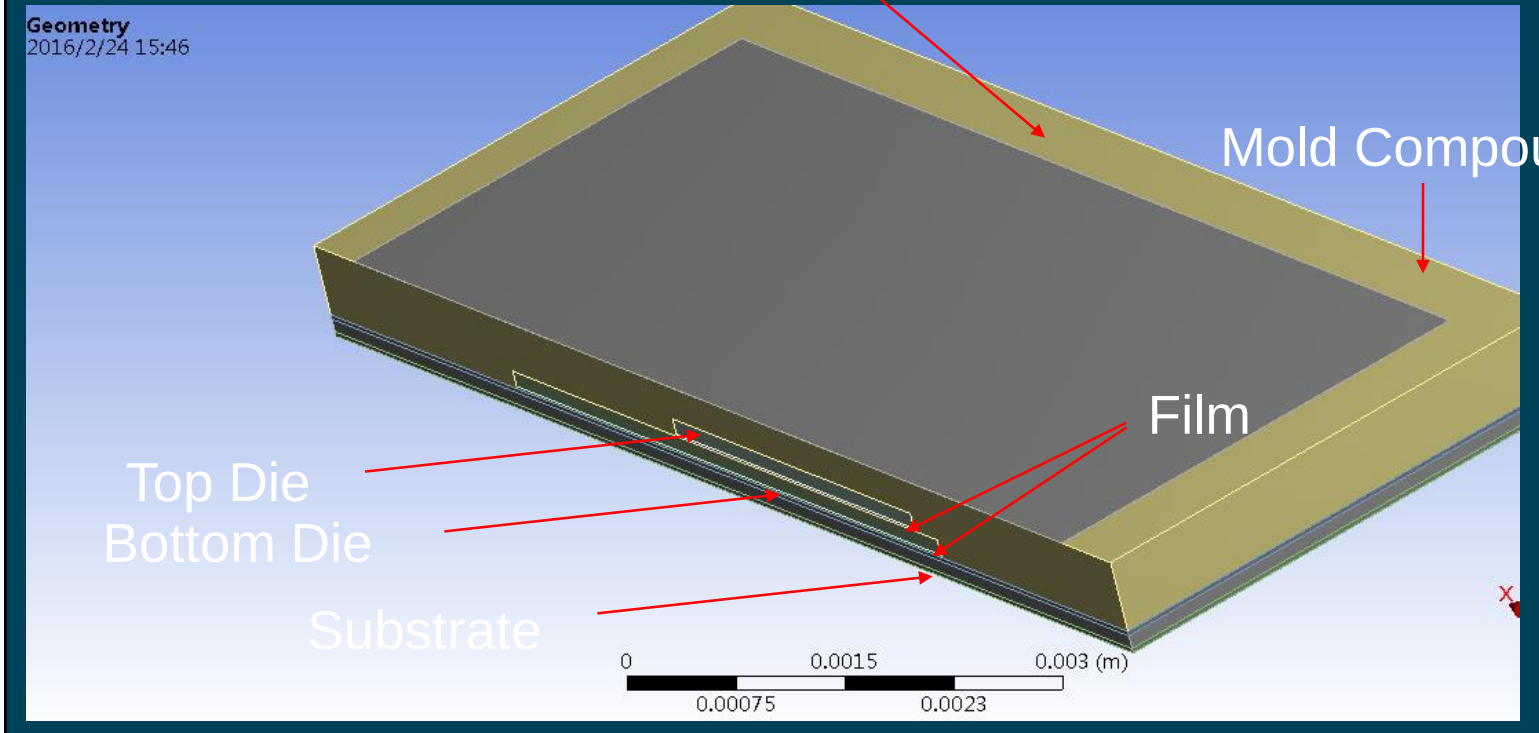
Item	PKG Structure	Thickness (um)	BOM	Tolerance
C1	mold to chip clearance	270		15
D2	2nd chip thickness	120	Gold wire: Heraeus HA6 20um	10
A2	2nd adhesive	20	Nitto EM760	4
D1	1st chip thickness	120	Gold wire: Heraeus HA6 20um	10
A1	1st adhesive	20	Nitto EM760	4
T1	mold cavity	550	G760L	25
T2	Substrate	170	Doosan DS7409HGB (core : 100) AUS320, 2 layers, 2block Plating: Bondfigner: Ni/Au ball land: OSP	30
T3	Solder Ball	220	Duksan SAC105_Φ0.3mm	50
T	Total height	940		63

Material Properties

Materials used and the mechanical properties

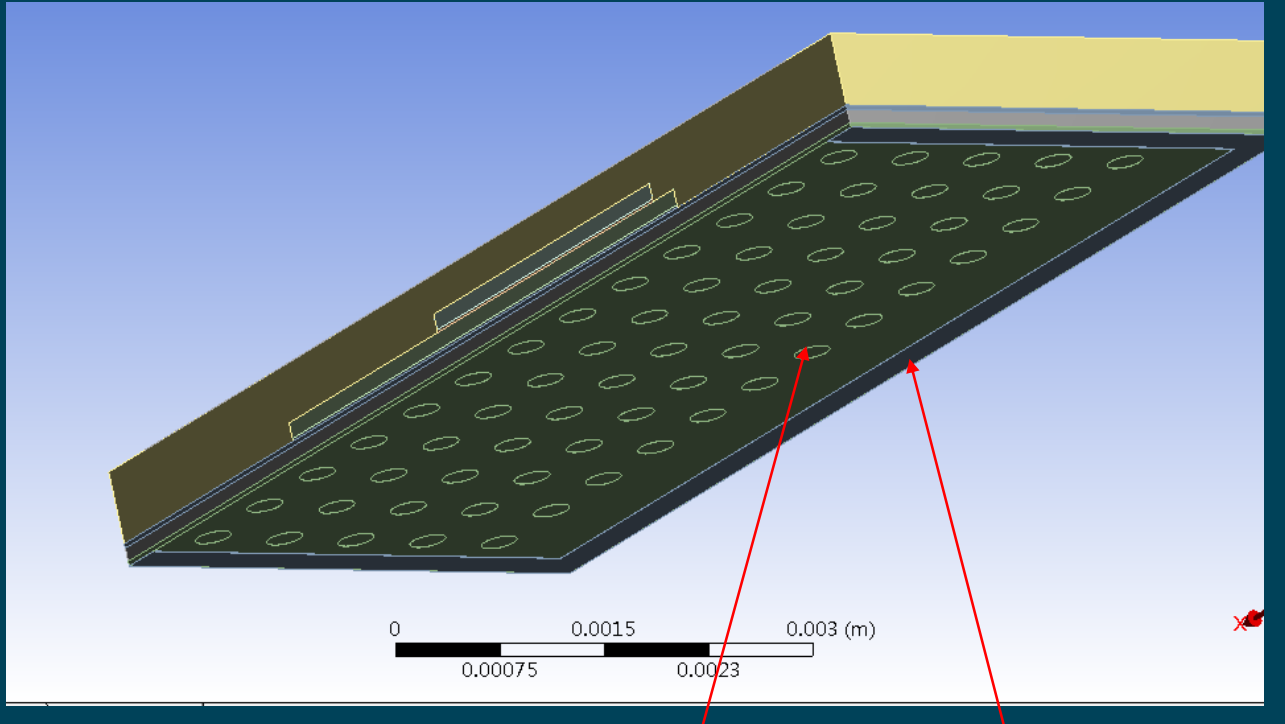
Material Type	Material Remark	Young's Modulus	Poisson's Ratio	Yield Strength	Tensile Strength
Unit		GPa	-	MPa	MPa
Die(Silicon)	Top Die	131	0.28		165
Die(Silicon)	Bottom Die	131	0.28		165
Mold compound	Mold compound	17.9	0.3		160
Adhesive		0.95	0.35		
Substrate	Core	25	0.3		

FEA Model Setup



- Simplify Model
- Do Symmetry Analysis

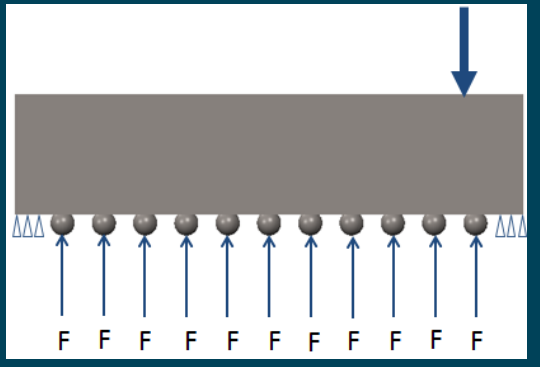
FEA Model Setup

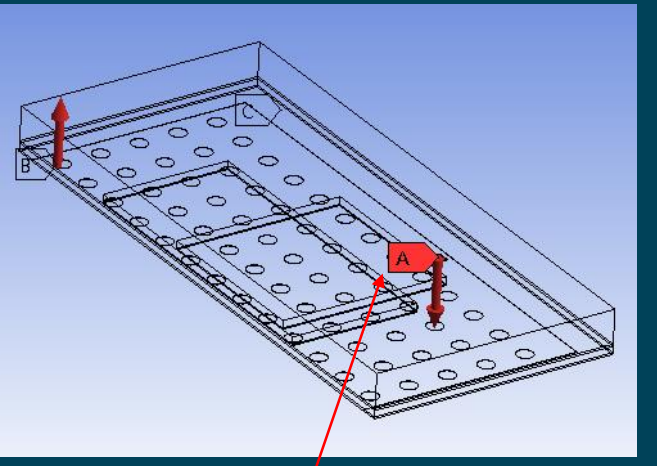


Boundary Condition Setup

Case 1:
Load on point near Die edge.

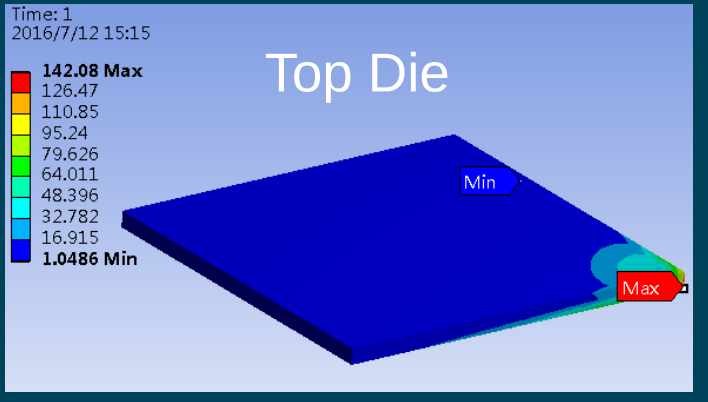
F= 1.0Kgf

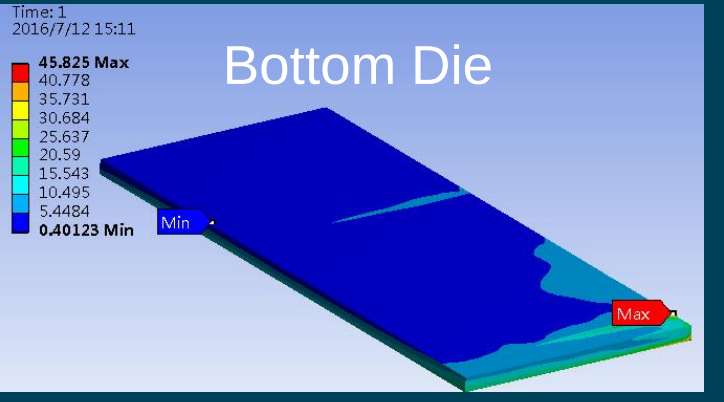


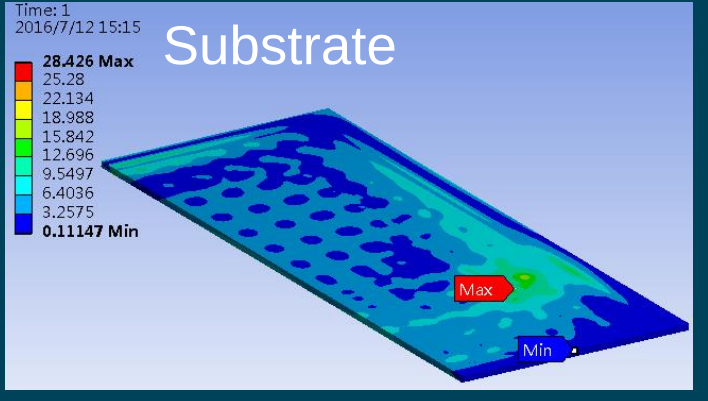


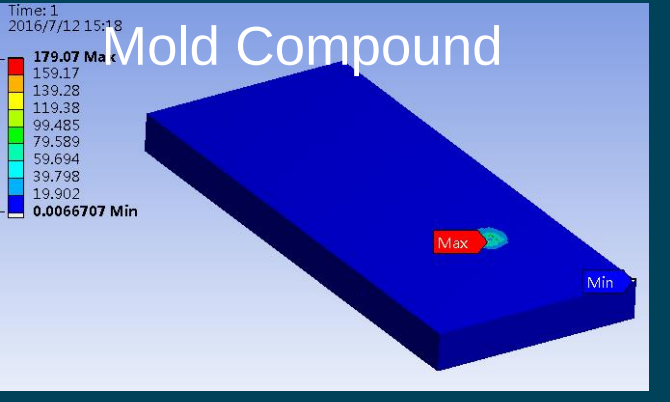
Load Point

Stress Result





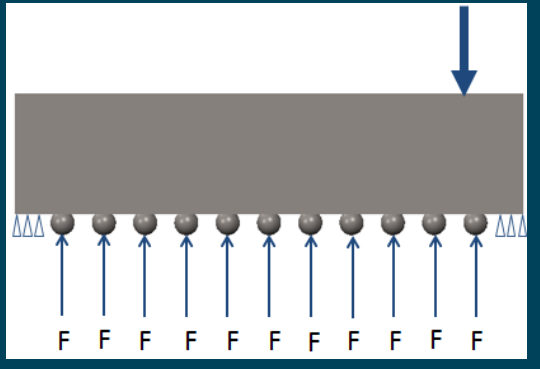


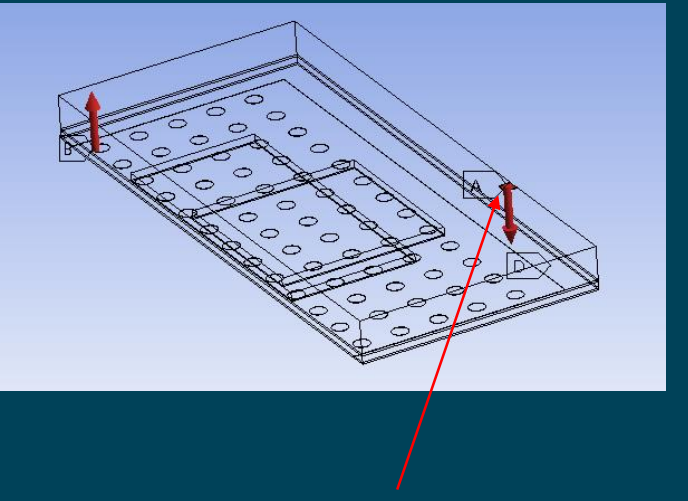


Boundary Condition Setup

Case 2:
Load point near Package edge, far away Die edge.

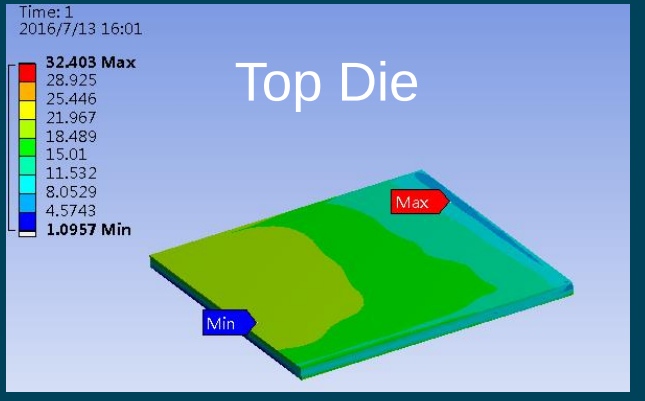
F= 1.0Kgf

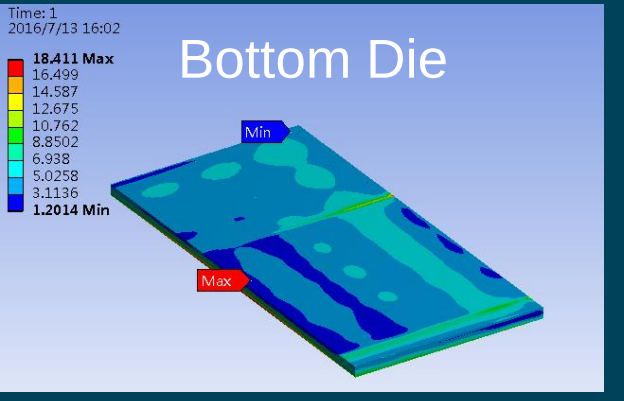


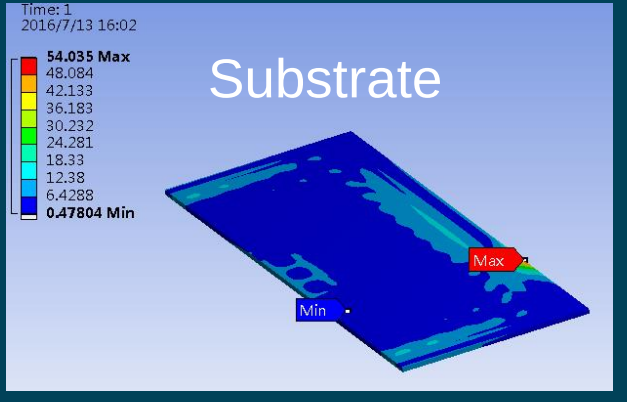


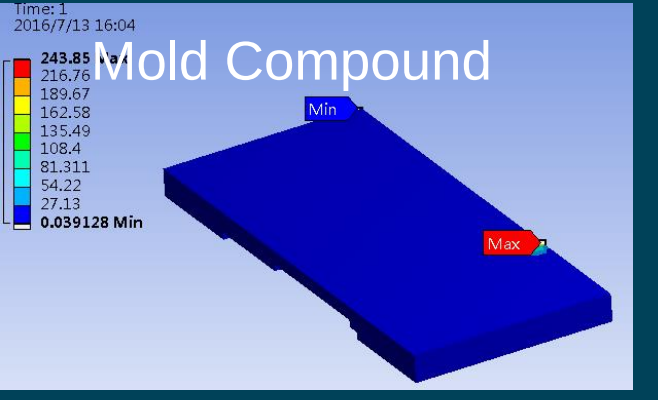
Load Point

Stress Result





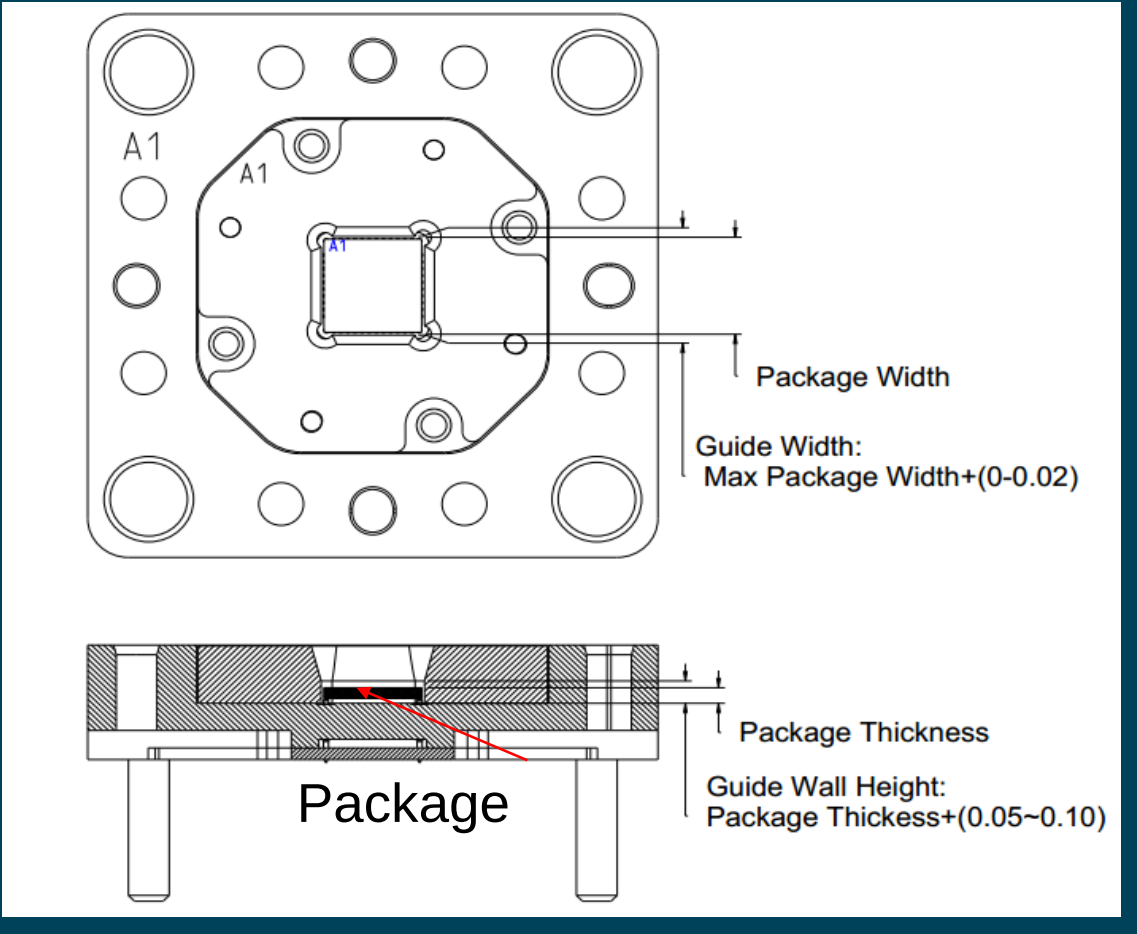




Result Analysis

- Load on point near Die edge and significant increase the stress (Max:142.08 Mpa) for the Top die, which is near to the silicon die tensile strength limit , since the kits is not compress the die.
- This load point near Package edge, far away Die edge; Significant decrease the stress (Max: 32.4 Mpa) for Top die.
- It is obvious when the nest contact to the device quite close to the Top die, this will create a stress focus on the Top die.
- Once stress concentrate in one point, even if the load force is very small, die crack will occur. Usually this is due to pocket not guiding the package well.

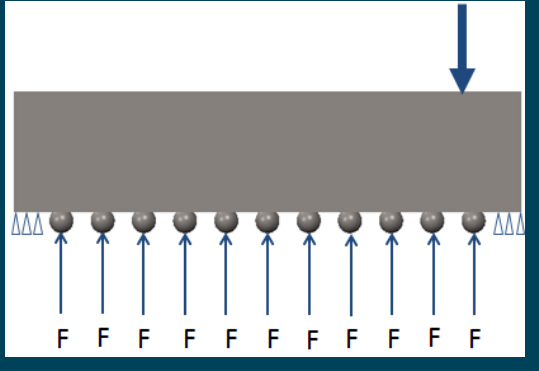
Result Analysis

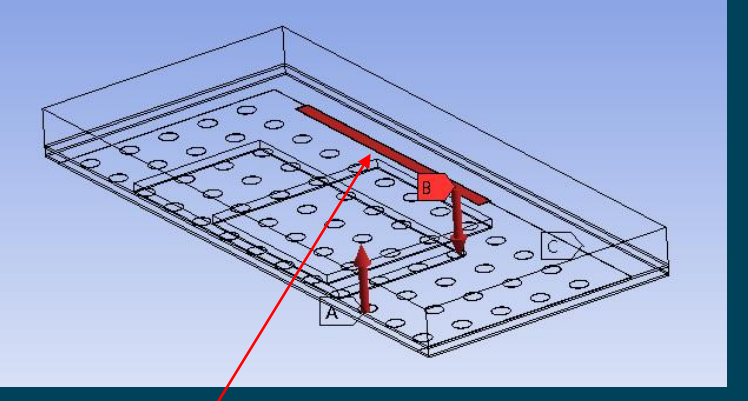


Boundary Condition Setup

Case 3:
Load on Die edge.

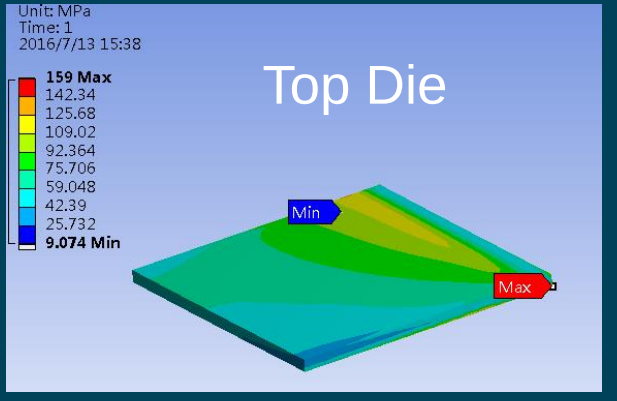
F= 7Kgf

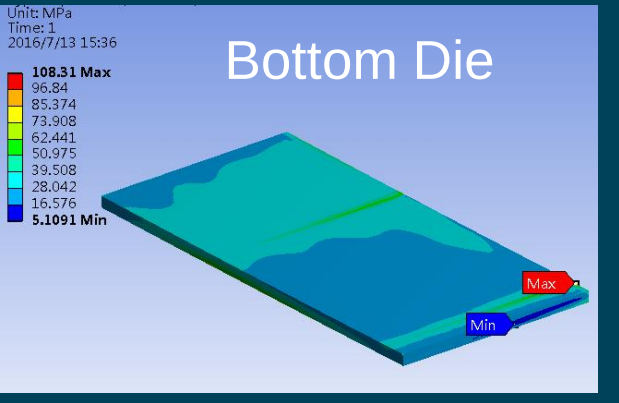


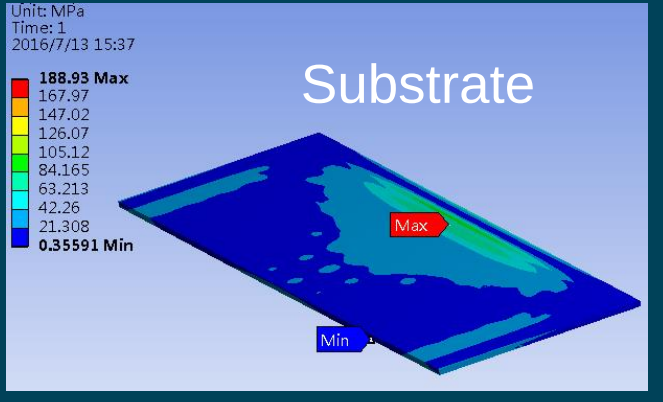


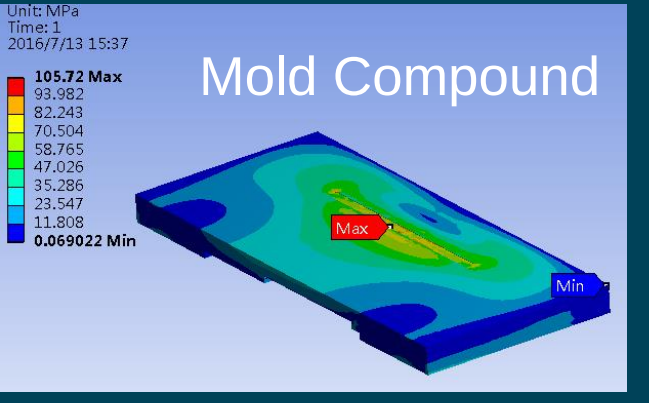
Load Die edge

Stress Result





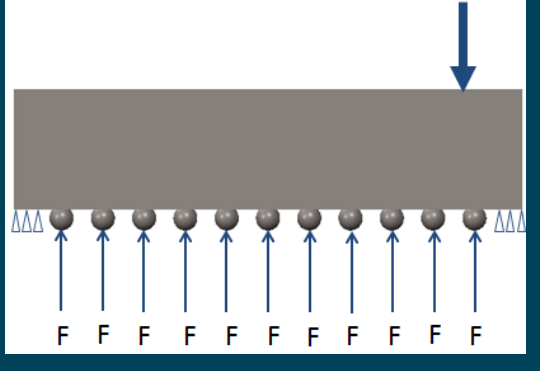


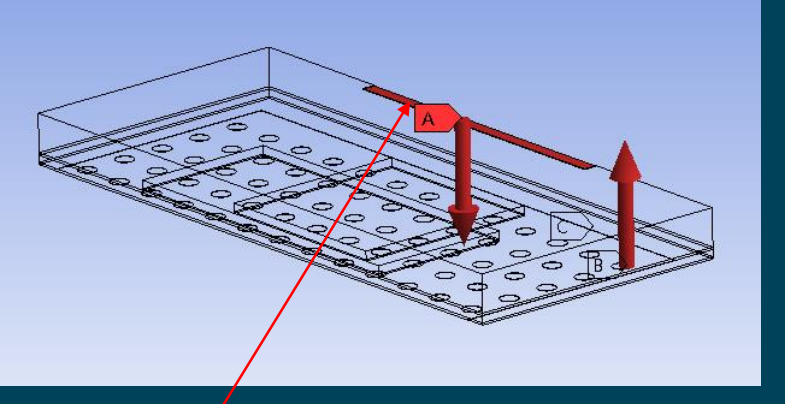


Boundary Condition Setup

Case 4:
Load on package edge.

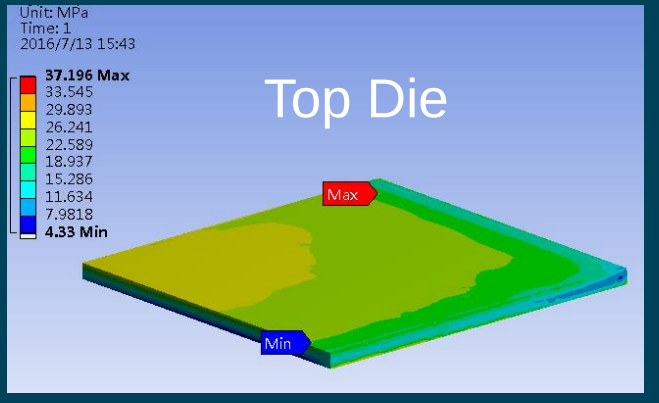
F= 7Kgf

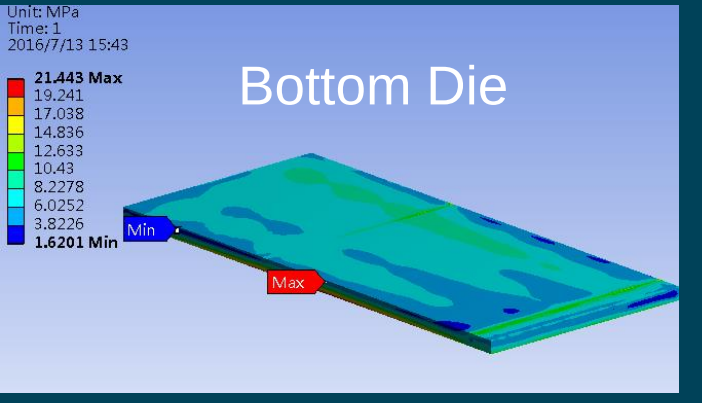


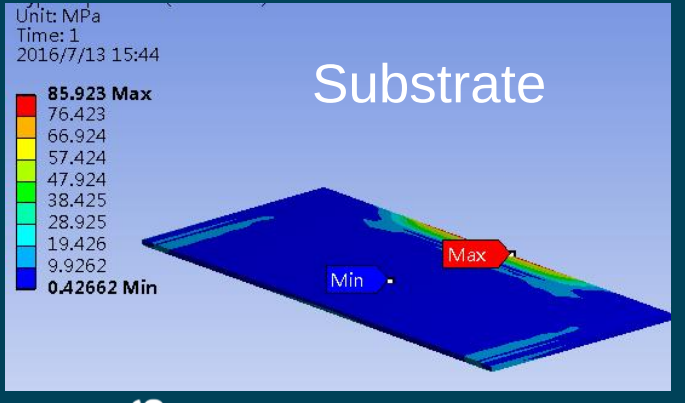


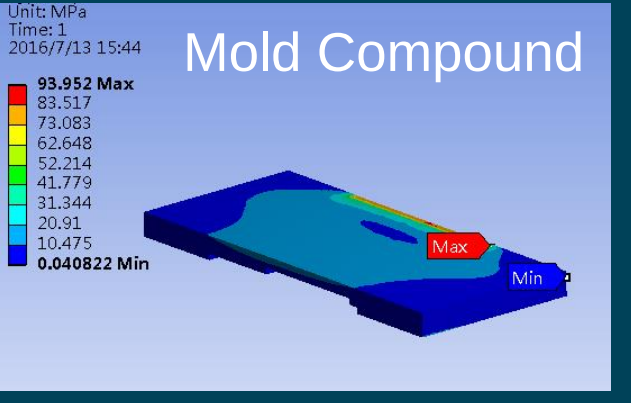
Load package edge

Stress Result









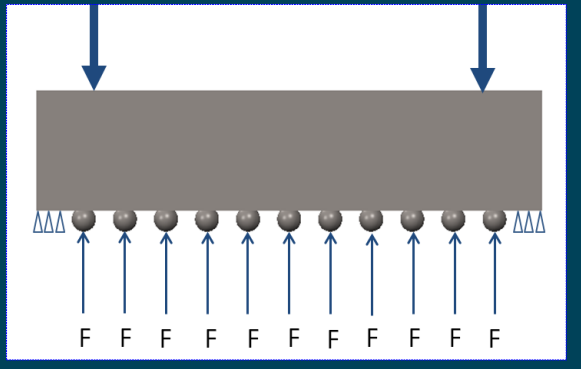
Result Analysis

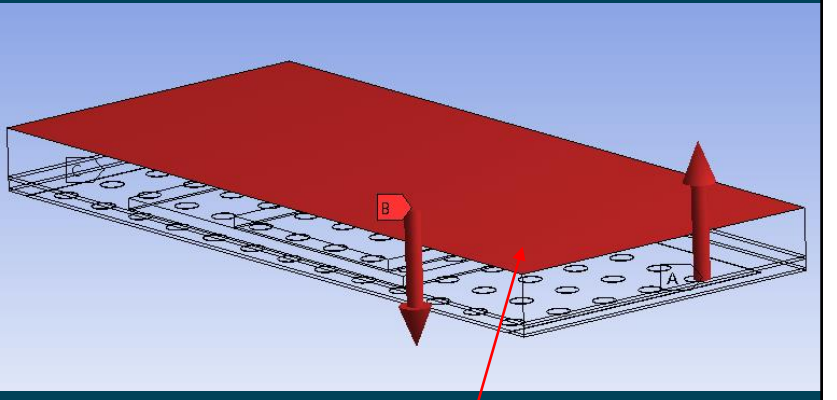
- Load on Die edge and significant increase the stress (Max:159 Mpa) for the Top die with 7 Kgf, which is near to the silicon die tensile strength limit ,die maybe crack from the load force position .
- Load on Package edge, far away Die edge; the load force don't load on die surface directly, can significant decrease the stress (Max: 37.196 Mpa) for Top die.
- Compare with case 1,2,3,4, we can conclude that we should avoided load force on die surface directly, can decrease the die stress.

Boundary Condition Setup

Case 5:
Load on whole surface

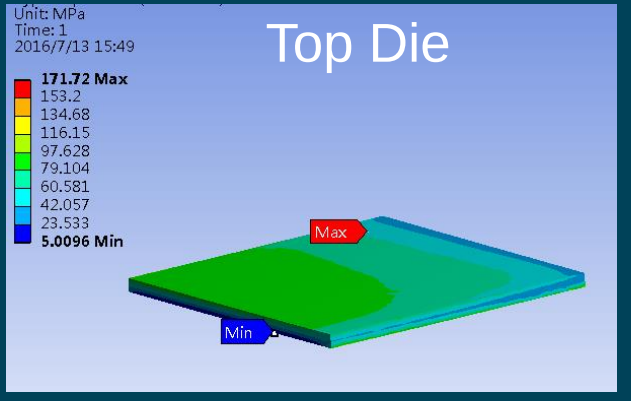
F= 10Kgf

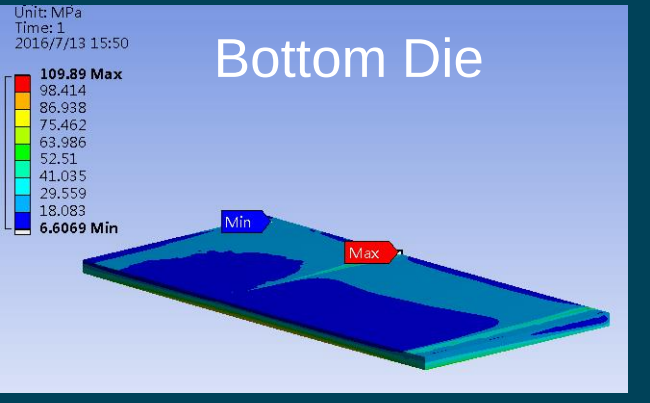


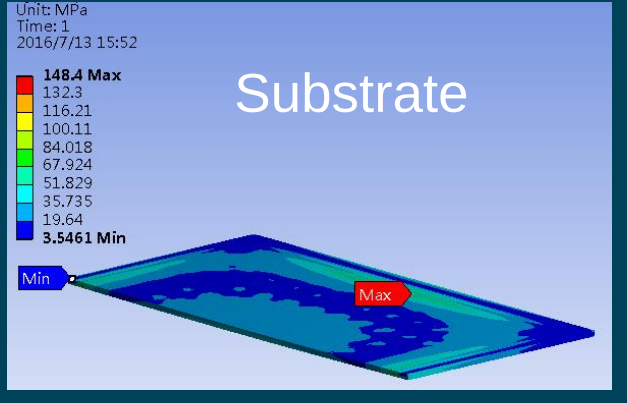


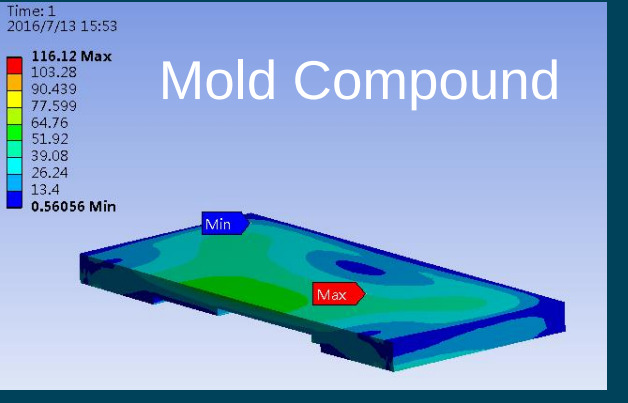
Load on surface

Stress Result





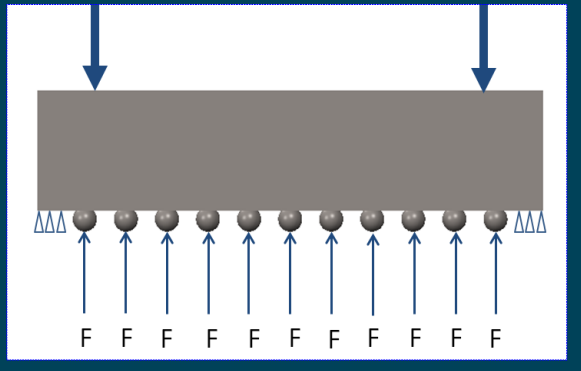


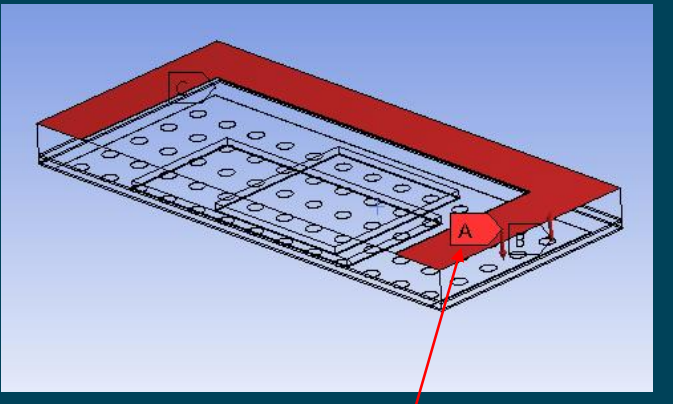


Boundary Condition Setup

Case 6:
Load on partial surface

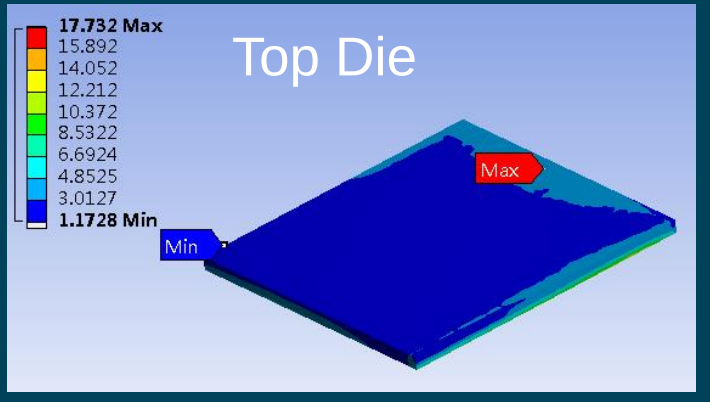
F= 10Kgf

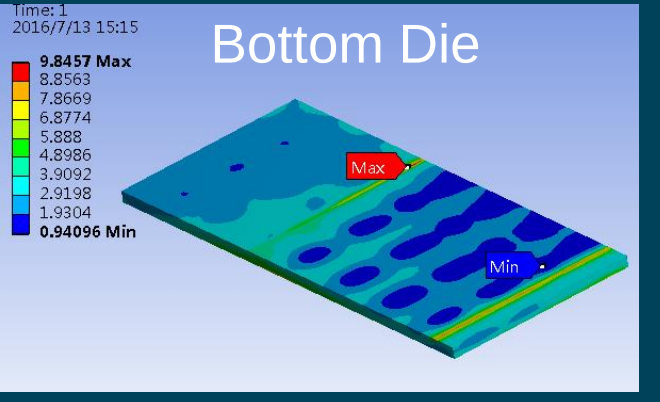


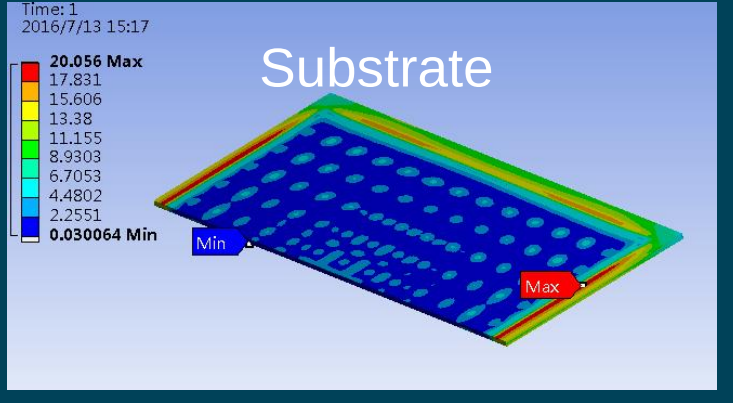


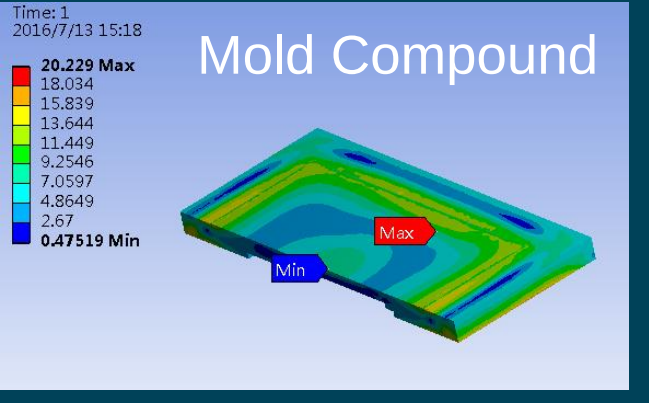
Load on surface

Stress Result





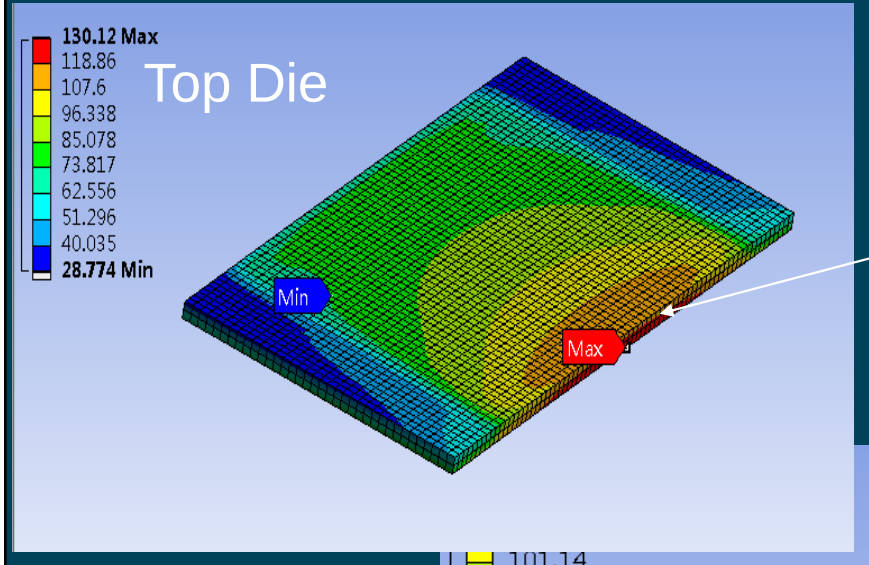




Summary Table

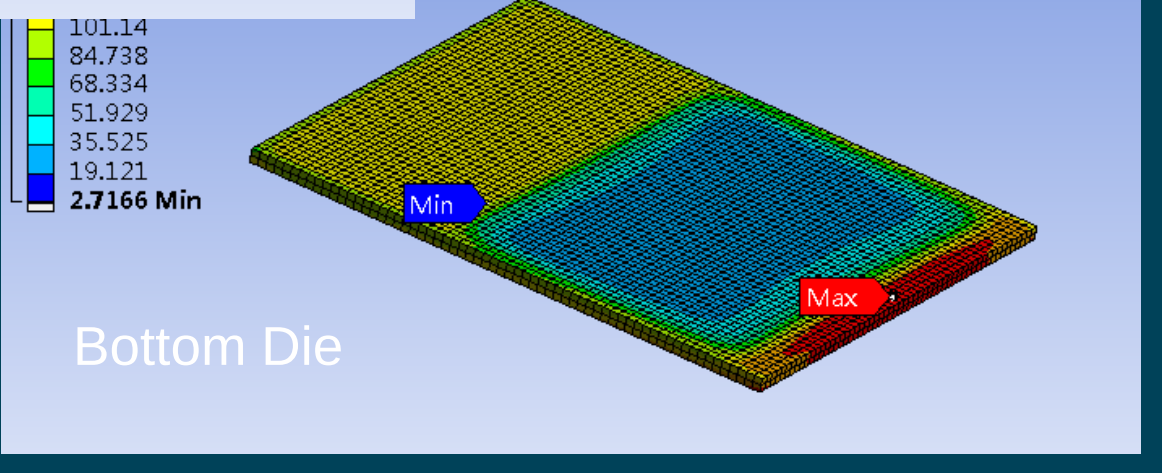
Case No	Load	Top (Mpa)	Bottom (Mpa)	Substrate (Mpa)
1	1Kg	142	45.83	28.4
2	1Kg	32.4	18.4	54.035
3	7Kg	159	108	188.93
4	7Kg	37	21.433	85.923
5	10Kg	171.72	108.9	148.4
6	10Kg	17.7	9.8	20.1

Thermal Stress



- Maximum stress happened in the middle of the top die.
- Highly suspect the CTE mismatch cause the die crack.

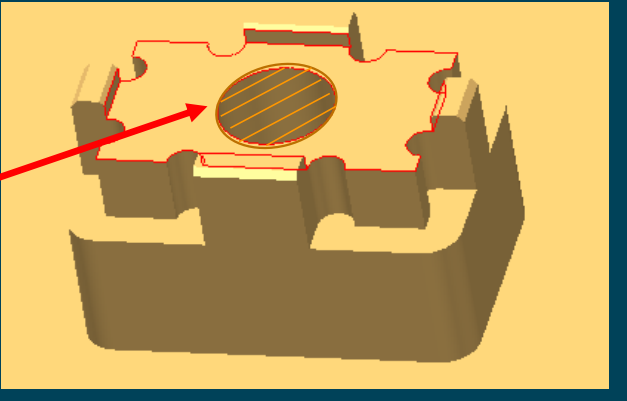
Temperature from $22C^0$ to $150C^0$



Result Analysis

- For stack die package, sometime uniform loading eventually create a stress focus and cause die crack.
- In this case, we found the handler force setup can not exceed 7 KgF.
- Platen design is very important to stack die package, especially when the top die do not have support underneath.
- Thermal stress could be also a very important factor for die crack.

Avoid contacting die directly



Platen shape