2nd Annual

September 13, 2016

GYgg]cb %

Presentation / Copyright Notice

The presentations in this publication comprise the pre-workshop Proceedings of the BiTS China Workshop. They reflect the authors' opinions and are reproduced here as they are planned to be presented at the BiTS China Workshop. Updates from this version of the papers may occur in the version that is actually presented at the BiTS China Workshop. The inclusion of the papers in this publication does not constitute an endorsement by the BiTS Workshop or the sponsors.

There is NO copyright protection claimed by this publication. However, each presentation is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.

The BiTS logo, 'Burn-in & Test Strategies Workshop', 'BiTS China', and 'Burn-in & Test Strategies China Workshop' are trademarks of BiTS Workshop.

BiTS Burn-in & Test Strategies Workshop 2016 China

Session 1

Yuanjun Shi

Session Chair

BiTS China

High Frequency & Burn-In

"Implementation Challenges of and ATE Test Cell for At-Speed Production Test of 32 Gbps Applications "

Jose Moreira - Advantest

"Addressing Challenges in High Temperature Burn-In"

Paolo Rodriguez - Analog Devices Philippines

"Derating Transient Voltage Suppressor Diodes for Burn-In Applications"

Gil Conanan - Analog Devices Philippines

"An Ignorable Testing Technology for High Speed/Frequency Device Testing"

Pang Cheng Chiu - Jthink Technology

BiTS Burn-in & Test Strategies Workshop 2016 China

Session 1
施元军
Session Chair

BiTS China

High Frequency & Burn-In

"32 Gbps速度应用在自动测试单元量产实施中的挑战 "
Jose Moreira – Advantest

"高温老化测试挑战的讨论"
Paolo Rodriguez - Analog Devices Philippines

"老化测试中瞬态电压抑制器的降额设计"
Gil Conanan - Analog Devices Philippines

"一个不容忽视的高速芯片测试方法"
Pang Cheng Chiu - Jthink Technology

BiTS Burn-in & Test Strategies Workshop 2016 China

Implementation Challenges of an ATE Test Cell for At-Speed Production Testing of 32 Gbps Applications

Jose Moreira, Hubert Werkmann, Daniel Lam, Bernhard Roth
Advantest

BiTS China Workshop
Suzhou
September 13, 2016

Presentation Outline

- Challenges of a 32 Gbps Volume Production ATE Solution
- Solution High Level Block Diagram
- ATE to DUT Test Fixture Interconnect
- Signal Path Loss
- Test Cell Integration
- SW Integration Challenges
- Test Fixture PCB and DUT Socket Challenges
- Calibration Strategy and Challenges
- DUT Reference Clock
- Solution Performance Results
- Conclusions
- References

BiTS 2016 China
Burn-in & Test Strategies Workshop

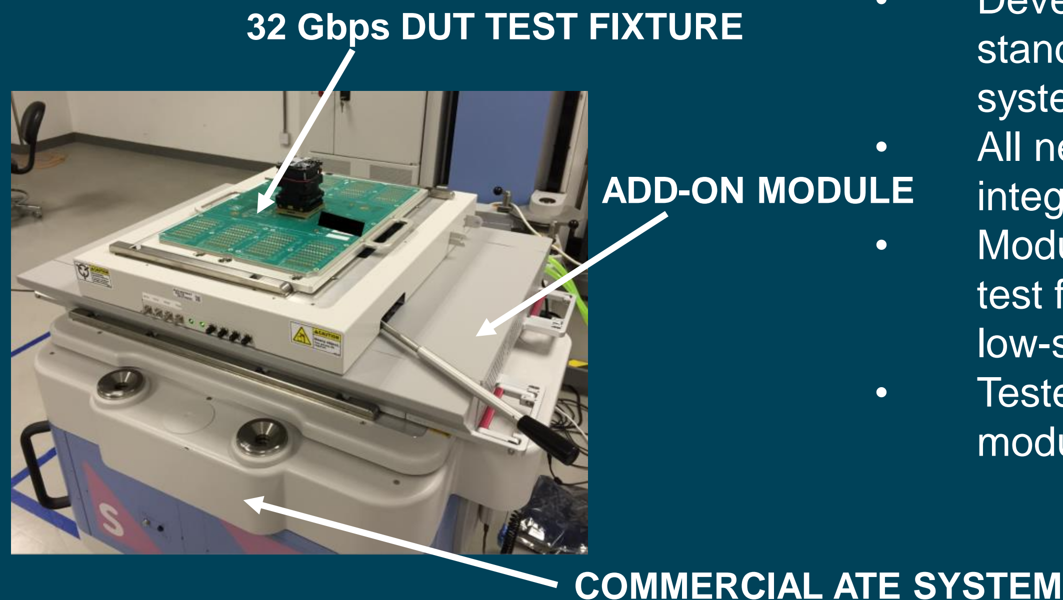
The Challenge

Develop a 32 Gbps cost effective testing solution

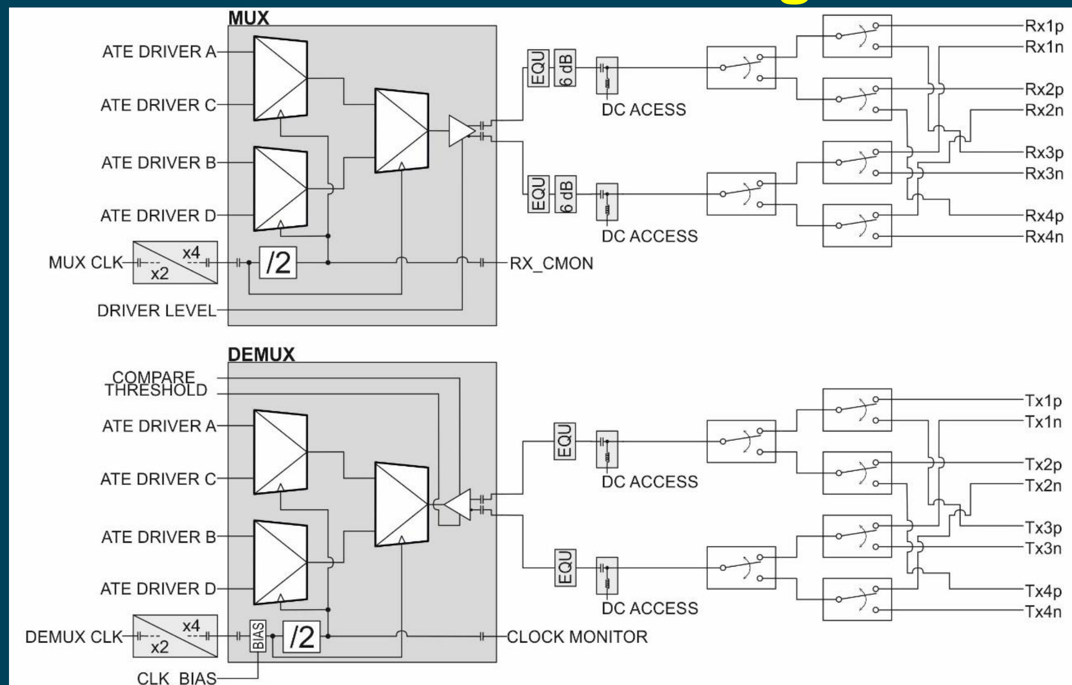
- In time for the customer needs.
- Low development costs (compared to a full ATE integrated solution).
- High performance and fully compatible with standard HW and SW ATE test cell environment (handler and prober).

Solution

- Develop an add-on module to a standard commercial ATE system.
- All needed active components integrated inside this module.
- Module uses a compatible ATE test fixture interface for all the low-speed and power signals.
- Tester resources not used by the module are feedthrough.



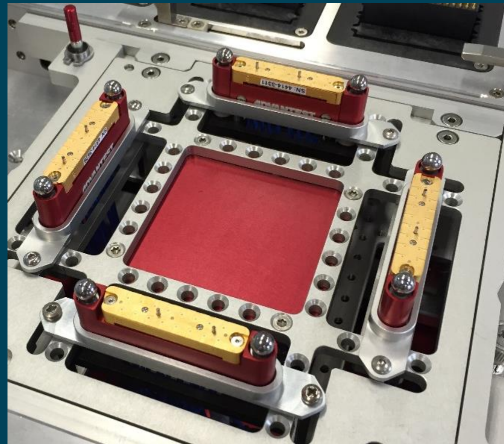
Solution Block Diagram

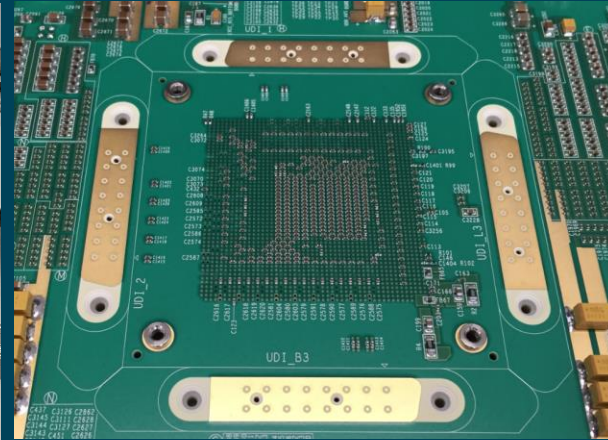


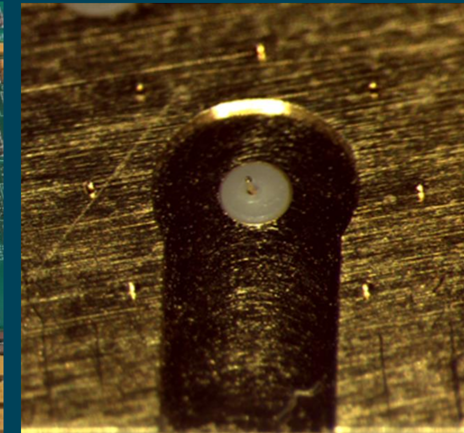
- Standard ATE system provides timing, data and power to the active modules.
- DC Access and common mode voltages provided by a Bias-Tee.
- Test time, signal performance and equipment cost are optimized by using a switch matrix to increase number or lanes to be measured.
- Maximum configuration of 16 measurement lanes.

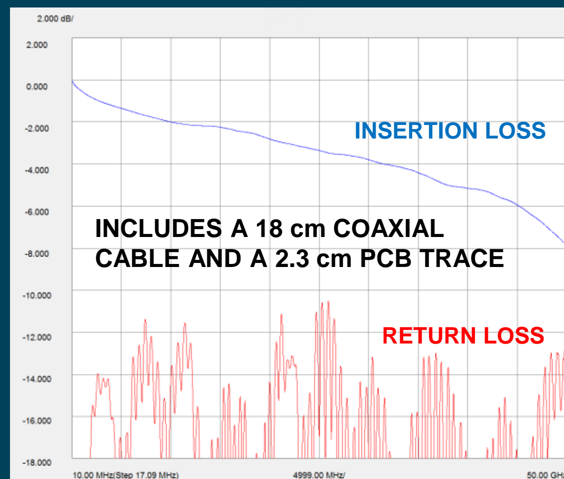
REFERENCES [1,2]

High-Speed DUT PCB Test Fixture Interconnect









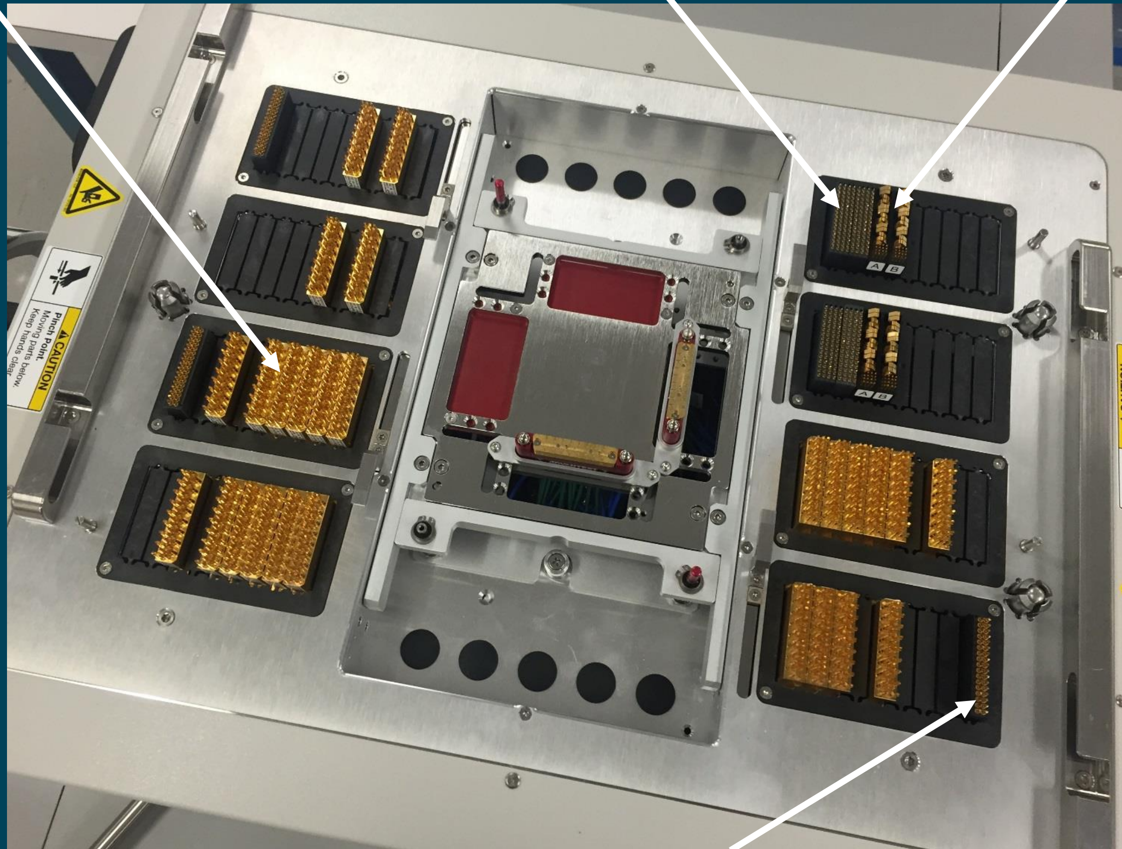
- Blind mating interconnect approach to allow easy exchange of DUT test fixtures.
- Measurements show a very high bandwidth (no resonances) suitable for 32 Gbps applications.
- Connectors need to be placed as close as possible to the DUT socket.

Feedthrough Standard ATE Resources

STANDARD ATE DIGITAL CHANNELS

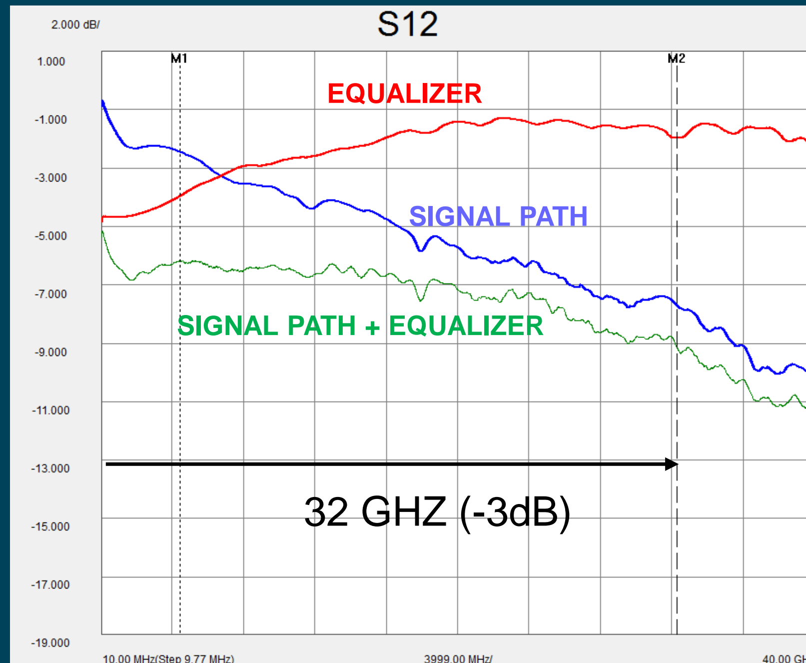
STANDARD DUT POWER SUPPLIES

HIGH CURRENT DUT POWER SUPPLIES



ATE UTILITY CHANNELS

Signal Path Equalization



Signal path to the comparator/driver module including a DUT test fixture with a 2.3 cm, 8.4 mil (0.215 mm) wide trace microstrip to a MMPX coaxial connector

- Even using state of the art materials and design techniques the cable and PCB loss dominate the signal path loss.
- Because of this a passive coaxial equalizer was developed and integrated on the solution.

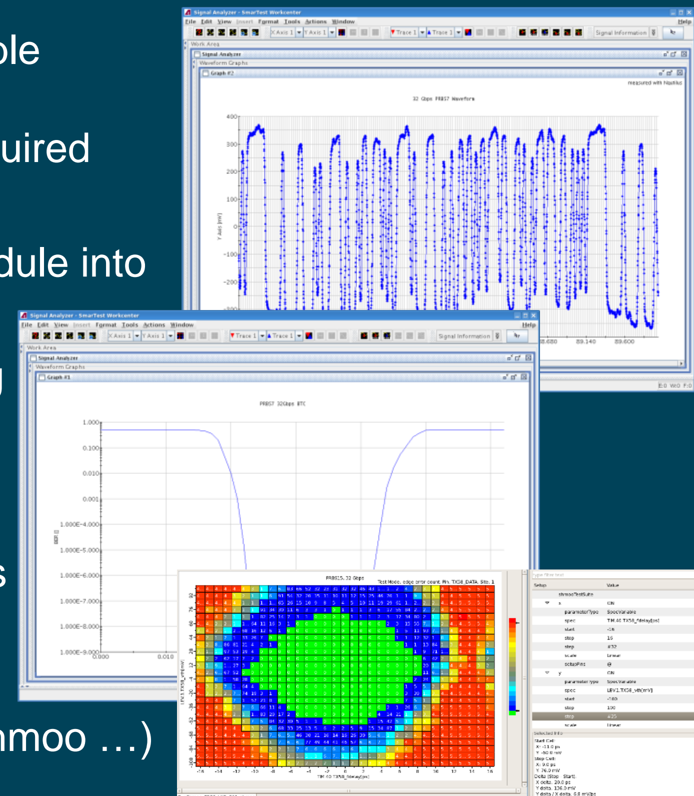
REFERENCES [3]

Docking and Test Cell Integration

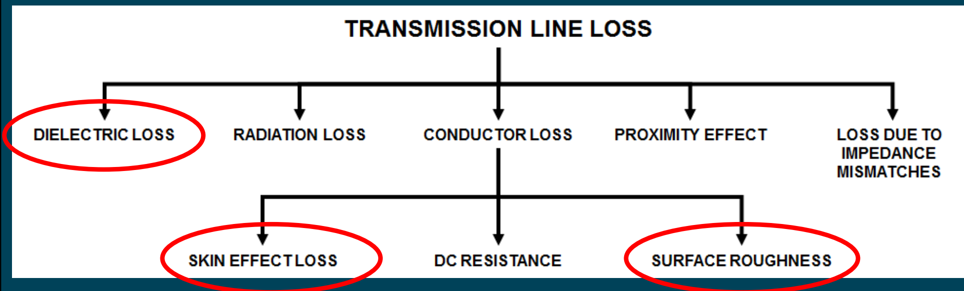
- An adjustable adapter was develop to keep the standard ATE test cell hard docking configuration.
- This allows that a standard handler or prober docking plate is used.

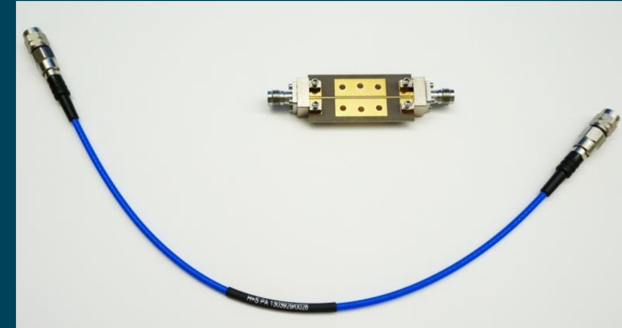
SW Integration Challenges

- Add-on module has to have the look and feel of an integrated ATE instrument
  - All operations based on DUT pin references (switch matrix hidden from user)
  - Integration of level and timing resource control into ATE software timing and level equation systems
  - Typical SerDes tests have to be available as library test functions
  - Automatic calibration data handling required
- API layer integrates access to add-on module into standard ATE programming environment
  - APIs integrate calibration data handling and resolve DUT centric user interface to real ATE resources used to control add-on module
  - Standard tests implemented using APIs
- Level and timing control signals are fully integrated into ATE equation system and allow usage of standard ATE tools (e.g. shmoo …)

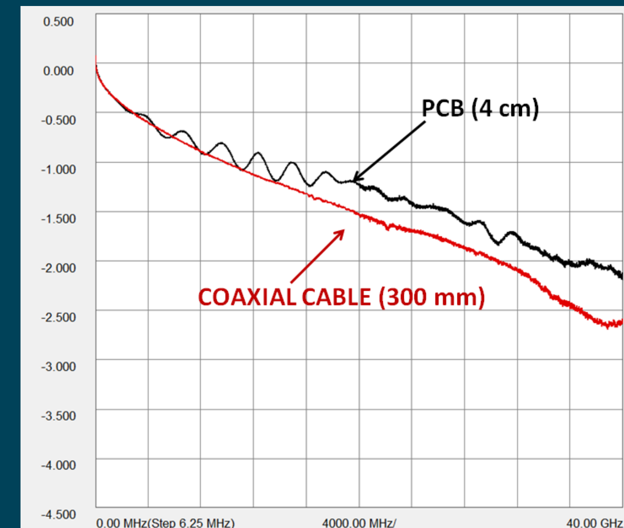


DUT Test Fixture PCB Challenges



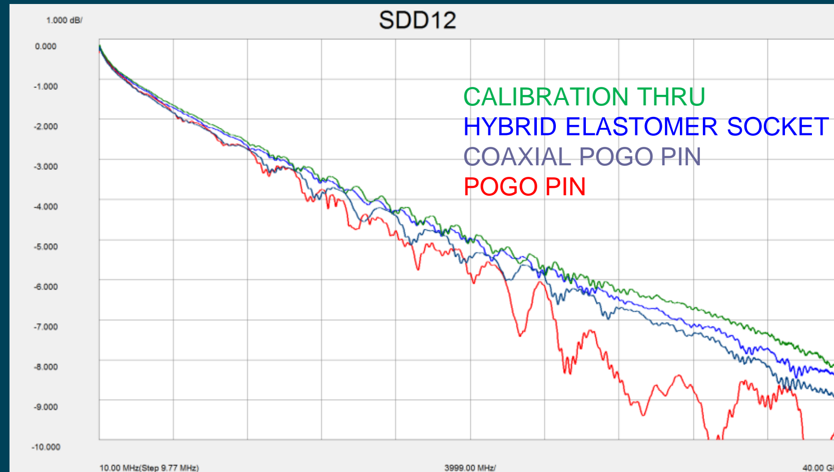


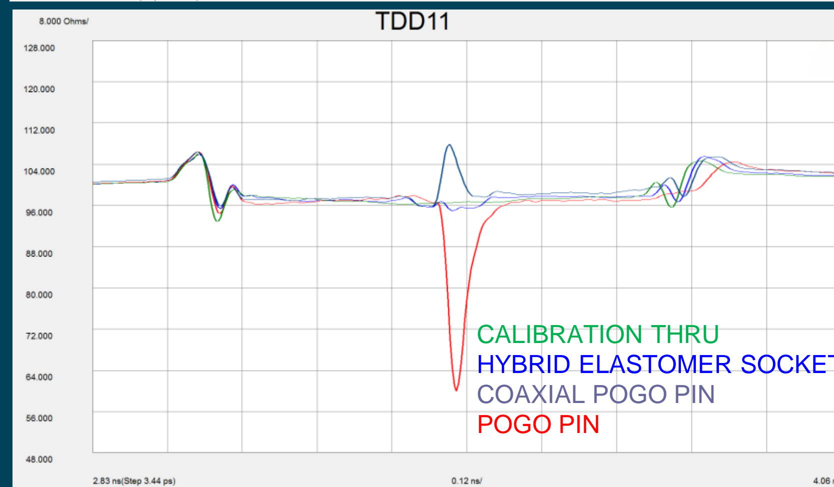
- The DUT PCB test fixture is the main loss contributor even compared with coaxial cabling.
- Main Items to be taken into account for 32 Gbps test fixture design:
  - Wide signal traces
  - Low loss dielectric material
  - Low profile copper
  - Approximately matching of the trace length to all I/Os to keep signal trace loss equal

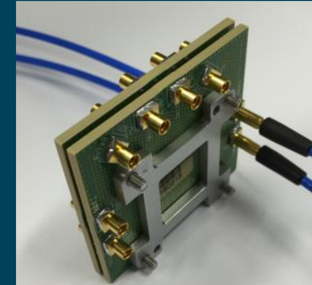


REFERENCES [3,4]

DUT Socket Challenges



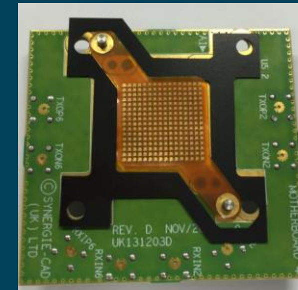




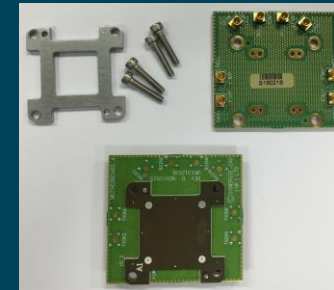
BGA BALLOUT

DUT PIN	GND	TX1
DUT PIN	GND	TX1
GND	TX0	GND
GND	TX0	GND
GND	POWER	GND

ELASTOMER



COAXIAL POGO PIN

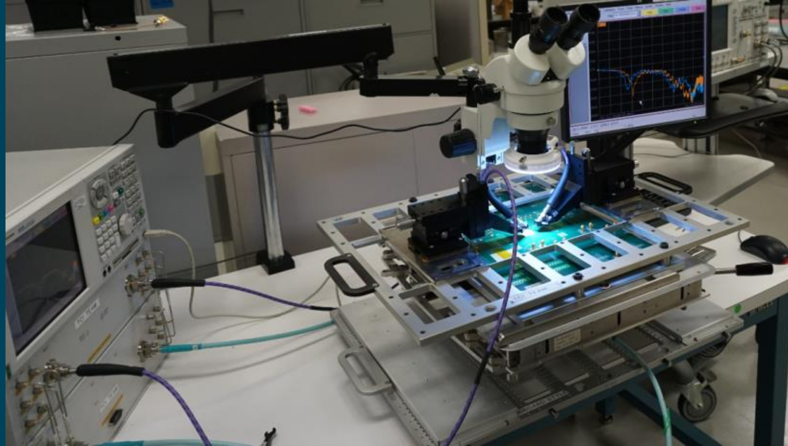


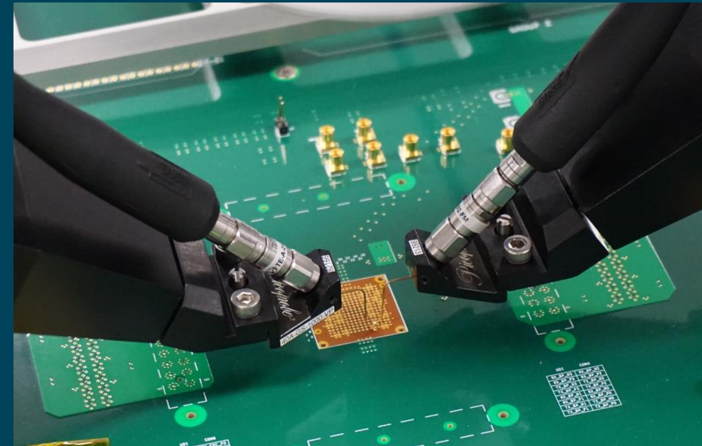
Different Socket Styles:
- **Standard Pogo Pin**
- **Coaxial Pogo Pin**
- **Elastomer**
- **Hybrid**

Production worthiness and reliability versus parametric performance.

REFERENCES [3,4]

Test Fixture Evaluation



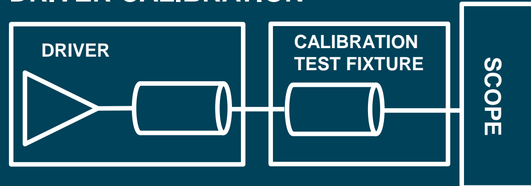


- It is critical to characterize the DUT test fixture before using it on the ATE system.
- Not only for the signal path performance but also for correlation between the different lanes
- To make it easier a bench setup with the high-speed DUT test fixture interconnect was created with coaxial connectors.
- Do not forget that power integrity is critical and should also be measured.

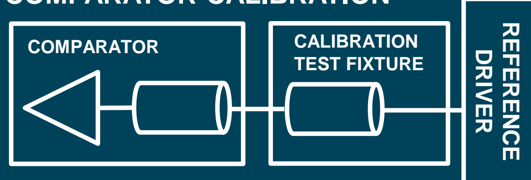
REFERENCES [3,5,6,7]

Calibration Strategy and Challenges

DRIVER CALIBRATION

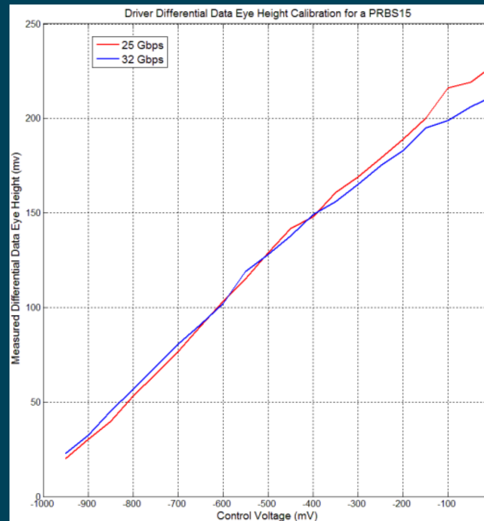


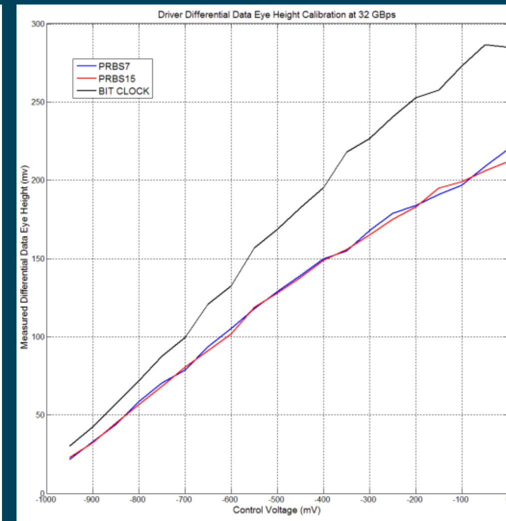
COMPARATOR CALIBRATION



Three types of calibration are required:

- DC calibration
- Setup/Hold Calibration
- AC Calibration (Data Rate and Pattern)



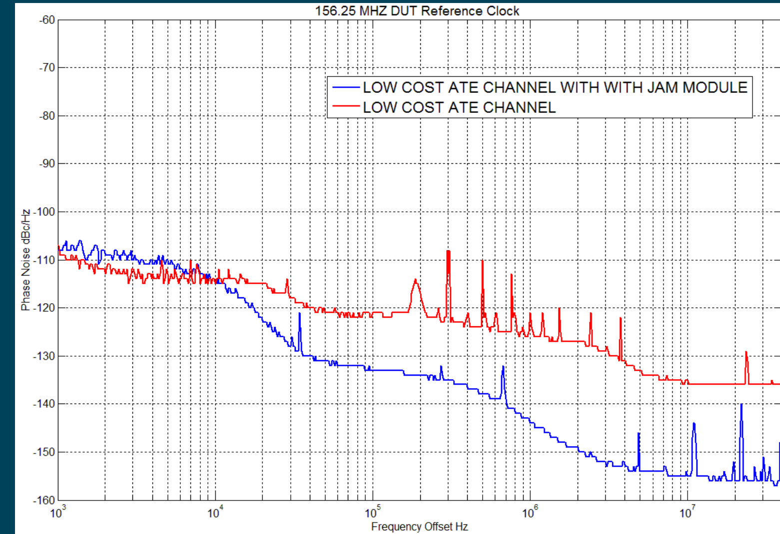


BiTS 2016 China Burn-in & Test Strategies Workshop

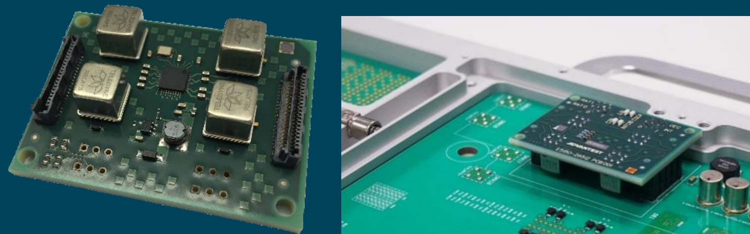
Implementation Challenges of an ATE Test Cell for At-Speed Production Testing of 32 Gbps Applications 13

DUT Reference Clock

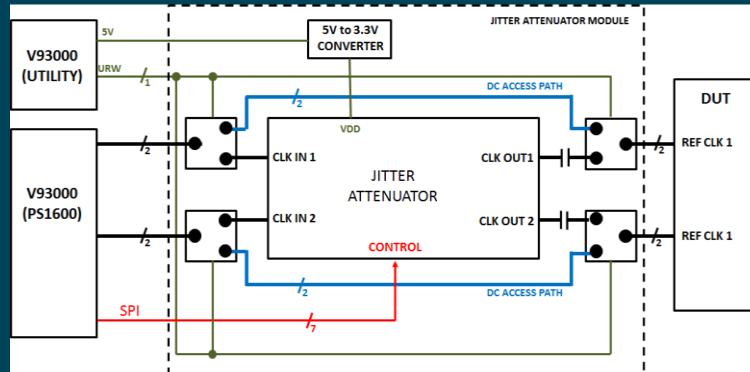
- A very low jitter DUT reference is critical.
- Using a low jitter ATE channel or an external reference clock is not cost effective.
- Solution is to use a low cost ATE channel and a "Jitter Attenuator" module based on a off the shelf Silicon Labs Si5236 IC.



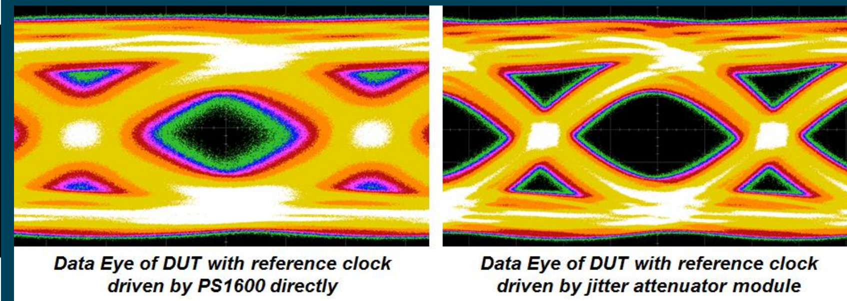
JITTER ATENUATOR MODULE



HIGH-LEVEL BLOCK DIAGRAM



DATA EYE DIAGRAM IMPACT



Data Eye of DUT with reference clock driven by PS1600 directly

Data Eye of DUT with reference clock driven by jitter attenuator module

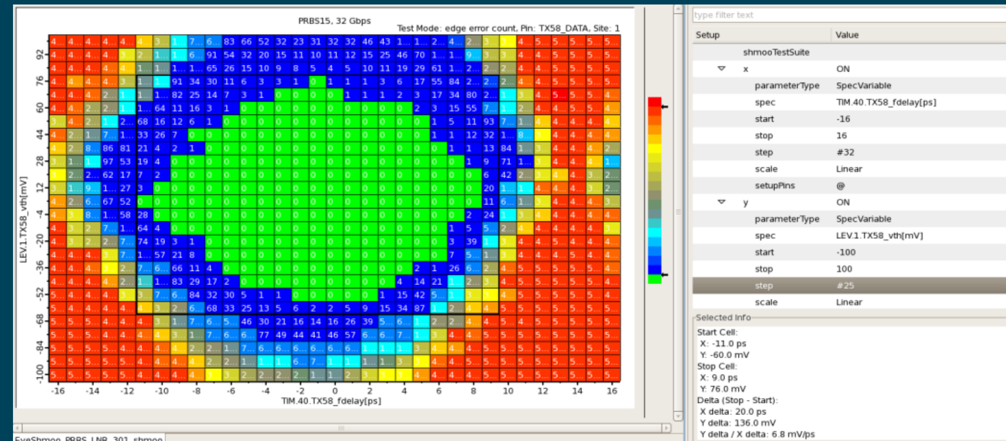
REFERENCE [8]

Driver/Comparator Performance (32 Gbps, PRBS15)

Measurement		Current	Minimum	Maximum	Count
Eye Width[Time]	D3A	24.125 ps	23.805 ps	24.235 ps	589
Eye Height[Ampl]	D3A	201.5 mV	199.9 mV	201.9 mV	589
Jitter[p-p]	D3A	7.8495 ps	5.4185 ps	8.7530 ps	587

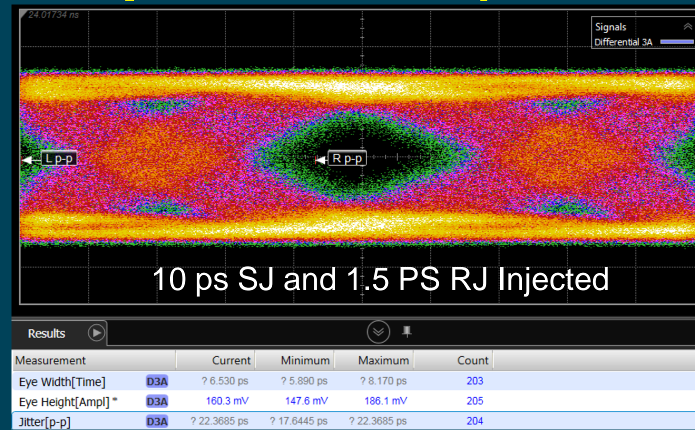
Measurement		Current	Minimum	Maximum	Count
Eye Width[Time]	D3A	24.150 ps	24.135 ps	24.810 ps	542
Eye Height[Ampl]	D3A	49.36 mV	49.28 mV	49.66 mV	547
Jitter[p-p]	D3A	8.1275 ps	5.6270 ps	8.1275 ps	548

LOOPBACK DATA EYE (Measurement includes a loopback PCB test fixture)

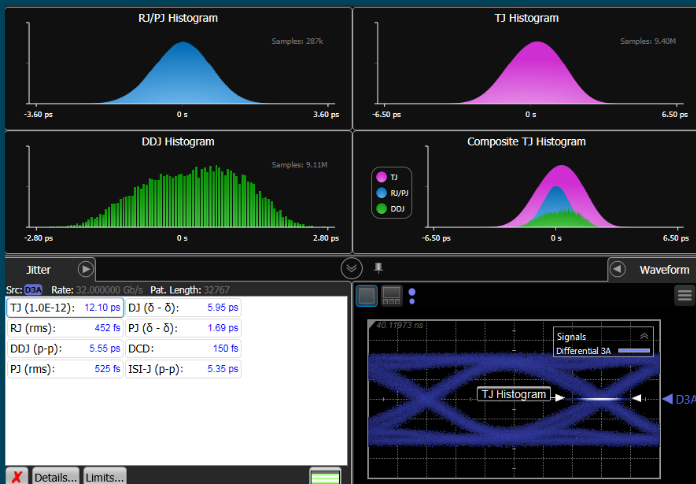


Jitter Injection (32 Gbps, PRBS15)

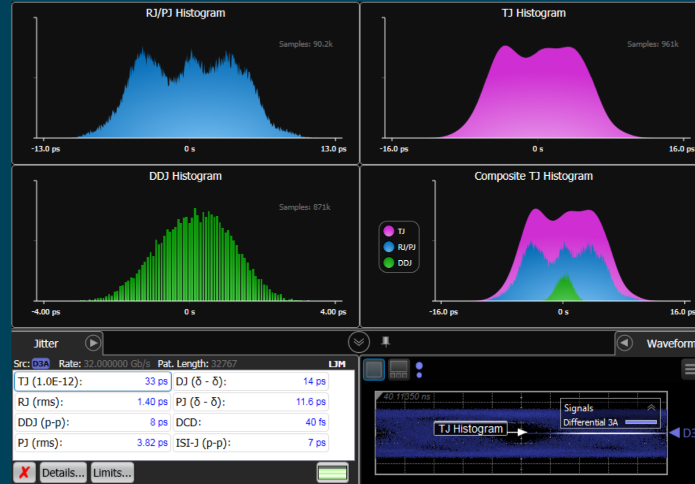
Measurement		Current	Minimum	Maximum	Count
Eye Width[Time]	D3A	24.125 ps	23.805 ps	24.235 ps	589
Eye Height[Ampl]	D3A	201.5 mV	199.9 mV	201.9 mV	589
Jitter[p-p]	D3A	7.8495 ps	5.4185 ps	8.7530 ps	587



Measurement		Current	Minimum	Maximum	Count
Eye Width[Time]	D3A	? 6.530 ps	? 5.890 ps	? 8.170 ps	203
Eye Height[Ampl] *	D3A	160.3 mV	147.6 mV	186.1 mV	205
Jitter[p-p]	D3A	? 22.3685 ps	? 17.6445 ps	? 22.3685 ps	204



TJ (1.0E-12):	12.10 ps	DJ (δ - δ):	5.95 ps
RJ (rms):	452 fs	PJ (δ - δ):	1.69 ps
DDJ (p-p):	5.55 ps	DCD:	150 fs
PJ (rms):	525 fs	ISI-J (p-p):	5.35 ps



TJ (1.0E-12):	33 ps	DJ (δ - δ):	14 ps
RJ (rms):	1.40 ps	PJ (δ - δ):	11.6 ps
DDJ (p-p):	8 ps	DCD:	40 fs
PJ (rms):	3.82 ps	ISI-J (p-p):	7 ps

Conclusions

- A cost effective high performance solution for at-speed testing of I/O interfaces to data rates of 32 Gbps was presented.
- There is always a complex trade-off between number of measurement channels, performance, test time and cost.
- For applications with more than 16 lanes there are two possible options:
  - Multiple insertions with different test fixtures.
  - Selection of 16 lanes that represent the I/O overall performance.
- To keep development and integration costs low it is critical to make the solution as transparent as possible in regards to test cell integration and also to SW usage.
- The DUT test fixture PCB and socket design is the performance bottleneck. It is critical to keep the PCB signal traces length as short as possible.

References

- [1] Jose Moreira, Bernhard Roth, Hubert Werkmann, Lars Klapproth, Michael Howieson, Mark Broman, Wend Ouedraogo and Mitchell Lin, “An Active Test Fixture Approach for 40 Gbps and Above At-Speed Testing Using a Standard ATE System”, IEEE Asian Test Symposium 2013.
- [2] Jose Moreira, Fabio Pizza, Christian Borelli, Fulvio Corneo, Hubert Werkmann, Sui-Xia, Daniel Lam, Bernhard Roth, “A Pragmatic Approach for At-Speed Characterization and Loopback Correlation at 28 Gbps“,Advantest VOICE 2014.
- [3] Jose Moreira and Hubert Werkmann, “An Engineers Guide to Automated Testing of High-Speed Interfaces”, Second Edition, Artech House 2016.
- [4] Jose Moreira, Christian Borelli and Fulvio Corneo “PCB Test Fixture and DUT Socket Challenges for 32 Gbps/Gbaud ATE Application”. BITS 2015.
- [5] Heidi Barnes, Jose Moreira, Abraham Islas, Michael Comai, and Francisco Tamayo-Broes, Orlando Bell, Mike Resso, Antonio Ciccomancini and Ming Tsai, Performance at the DUT: Techniques for Evaluating the Performance of an ATE System at the Device Under Test Socket”, DesigCon 2009.
- [6] Heidi Barnes, Jose Moreira, Mike Resso and Robert Schaefer,“ Advances in ATE Fixture Performance and Socket Characterization for Multi-Gigabit Applications”, DesignCon 2012.
- [7] Jose Moreira, “Design of a High Bandwidth Interposer for Performance Evaluation of ATE Test Fixtures at the DUT Socket”, IEEE Asian Test Symposium 2012.
- [8] Hubert Werkmann, Jose Moreira, Sui-Xia Yang, “A DUT Reference Clock Jitter Attenuator Module for the V93000 ATE Platform “,Advantest VOICE Users Conference 2015.