
2nd Annual
BiTS
CHINA 中国
September 13, 2016
Keynote
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Keynote Address

BiTS China

Evolutions in Packaging Technologies for IoT – Assembly and Testing

Yifan Guo

Vice President

Advanced Semiconductor Engineering (ASE)

BiTS 2016 China Burn-in & Test Strategies Workshop

Keynote Address – Abstract & Biography

As the IoT applications become a more and more important part of people's life, packaging technologies are also evolved to meet the assembly and testing challenges for building the required semiconductor devices. In today's world, as the rapid expansions of IoT applications, typically presented by the mobile/wearable devices and networks, consumer products are high volume and low cost, small and power efficient. These applications impose requirements for highly integrated system solutions and associated new assembly and testing technologies. The SiP (System in Package) is one of the emerging technology for an effective packaging solution. In this presentation, the evolutions of packaging technologies in the IoT era is introduces. The SiP technology, assembly and testing processes and challenges are presented. The potential future packaging technology requirements and developments for IoT are discussed.

Yifan Guo is vice president of ASE Assembly and Test in Shanghai, ASE China. With over thirty years experience, he has performed roles in both academia and industry. He previously held positions as Professor and Adjunct Professor at Virginia Tech, State University of New York at Binghamton and University of California at Irvine. He has also worked for IBM, Motorola, Skyworks, ASE, in a variety of middle and high level management roles with responsibility for charges of R&D, engineering and operations. He holds nine patents and has published seven book chapters, and more than 50 refereed journal papers. Yifan Guo received his Ph.D degree from the Engineering Science and Mechanics (ESM) Department at Virginia Tech, and also holds an MBA from University of Redlands in California.

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Evolutions in IC Packaging Technologies for IoT

BiTS China 2016

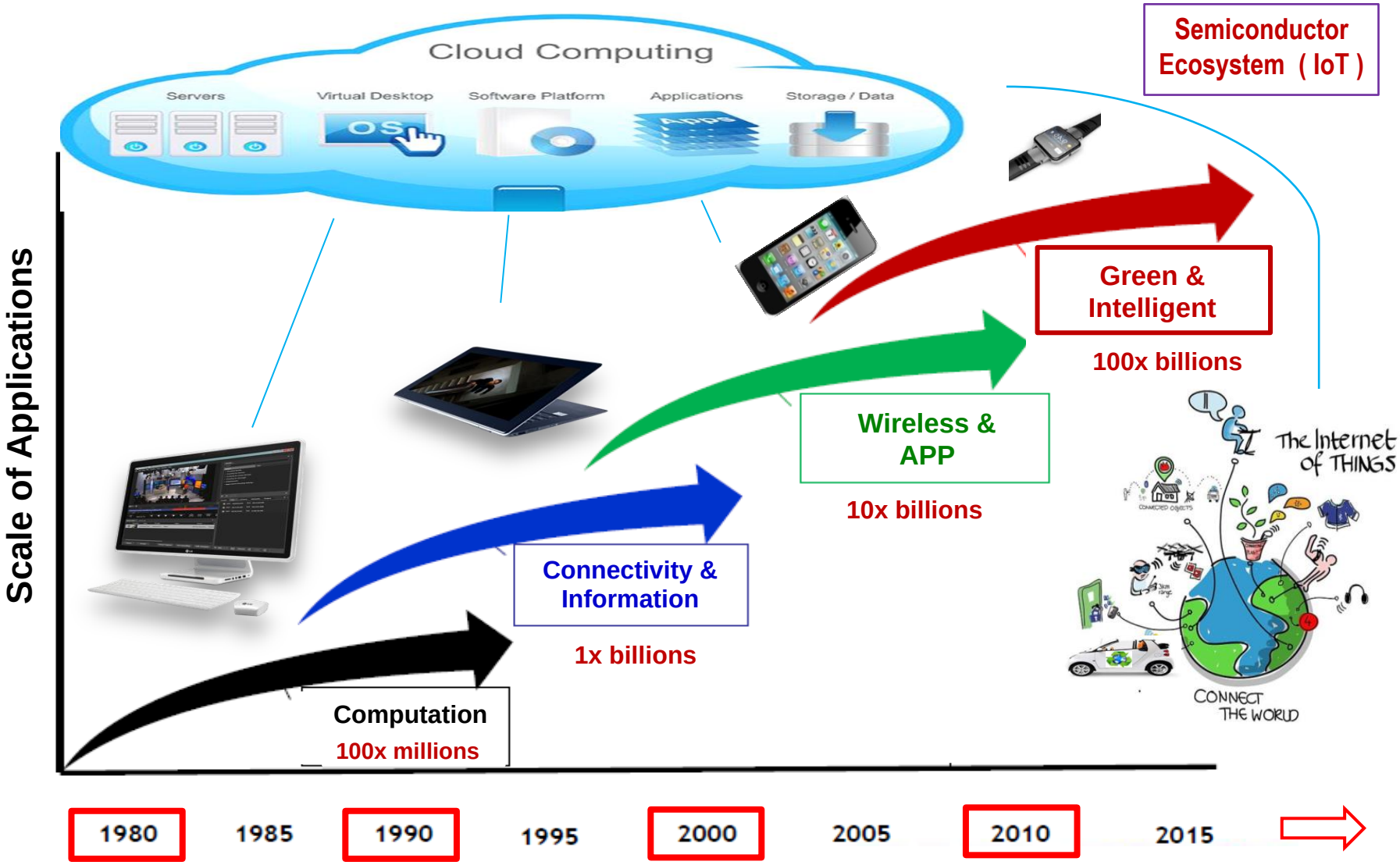
2016.09.13

Suzhou, China

《 Agenda 》

- Technology and Application Evolution
- Major Trends in Development and Demand
- Status and Challenges to Semiconductor A&T
- Summary

Paradigm Shift in Semiconductor Technology



Green and Intelligent are the key arears for next generations of development

Semiconductor Opportunities in IoT (CAAGR)

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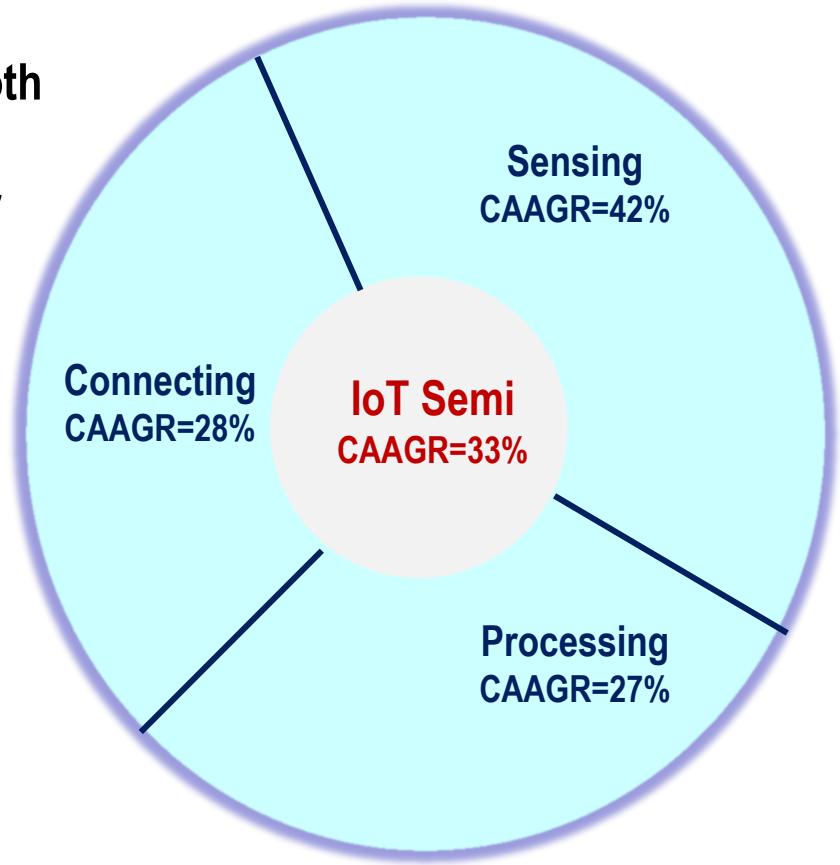
Connectivity

Connecting

- NFC
- Bluetooth
- WiFi
- Cellular
- ZigBee
- GPS



Intelligent

Sensing

- Image Sensor
- Pressure Sensor
- Humidity sensor
- Inertial Sensor
- Magnetic Sensor
- Chemical Sensor
- ……

Processing

- CPU
- Application Processor
- Micro-processor
- Micro-controller
- Memory

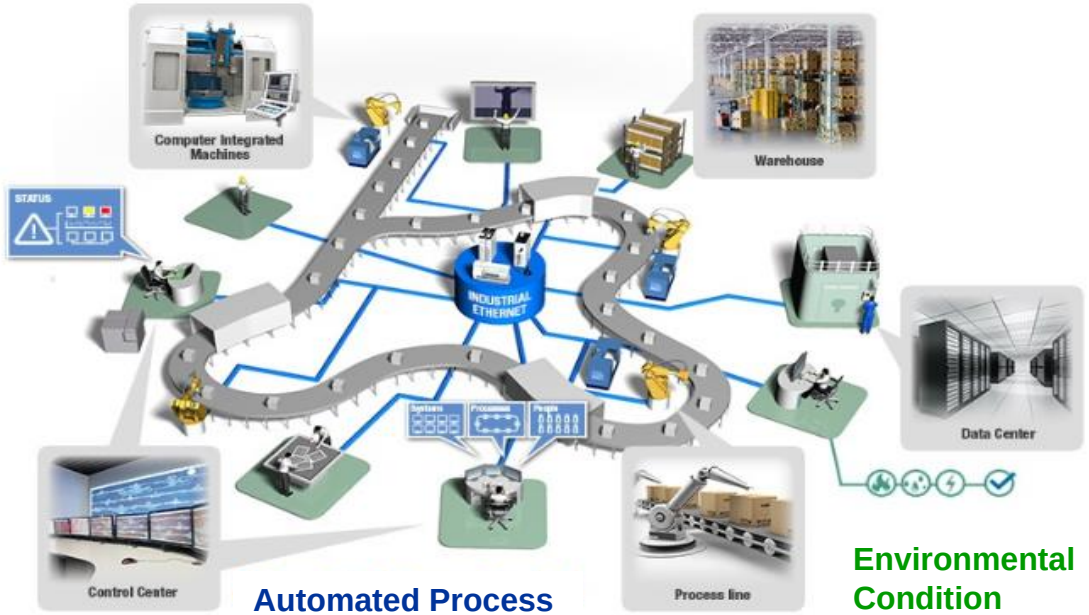
Generation of Semiconductor Technology

Green and Intelligent are the Key Areas

How to be "INTELLIGENT"?

Computer- Integrated Manufacturing

Real-Time Production Monitoring



Automated Process Control

Environmental Condition Monitoring

The Ultimate Challenge — Human Intelligence

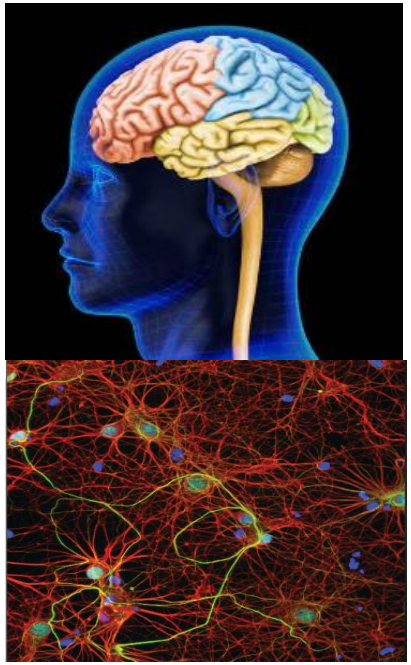
Semiconductor Technology has the Greatest Potential!

- AlphaGo beat Lee Se-dol (李世石)
- DeepMind rises the Semiconductor Technology and Artificial Intelligence to a new level
- Integrated circuits with programs use deep neural networks mimicking expert players and learning from games

Where Are We? — Competing with Human Brain

Human Brain

- 100B Neural Cells
- > 1M nerves (parallel connections)
- 3D structure
- ~ 20 W



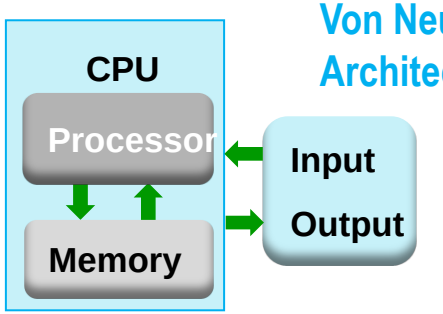
IBM Deep Blue

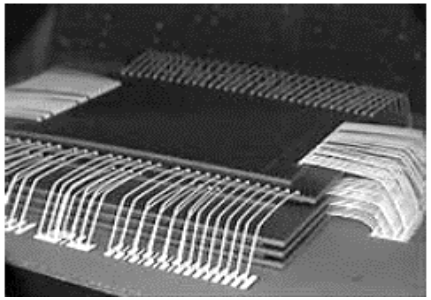
- 500B Transistors
- ?? Interconnects (serial connections)
- 2D structure
- ~ 2000 W
- Learning and mimicking ??

Differences are :

1. Speed is 1000 times slower
2. Power is 100 times greater
3. Size is ???
4. Cost

Von Neumann Architecture





Understanding of Human Brain Provides Direction for Semiconductor Development

We Need Breakthroughs in 3 Major Areas

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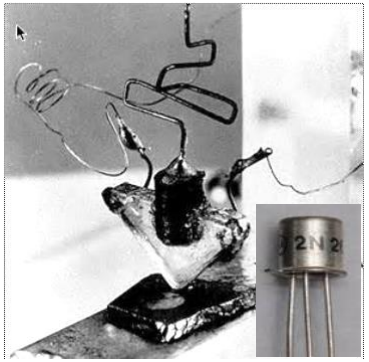
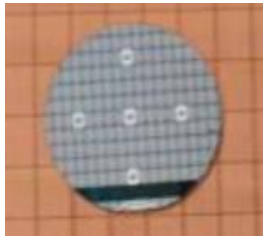
1. Higher **Speed**
2. Better **Efficiency (power)**
3. Smaller **Size**



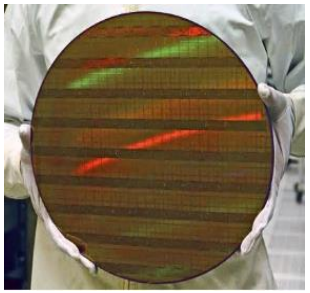
Point-contact transistor （1947） William B. Shockley AT&T

Integrated circuit (1958) Jack Kilby TI



Intel 4004 CPU 1972

- 10 um process
- 2,500 transistors



Intel Xeon Phi CPU 2013

- 14 nm process
- 5 billion transistors

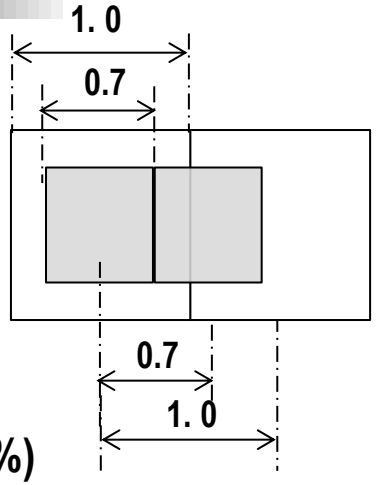
Si Technology to Address Speed, Efficiency and Size

Moore's Law and Physical Scaling :

Every technology generation (about 2 years) :

— Density increases by 2X , # transistors increase by 2X (size)

- Reducing area by 50% and linear dimension by 0.7X (30%)
- Reducing signal delay by 0.7X (30%), increasing speed by 1.4X (40%)
- Reducing voltage by 0.7X (30%), improving power efficiency by 1.4X (40%)



after 40 years

Generations	1	2	3	…	10	…	14	15	16	17	18	19	20	21
Node Size (nm)	10,000	7,070	4,998	…	441	…	110	80	55	40	28	20	14	10
# Transistors (K)	2.5	5	10	…	1,280	…	20,480	40,960	81,920	163,840	327,680	655,360	1,310,720	2,621,440
Speed (MHz)	1	1.4	2	…	21	…	79	111	156	218	305	427	598	837

✓ Intel 4004, 1972
✓ 10 um
✓ 2.5 K Transistors
➢ 1 MHz

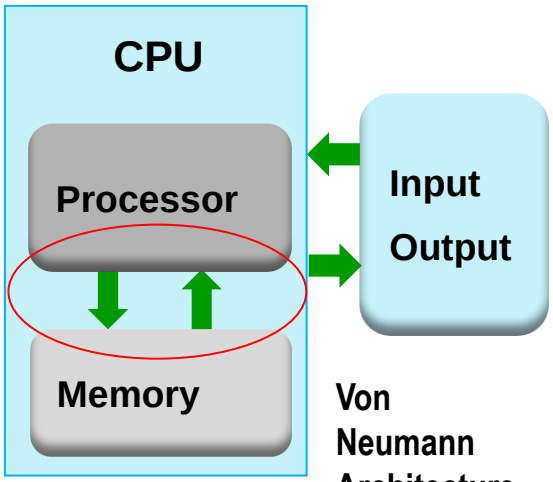
- # Trans. ↑ 1 M x
- Speed ↑ 1 K x

✓ Xeon Phi, 2013
✓ 14 nm
✓ 5 B Transistors
➢ 1.3 GHz

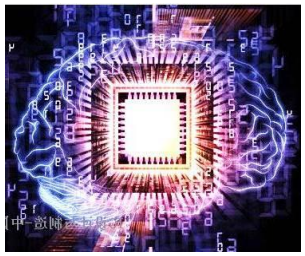
After 40 years, chip is much advanced, but we still have 3 bottlenecks

Bottleneck 1 : Between Processor and Memory

Von Neumann Bottleneck in Processor and Memory



Von Neumann Architecture



Human Brain :

Processing + Memory

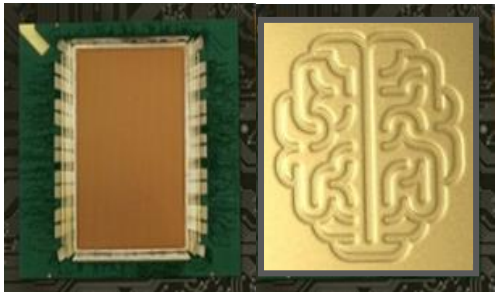
100B Neural Cells

Chip Technology:

IBM SyNAPSE:

Neuromorphic Chip

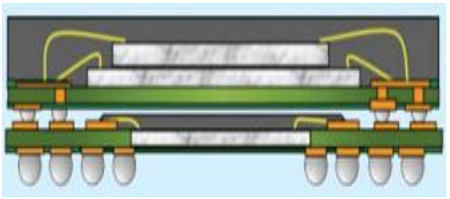
1 Million Neural Cells

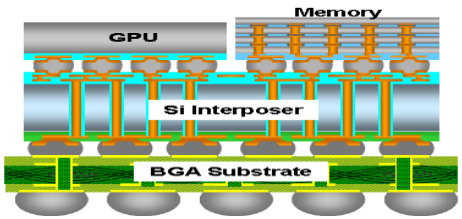


Chip Solution:
SyNAPSE : Systems of Neuromorphic Adaptive Plastic Scalable Electronics

Packaging Tech:

- ✓ Stack / Embed
- ✓ PoP
- ✓ TSV + 3D





Packaging Solution:

Move processor closer to memory with more I/Os

Bottleneck 2 : Between CPU and Interface

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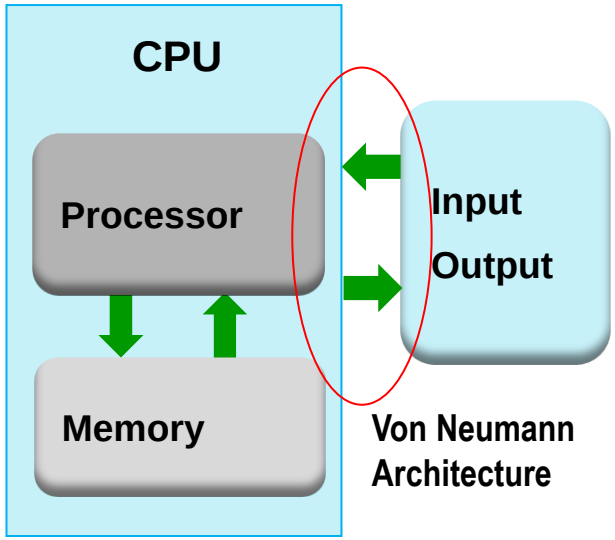
Von Neumann Bottleneck
in data input and output



Packaging Tech:

Bring CPU Closer to
in / output Interfaces

Chip Solution:
Move CPU closer to
User Interface

Packaging Solution:

- ***System Packaging***
- ***Wafer Level Packaging***

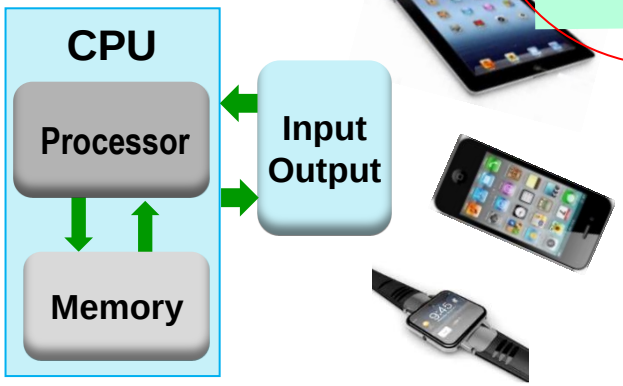
Bottleneck 3 : Data Transportation - Speed of Network

Data Processing

Bottleneck in Data Transportation

- FE Module
- Transceiver
- Base Band

User End



System Solution:
Wired & Wireless
Data Transport
3G, 4G, 5G …….

The Fan-Out Architecture of Working with the “Brain”

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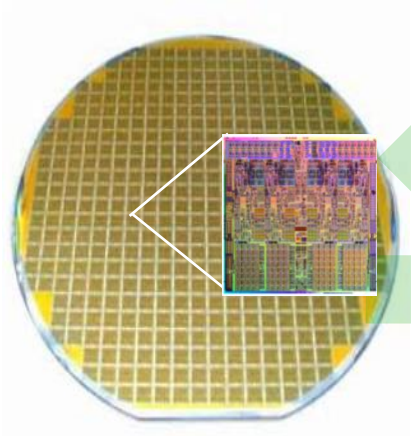
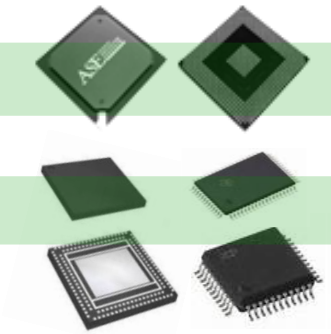
Design House (OEM)	Foundry	OSAT	EMS	EMS
	Level 0 Packaging	Level 1 Packaging	Level 2 Packaging	Application Level Pkg





Input

Output

End Product

Process	Device Level	Package Level	Board Level	User Interface
Dimension	nanometer(10^{-9} m)	micrometer(10^{-6} m)	millimeter(10^{-3} m)	Centimeter (10^{-2} m)

Efforts from Packaging Technologies

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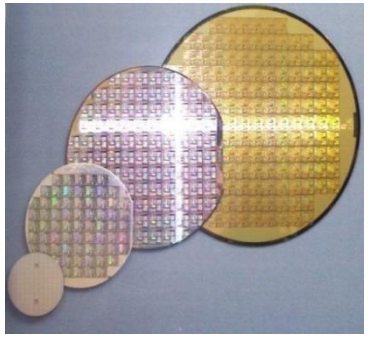
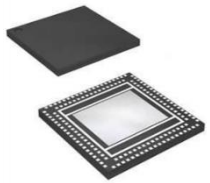
Level 0 → Level 1 → Level 2 → Level 3 → Level 4 → Level 5





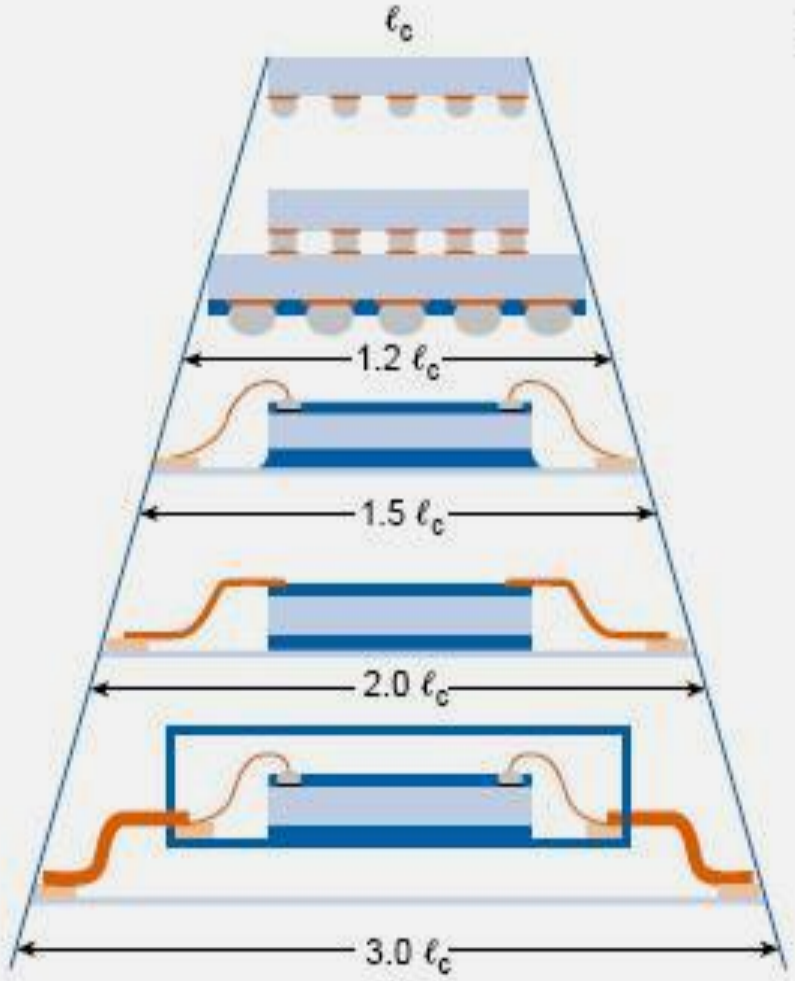
End Product
(user interface)

1. Speed; 2. Efficiency; 3. Size

— Eliminated Level 3 Packaging

Packaging Density Progression

(Package Size and Signal Path Length)



Technology	Area ratio: package/chip
Flip chip	1:1
Chip-scale package	1.5:1
Chip-on-board	2.25:1
Tape automated bonding	4.0:1
Quad-flat package	9.0:1

I/O Density Technology Improvement in Packaging

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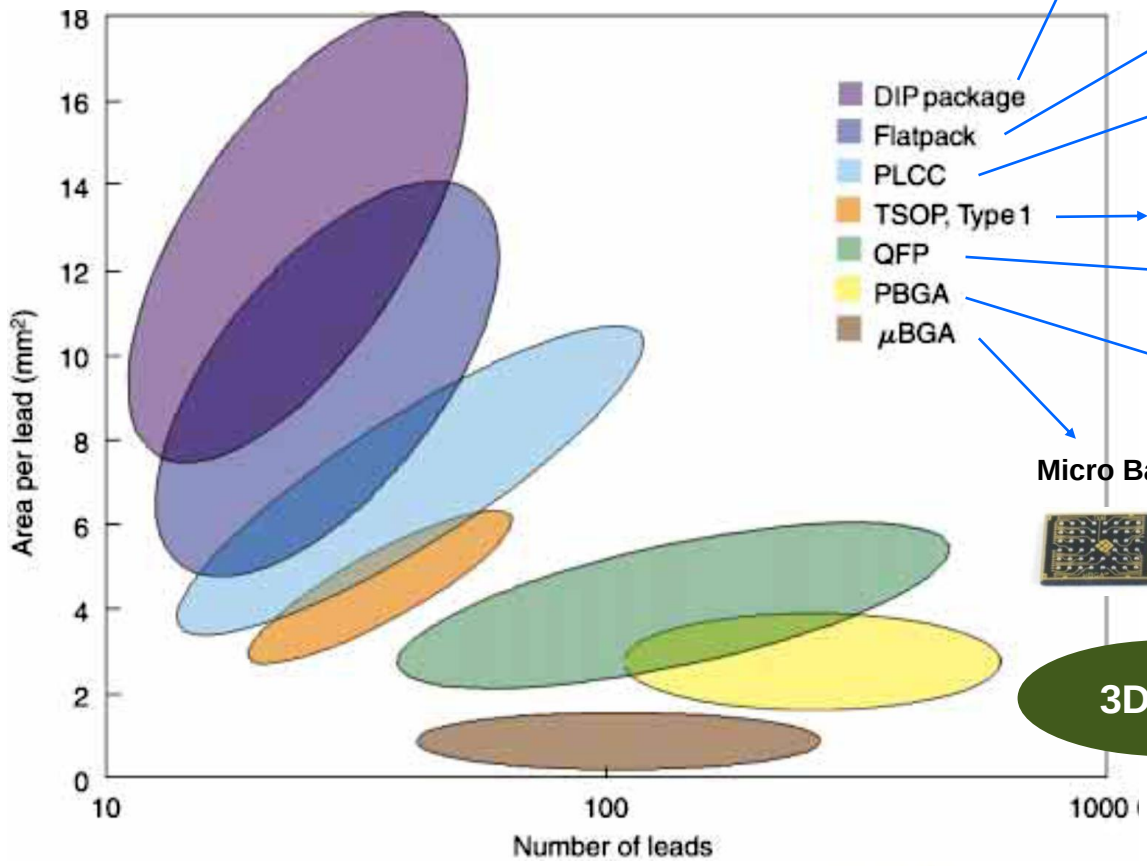
Increase of I/O # of Interconnects by new Packaging Technologies



Dual In-line Package

Flat Package

Plastic Leaded Chip Carrier

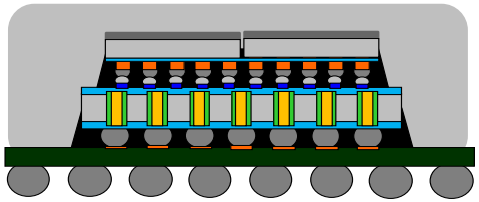
Quad Flat Package

Thin small-outline package

Plastic Ball Grid Array

Micro Ball Grid Array

3D TSV



Definitions of Advanced Packaging Technology

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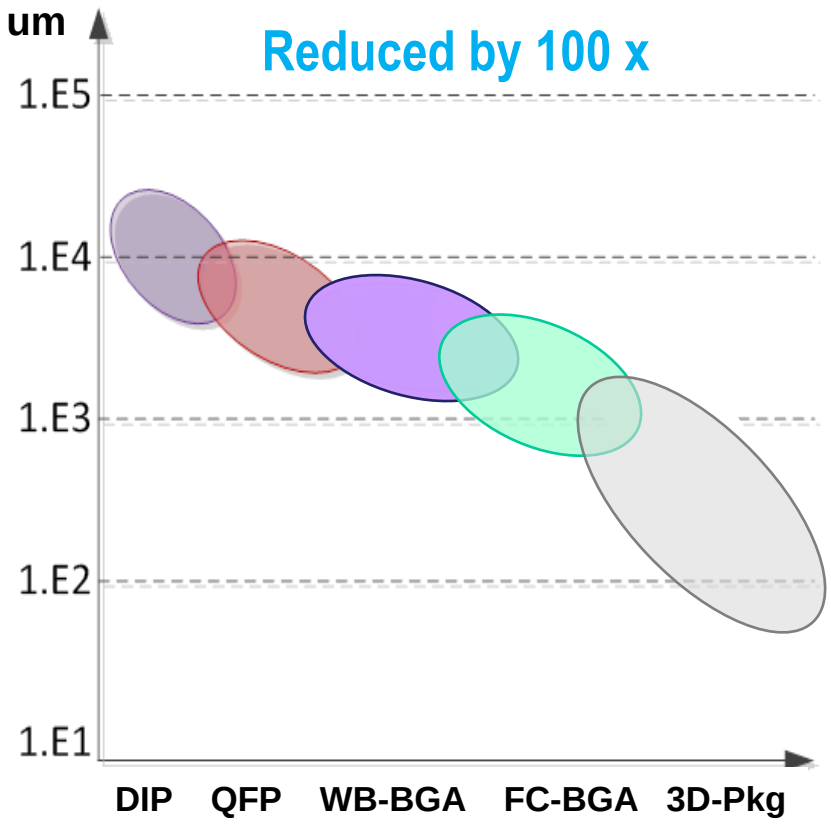
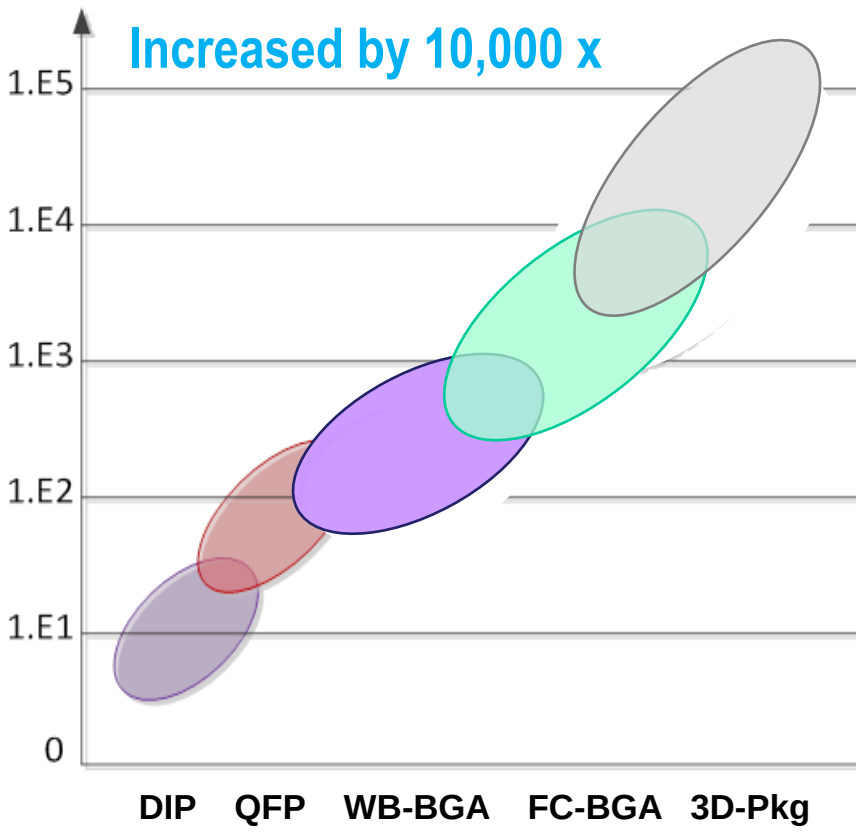
Signal Path Length in Packages



reduces signal delay

of Interconnects in Packages



parallel connections

3D and SiP High Density Technology Development

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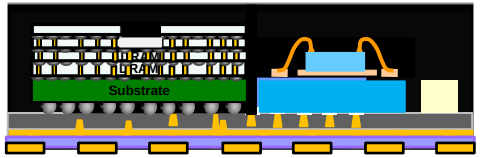
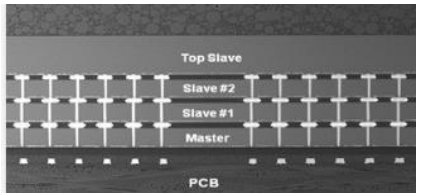
Heterogeneous Integration

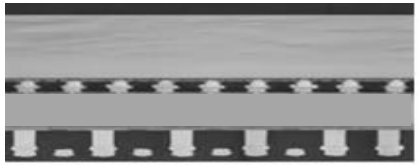
- **3D FOWLP**



- **3D TSV SiP**



- **2.5 D Interposer**



- **Embedded die**

High Density Interconnects

Packaging Feature Size – Packaging Moore's Law???

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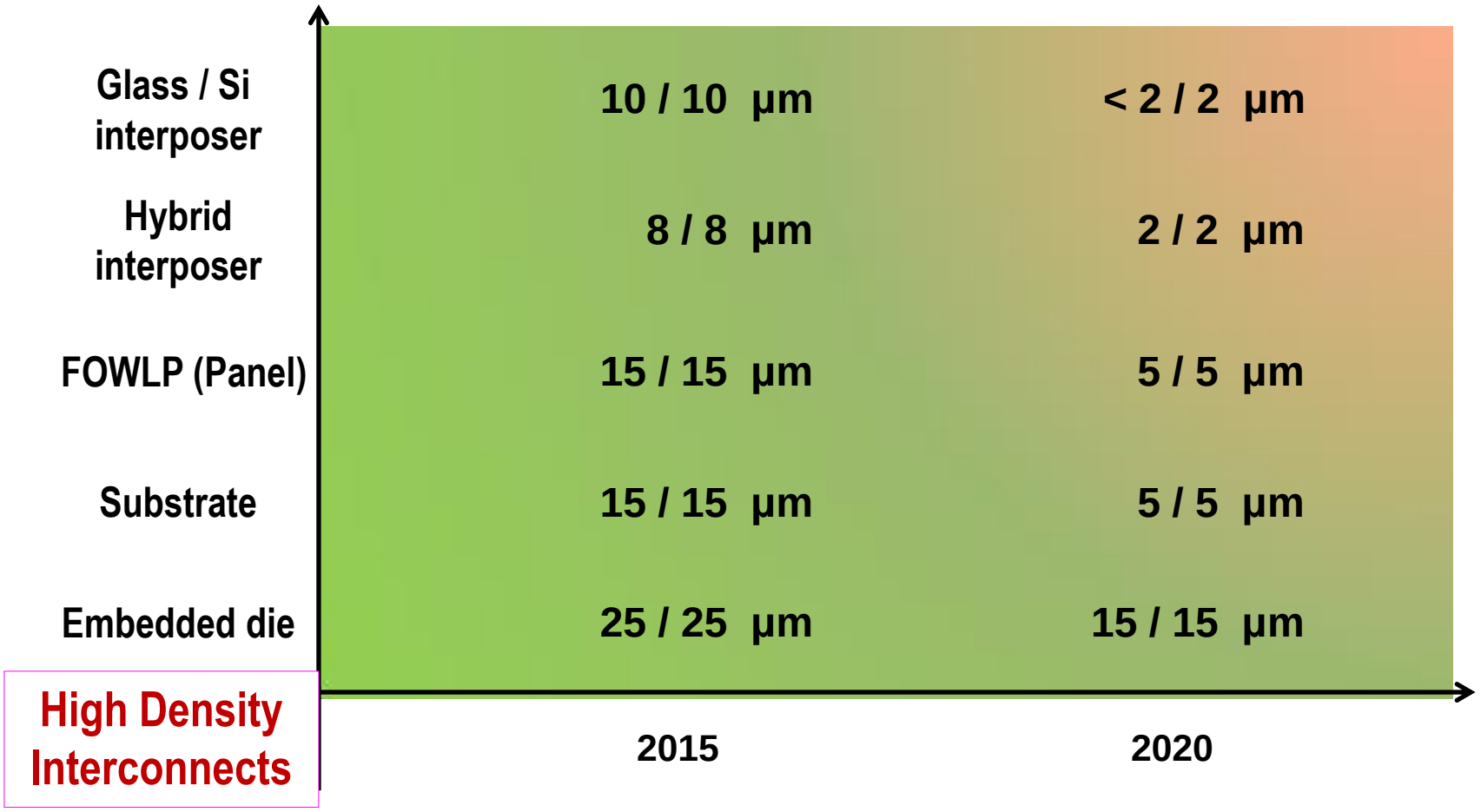
1970 → Line/Space Reduced by ≈ 1,000 X → 2020



High Density Interconnects

The Path of Evolution in Packaging Technologies

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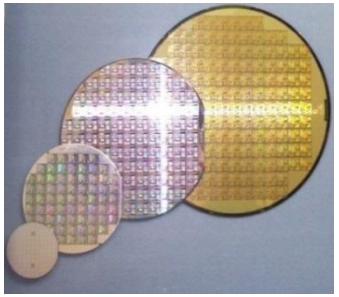
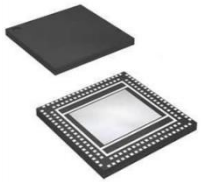
Level 0 → Level 1 → ~~Level 2~~ → ~~Level 3~~ → Level 4 → Level 5





End Product
(user interface)

Using System in Packaging (SiP)

— Eliminating Level 2 Packaging

Evolutions in IC Packaging Technology Development

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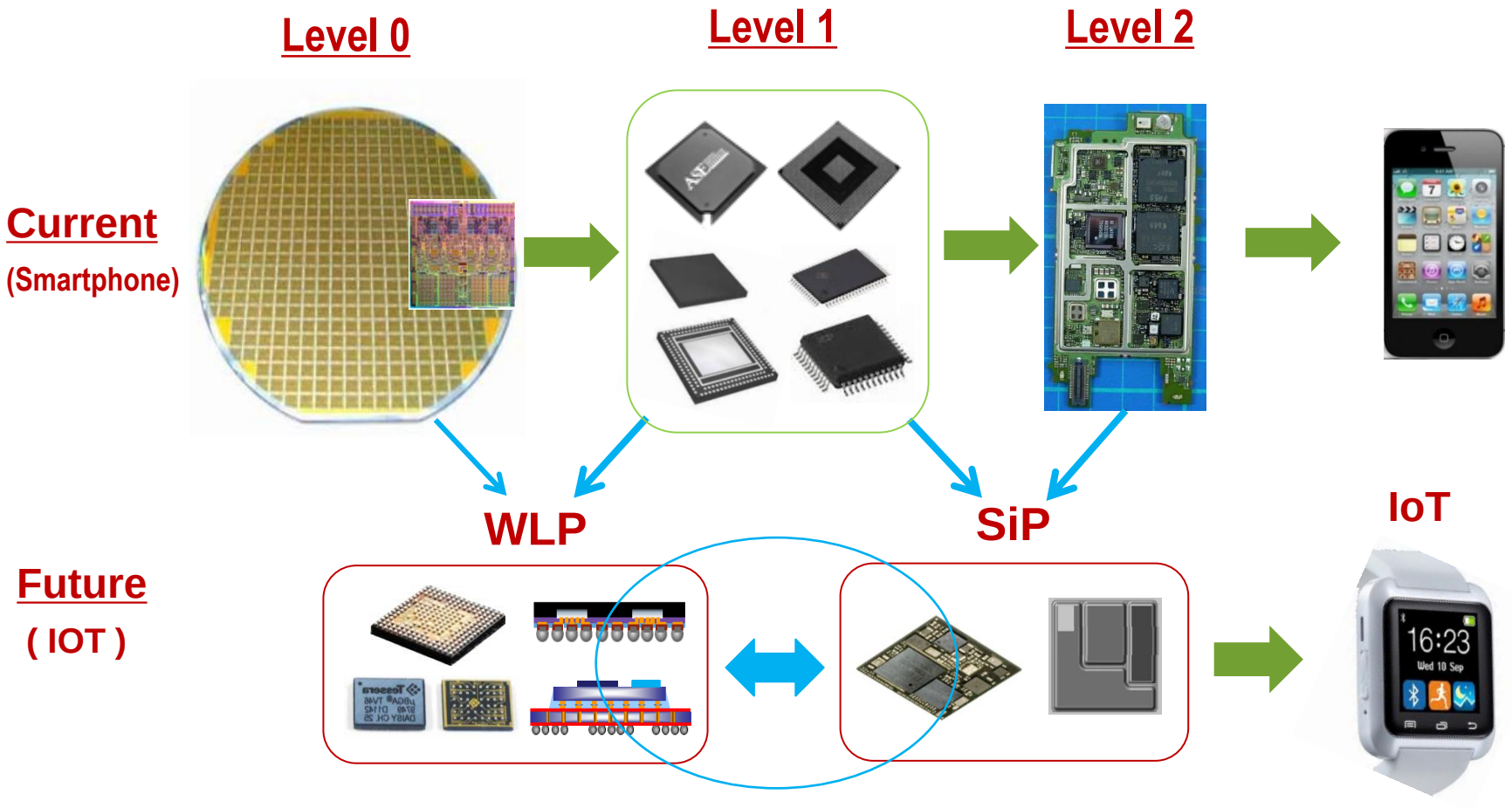

— Next System Integration ???

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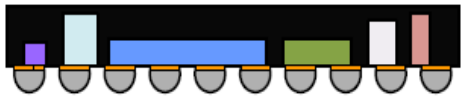
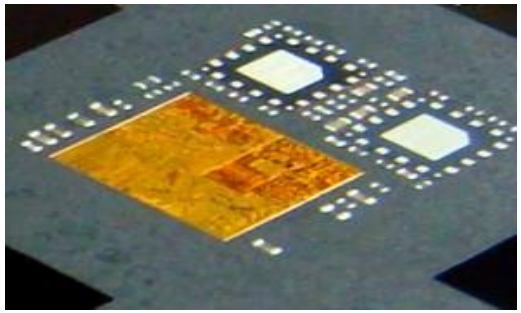
Heterogeneous Integration using FOWLP

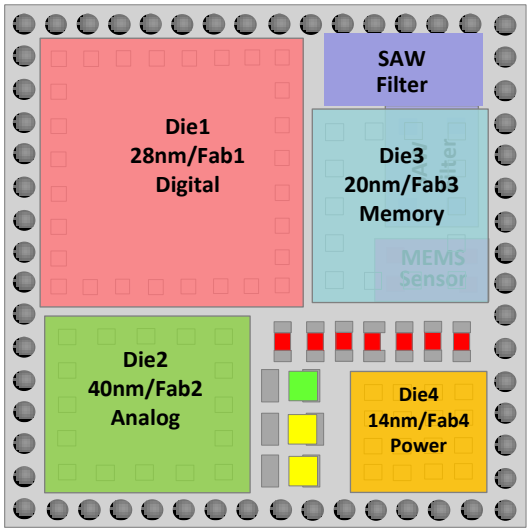
2D Multi Dies FOWLP

3D Multi Dies and Passives FOWLP

2D Multi Dies and Passives FOWLP







Characteristics of IoT Solutions — Requirements to Electronic Packaging

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- Holistic design and customization – a complete system
  - Operating SW, processor, memory, transmit, power, security ….
- Heterogeneous Integration
  - Digital, analog, mixed, Si, GaAs, MEMS, optics ….
- Miniaturization and Low Cost
  - WLP, SiP, IPD, stacking, embedding, shielding, CP molding ….
- Ecological System, Multi-Standards
  - Regional specs, local regulations, security and reliability ….

Challenges

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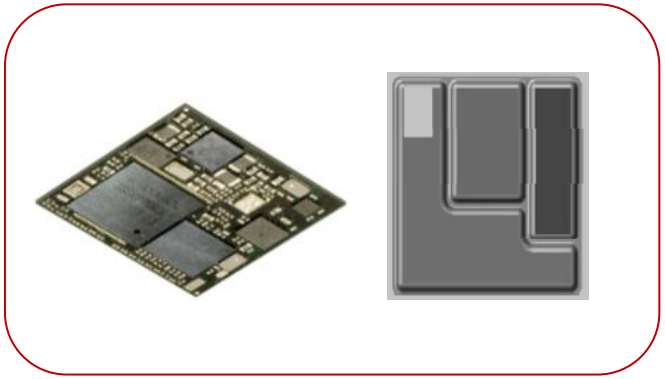
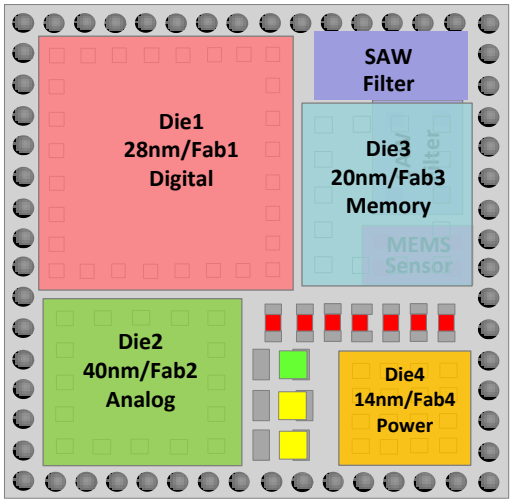
- **Performance Challenge:**
  - Design and simulation becomes more complicated
  - Electrical, thermal and mechanical cross-effect
- **Test Challenge:**
  - Multi layers of functions and assembly process flow require multiple test steps, burn-in and retest
- **Yield and Reliability Challenge:**
  - Complex design, process and materials systems affecting yield
  - Higher reliability requirement for special applications and user conditions
- **Tooling and Equipment Challenge:**
  - Verities of designs require customized tooling and equipment
- **Low Cost Challenge**

Advanced System in Package (SiP)

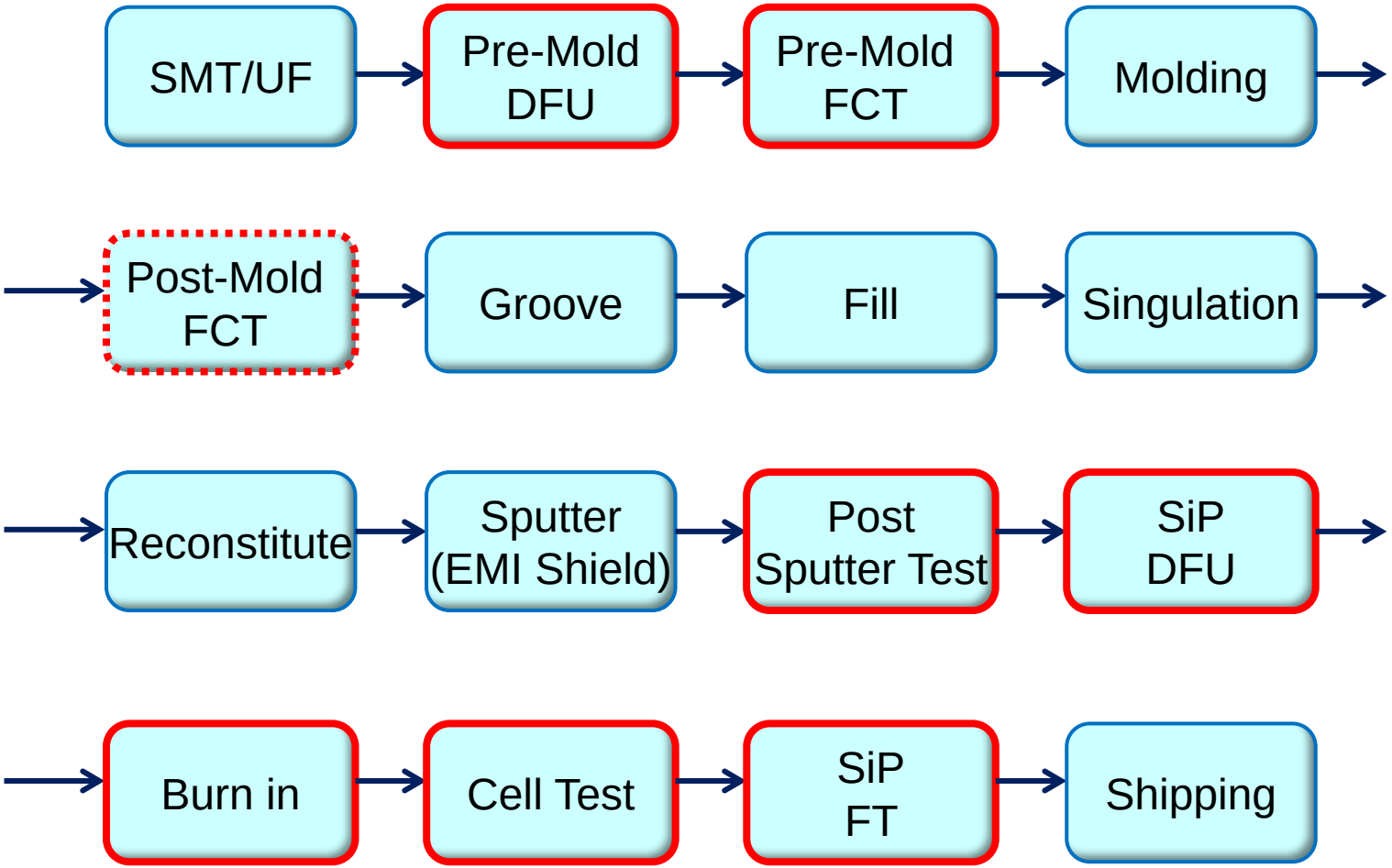
A big step toward IoT (wearable) applications





- Integrating Digital, Analog, RF FEM, PMIC, Memory, Sensors…
- Employed many state of art packaging technologies
- Used many new packaging processes and materials
- Very high density interconnects and L/S with many functions

A Typical SiP Assembly / Test Flow (key steps)



(could be more than 50 A&T process steps)

Challenges in Testing of SiP

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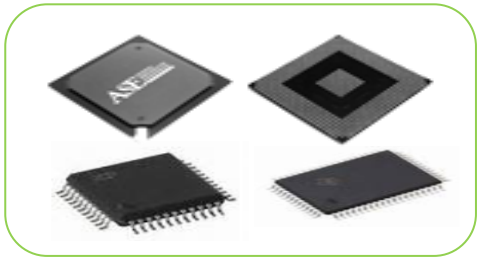
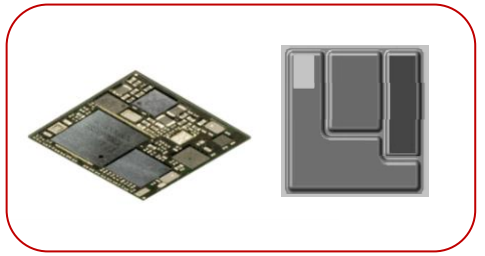
- Past: BGA, QFN, SO
  - CP (or blind build) + FT + (system level tests)



- Current: 3D + SiP
  - PCB + CP + FCT 1,2,3…+ Burn-in + FT



- Future: 3D + SiP + FOWLP
  - How to Test ???

Next Generation of Testing Technology

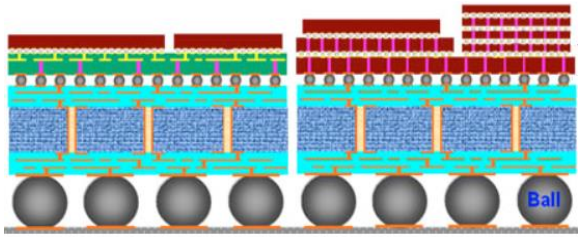
ASE GROUP

For highly integrated systems, test becomes more critical !

We know how to build it
But how we test it ?

- **Yield**
- **Reliability**
- **Cycle time**
- **Cost**

Testing



◆ **Burn-in and Test will take more important role and higher cost portion in A&T for IoT applications**

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Thank You