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BiTS
TM
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 8
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BiTS Burn-in & Test Strategies Workshop 2016

Session 8

Jason Mroczkowski
Session Chair

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 9 - 10:30 am

Cell-ebrating Test Too

"Modeling Socket Thermal Performance Inside a Burn-In Chamber"

Jason Cullen – Plastronics
Rob Caldwell - Delta V Instruments

"Established the first WLCSP Testing at Tri-temp for RF and Non-RF Products"

Edwin Valderama & Jin Sheng Tan -Intel Technologies

"A Silicon Photonics Wafer Probing Test Cell"

Roberto Aranzulla, Daniele Sala, Roberto Barbon - ST Microelectronics
Giuseppe Astone, Maurizio Rigamonti, Massimo Galli - ST Microelectronics
Jean Luc Jeanneau, Dario Adorni, Paul Mooney - Tokyo Electron
Hubert Werkmann, Fabio Pizza - Advantest Europe GmbH
Jose Moreira, Zhan Zhang - Advantest

BiTS Burn-in & Test Strategies Workshop 2016

A Silicon Photonics Wafer Probing Test Cell

Massimo Galli[1], Maurizio Rigamonti[1], Giuseppe Astone[1], Roberto Barbon[1] Daniele Sala[1], Roberto Aranzulla[1], Paul Mooney[2], Dario Adorni[2], Jean Luc Jeanneau[2], Yasuhiro Osuga[2], Hidekazu Shibata[2], Jose Moreira[3], Hubert Werkmann[3], Zhan Zhang[3], Fabio Pizza[3]

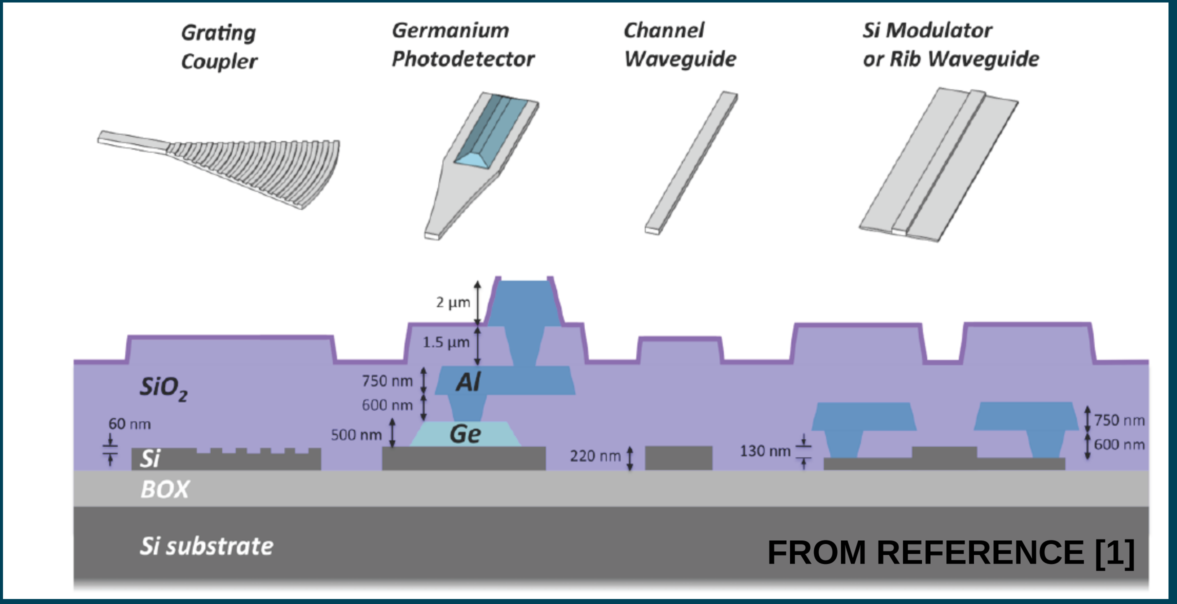
[1]ST Microelectronics, [2]Tokyo Electron, [3]Advantest

2016 BiTS Workshop
March 6 - 9, 2016

Presentation Outline

- Silicon Photonics
- Test Requirements
- Probing Challenges
- Volume Production Challenges
- Test Cell
- Software Requirements
- Conclusions

Silicon Photonics CMOS Line Process



- Silicon photonics design can now be manufactured using a standard CMOS line (except the laser).
- This opens silicon photonics to the same cost structure advantages that standard CMOS ICs have benefited.

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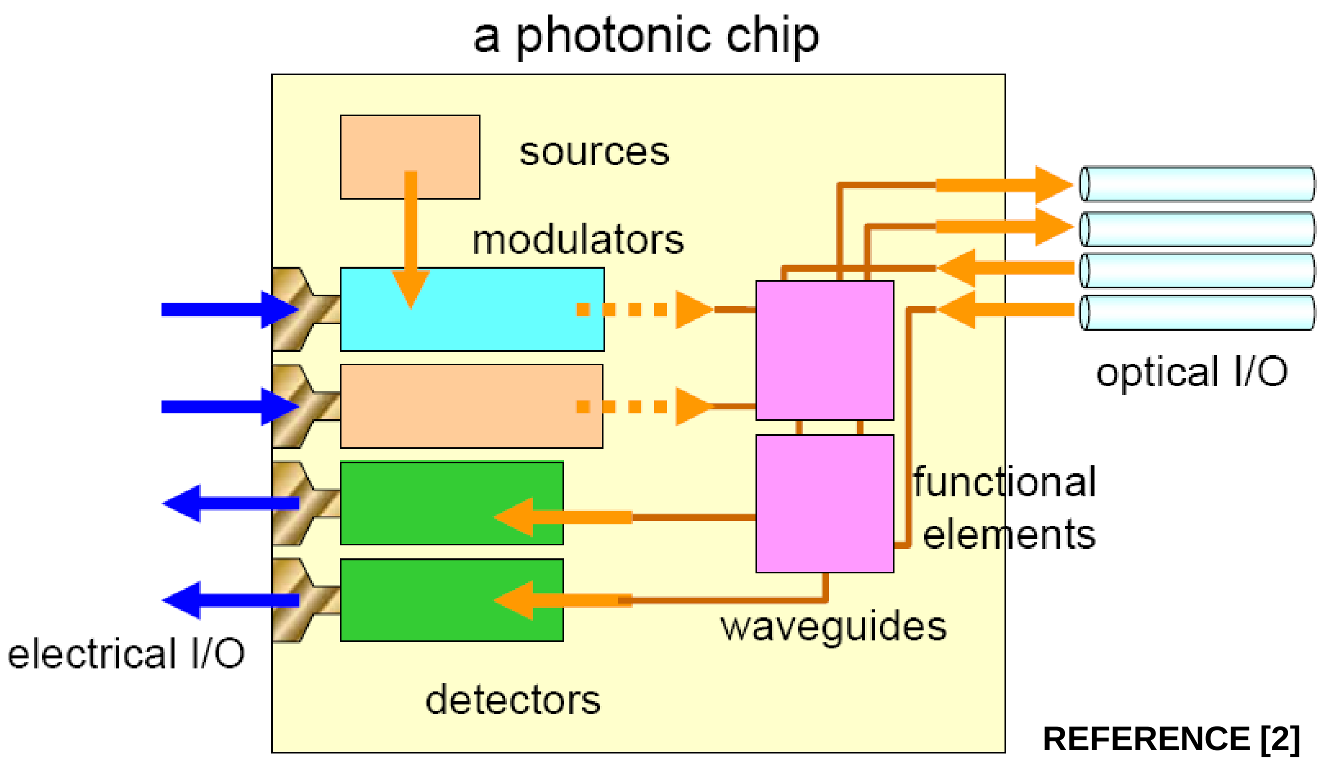
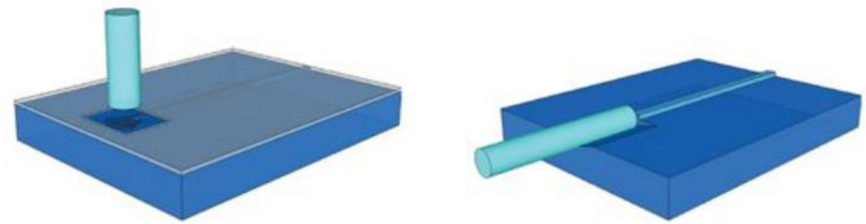
Silicon Photonics ICs



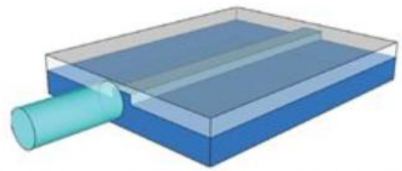
REFERENCE [2]

Connecting a Optical Fiber to the Silicon Die Optical Waveguide



(a) Vertical coupling of optical fibre to on-chip grating coupler

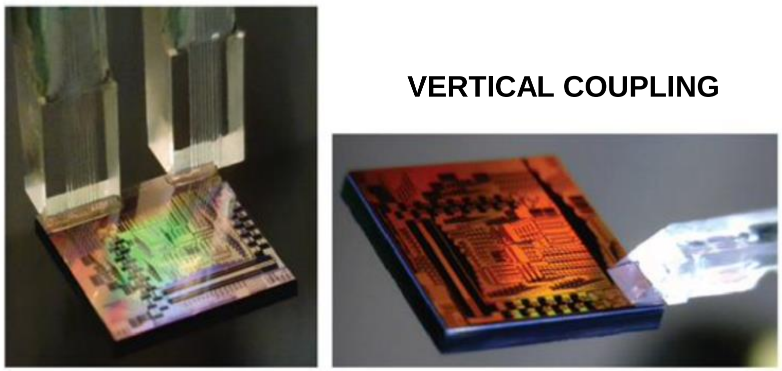
(b) V-groove coupling of optical fibre to on-chip waveguide



(c) Edge-coupled optical fibre to on-chip waveguide

FROM REFERENCE [3]

VERTICAL COUPLING



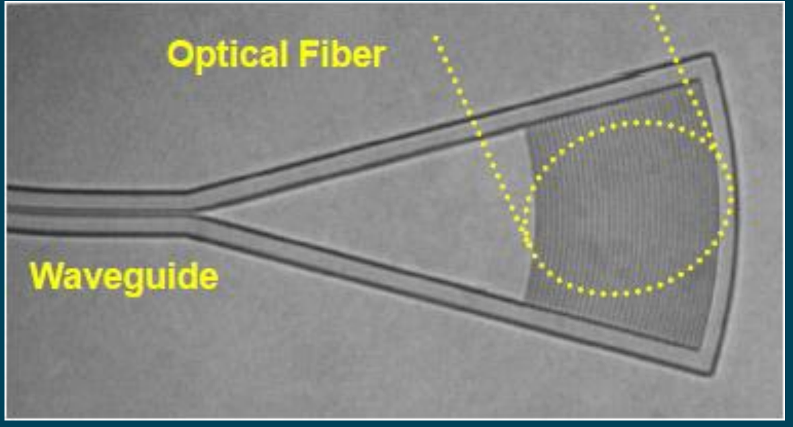
(a) Vertical mounting.

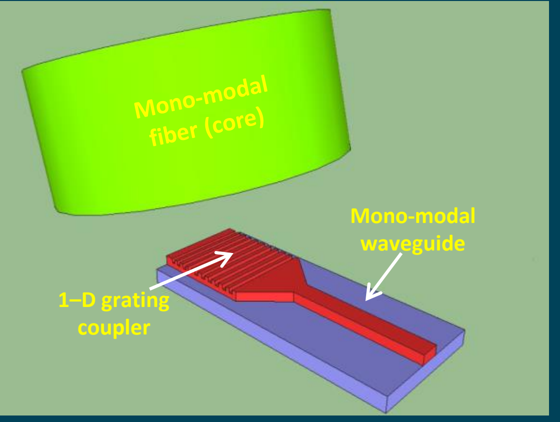
(b) Horizontal mounting using reflector.

Transmitter Side: Optical Coupler

1-D Grating Couplers

- Coupling a fiber to a waveguide is like trying to fill a water bottle with a fire hose, using a straw as connection (fiber core ~ 300 μm^2, waveguide core section ~ 0.1 μm^2).
- The grating coupler connects the fiber to the waveguide thanks to a taper that fits the width of the grating to the waveguide section area.

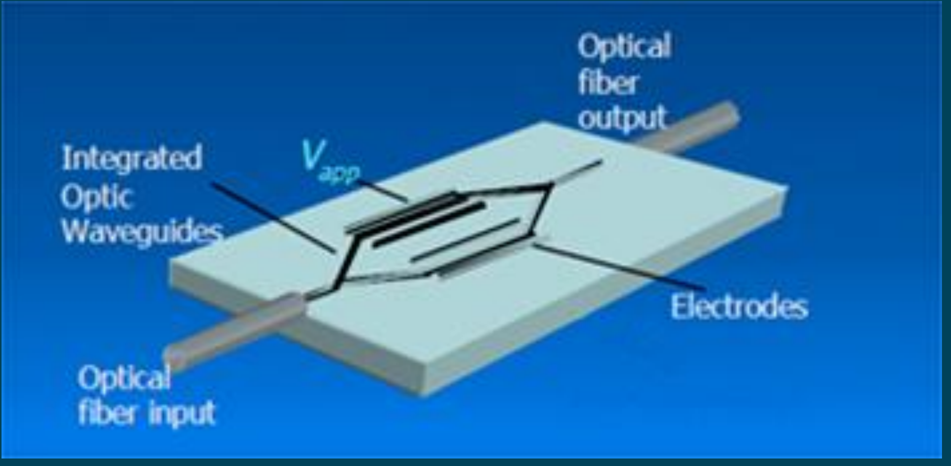




Transmitter Side: Optical Modulator

MZ Modulator

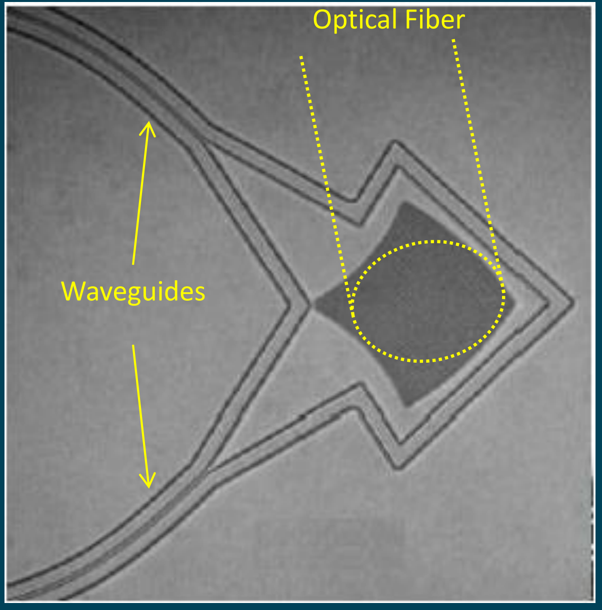
- Refractive index changes with the electric field applied into the semi-conductors (free carrier plasma dispersion effect).
- Changing the electric field along a waveguide allows to introduce a phase shift between the paths in order to achieve the signal modulation:
  1. An opposite phase situation between the parallel paths (no signal on output).
  2. An in-phase situation between the parallel paths (signal on output).

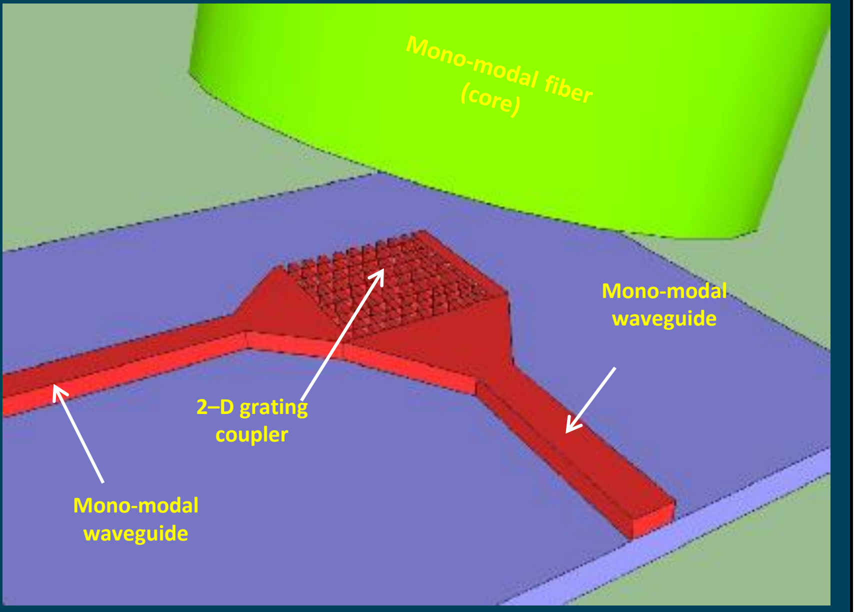


Receiver Side: Optical Coupler

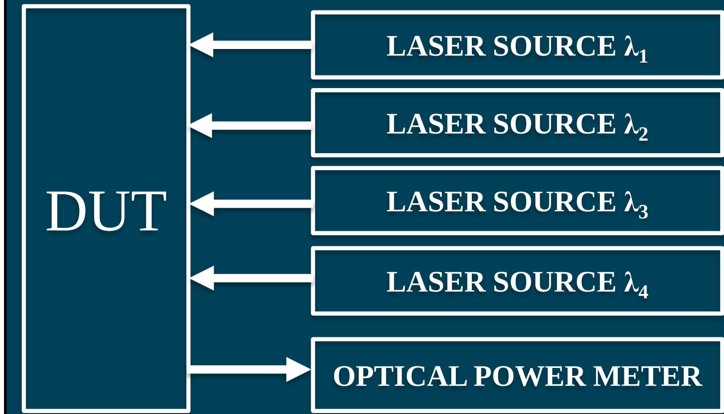
2-D Grating Couplers

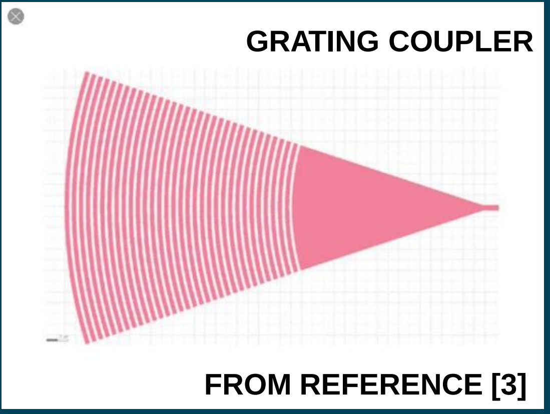
- The bi-dimensional grating coupler is made of two overlapped mono-dimensional gratings rotated by 90 degrees with two waveguides that couple two orthogonal states of polarizations.

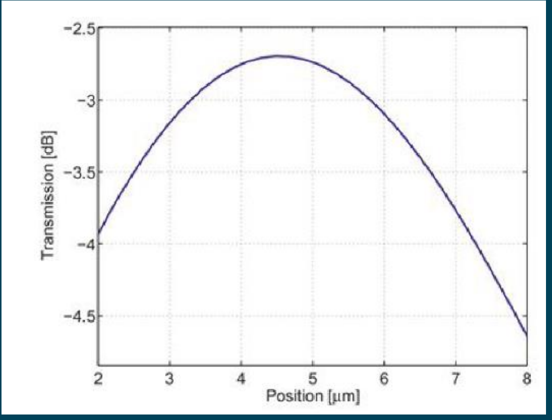




Test Requirements and Challenges

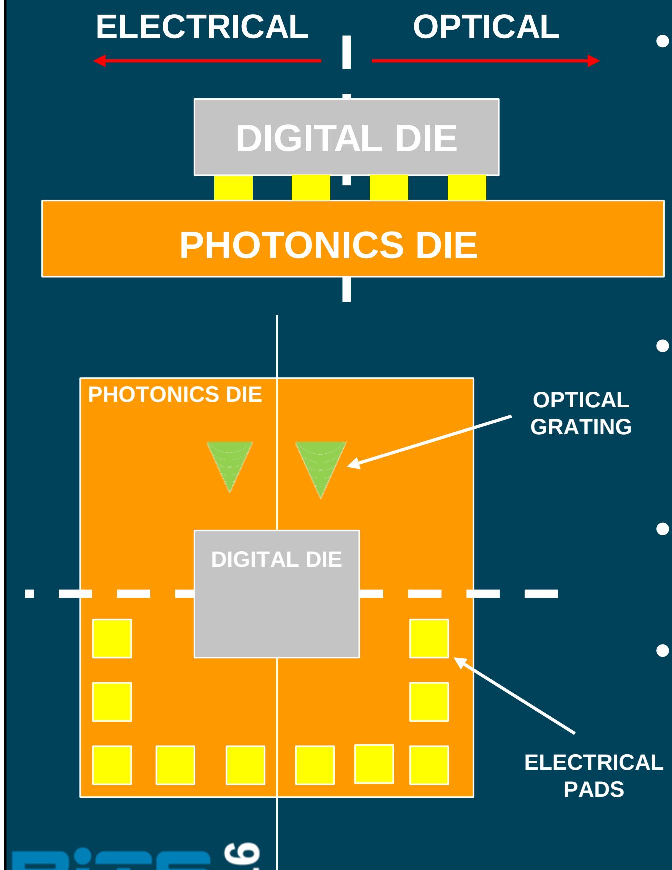






- Multiple laser sources are required.
- The optical fibers in a fiber array need to be aligned to the grating coupler in the die.

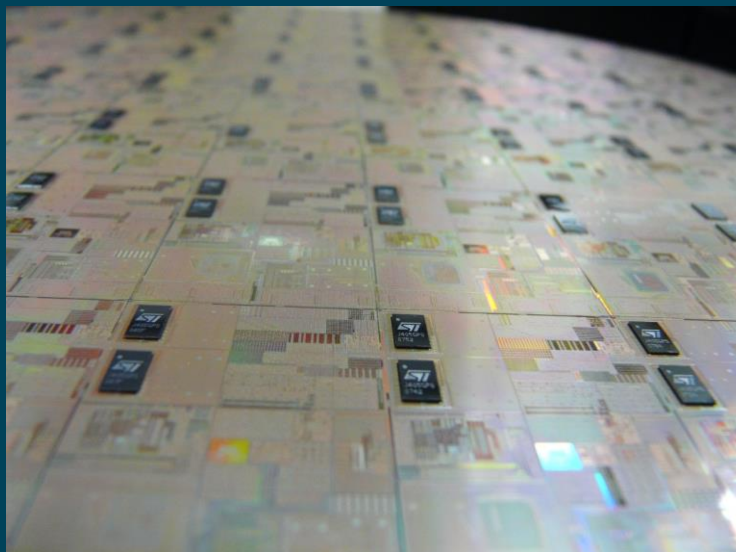
Probing Challenges



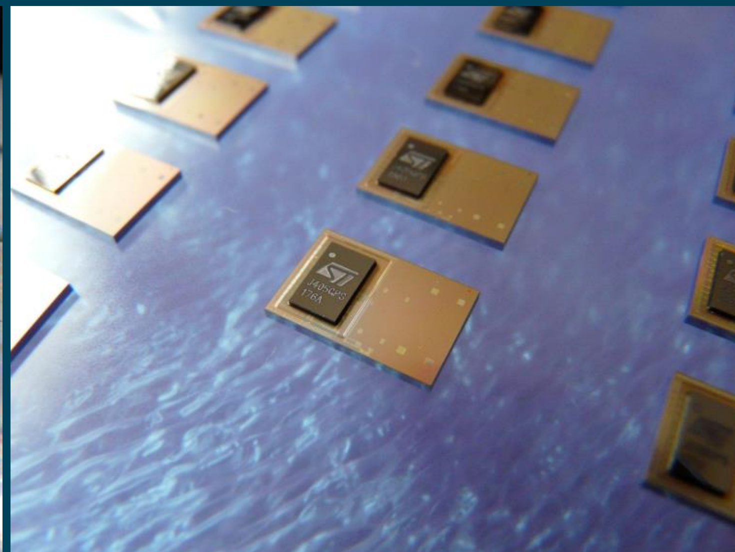
- By separating the digital and photonics parts into two separate dies it is possible to take maximum advantage of each process.
- The digital die can be tested using a standard electrical wafer probing approach.
- Both dies are stacked using copper pillars.
- The challenge is testing the die electrical and photonics sides at the same time.

Silicon Photonics Die Example

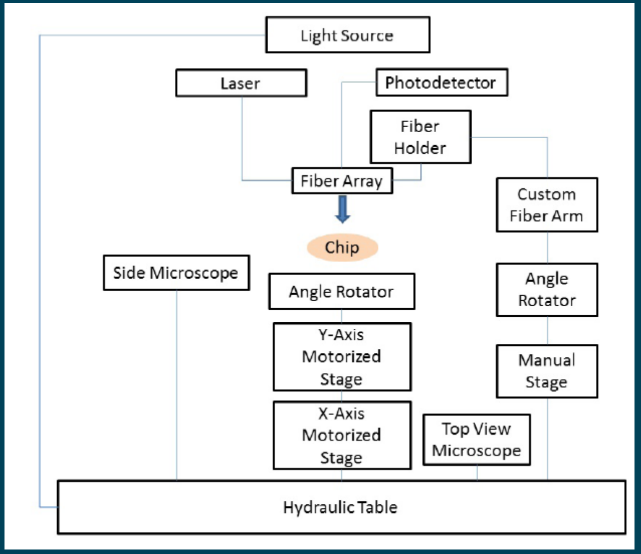
300 mm Wafer

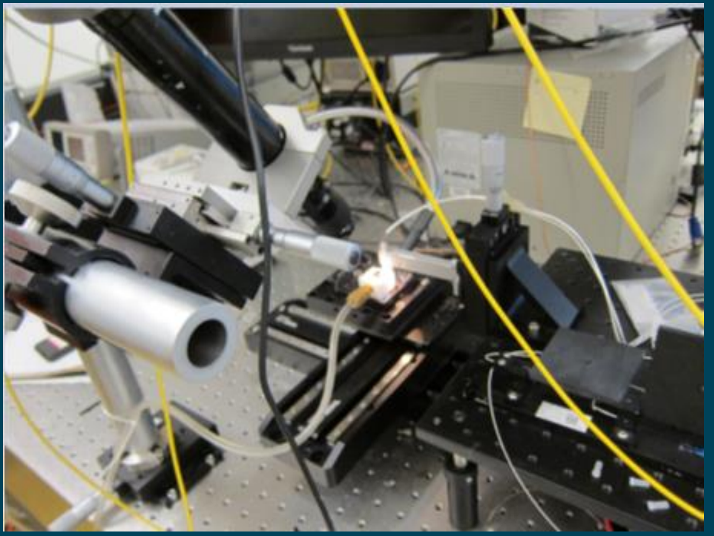


Singulated Dies



Photonics Die Measurement Approaches

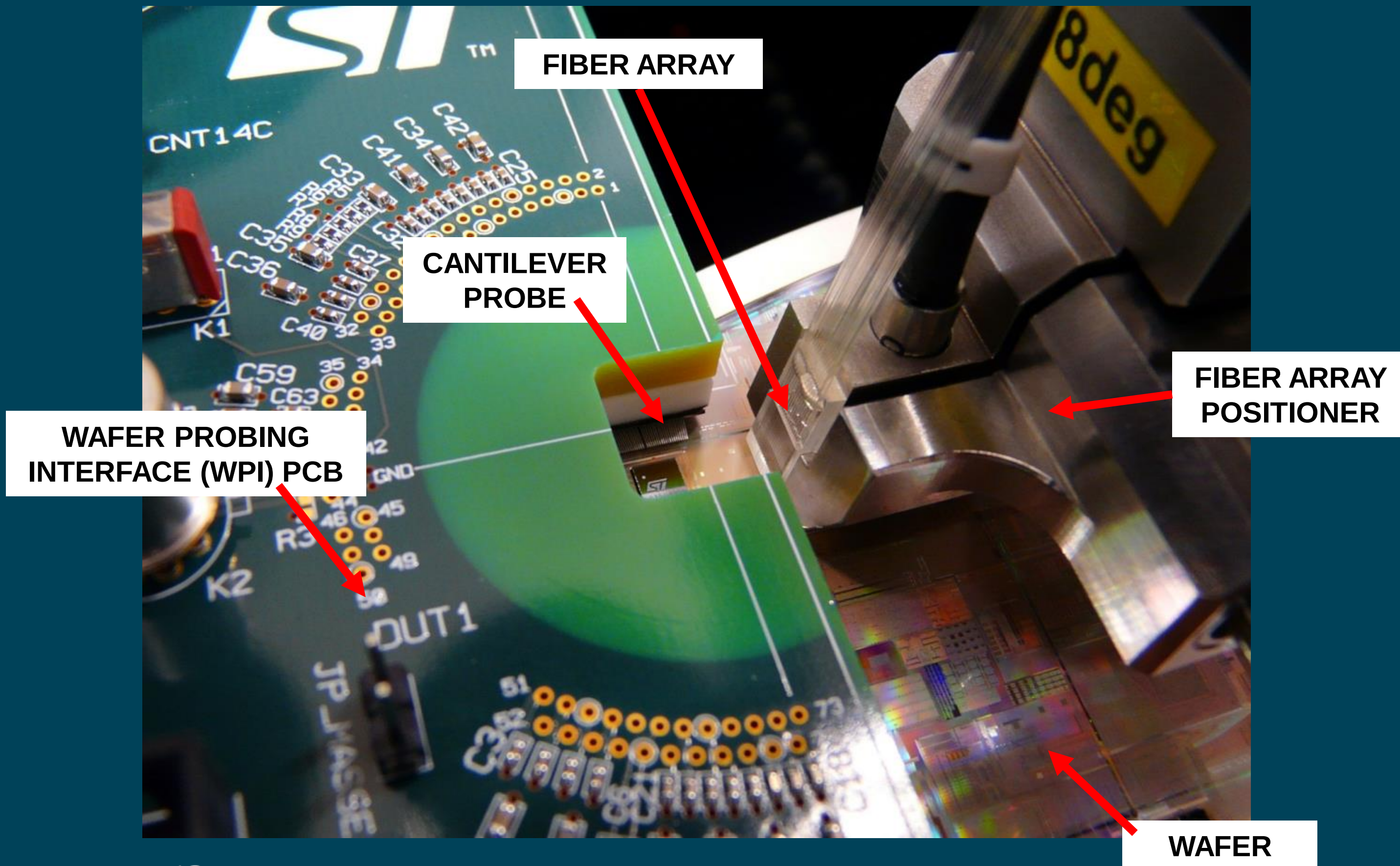




PICTURES FROM REFERENCE [4]

Although die level measurement approaches have been presented for photonics applications, they are mainly intended for lab characterization measurements and not volume production

Proof of Concept Wafer Probing Setup



Volume Production Challenges

- The optical side requires the fiber array to be aligned with precision on top of the grating coupler.
- The alignment of the fiber array needs to be done as fast as possible to minimize test time.
- Probe card needs to use standard wafer prober auto-loading.

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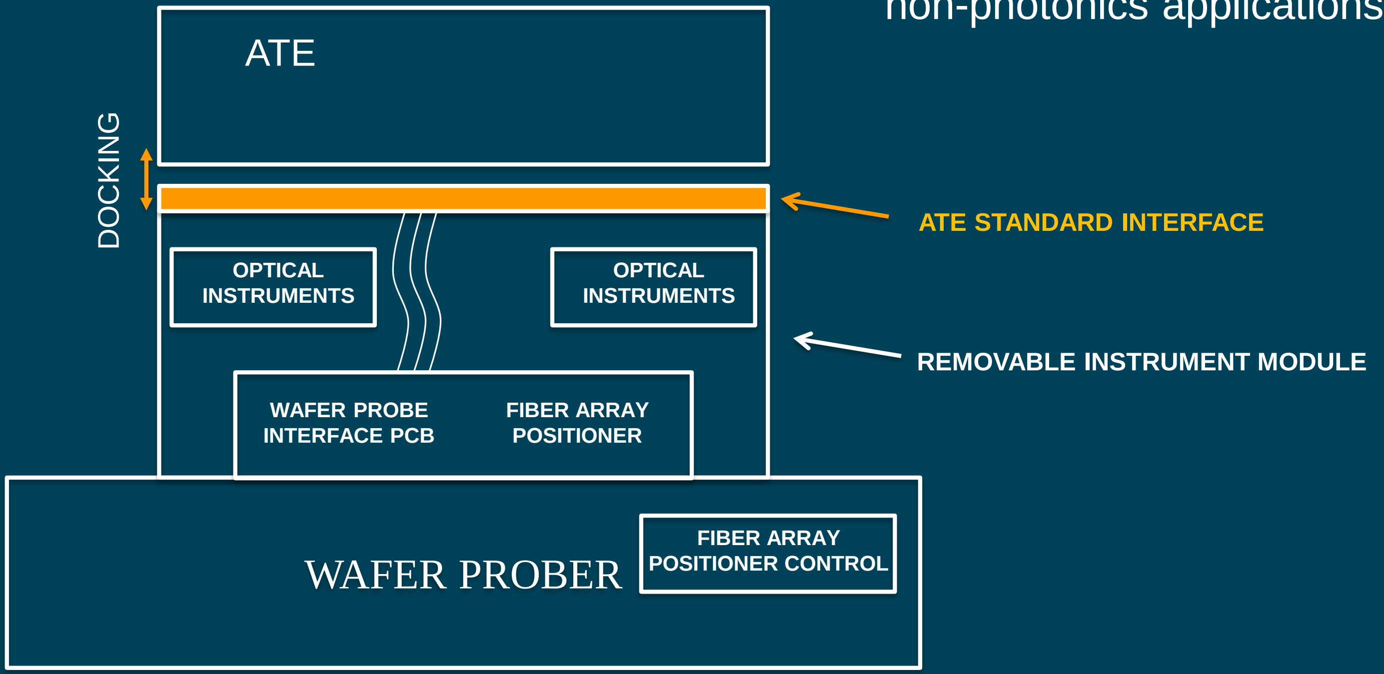
Wafer Probing Test Cell

The ATE system can be undocked and used for other non-photonics applications



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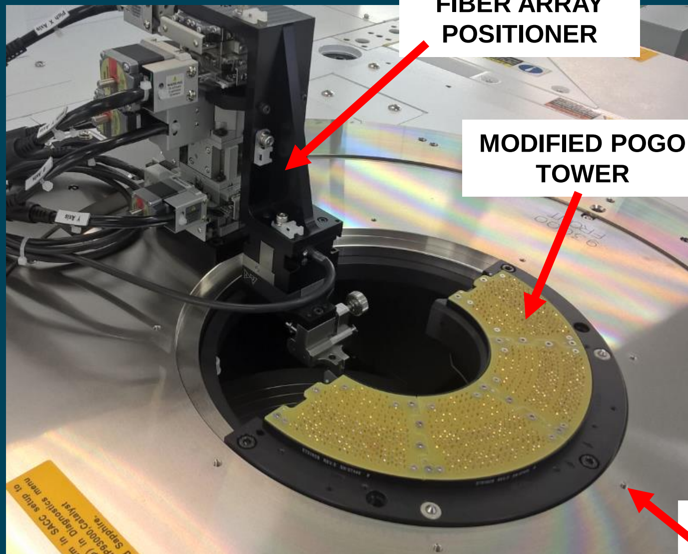
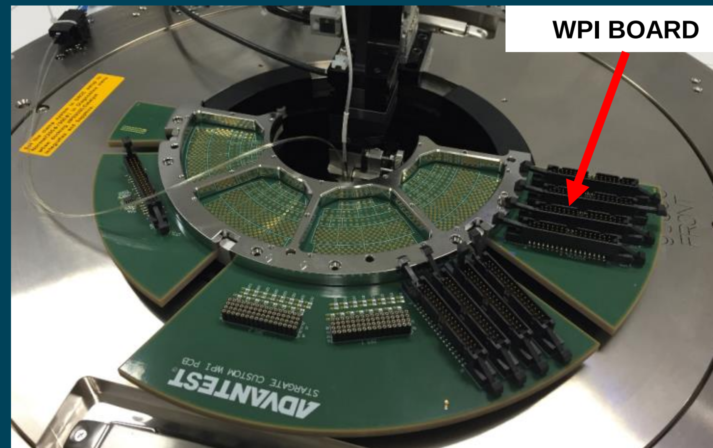
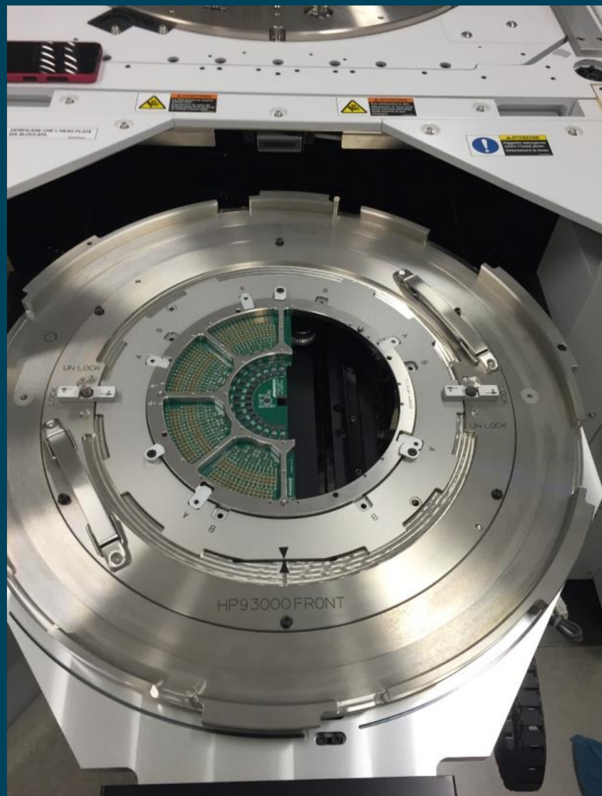
Wafer Probing Approach



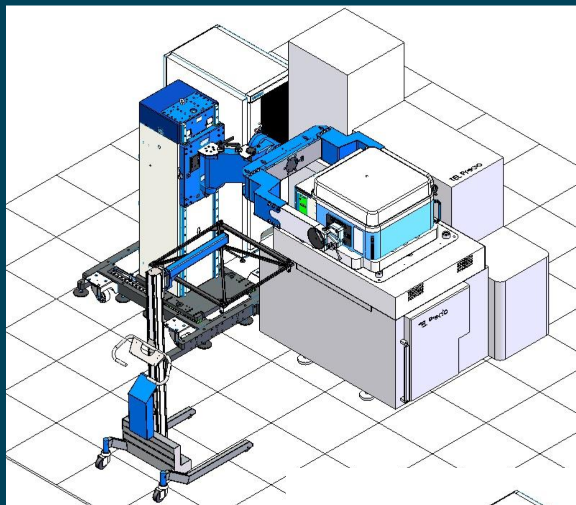


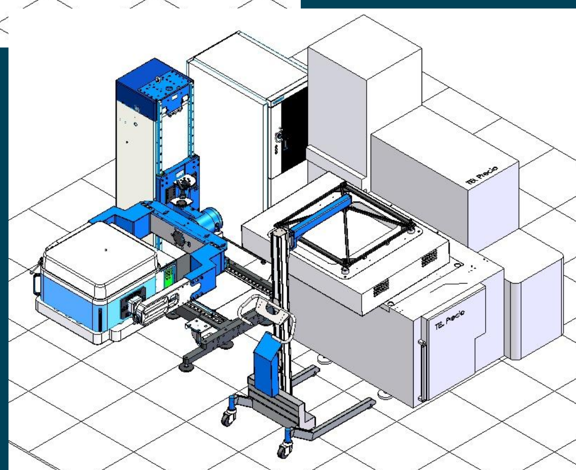
- Instrument measurement module is not shown in this picture.
- Special hardware is required to align the fiber to the probecard and the wafer.
- A modified “half-moon” pogo tower was designed to keep the photonics probing area free for the fiber array positioner movement.

Test Probe Card Auto-Loading



Test Cell





- The testcell includes a cart to lift the instrument module unit for prober maintenance.
- Because both the ATE system and the prober system are standard units, the test cell can be used for non silicon photonics applications if needed with a minimal effort.

Pictures courtesy of ESMO

Test Cell

PROBER INSTRUMENT RACK FOR PHOTONICS

ATE

ATE STANDARD DOCKING INTERFACE

REMOVABLE INSTRUMENT MODULE WITH LASERS AND POWER METERS

WAFER PROBER (ALSO CONTROLS THE FIBER ARRAY POSITIONER)

Software

- All laser sources and optical power meters in the instrument module are controlled via the ATE software using a GPIB interface.
- The ATE software also communicates with the wafer prober via a separate GPIB connection.
- Dedicated software is required for the fine alignment of the fiber array to the die.

Conclusions

- To achieve a high failure coverage at a low cost for silicon photonics products it is critical to test at wafer level in a production worthy test cell that can be deployed in an OSAT environment.
- Silicon photonics requires a merger of traditional digital ATE testing with silicon photonics testing requirements.
- To keep costs low it is critical not only to reuse standard equipment as much as possible but also to avoid a fully customized and dedicated silicon photonics test cell.

References

- [1] Tom Baehr-Jones, Ran Ding, Ali Ayazi, Thierry Pinguet, Matt Streshinsky, Nick Harris, Jing Li, Li He, Mike Gould, Yi Zhang, Andy Eu-Jin Lim, Tsung-Yang Liow, Selin Hwee-Gee Teo, Guo-Qiang Lo, and Michael Hochberg, "A 25 Gb/s Silicon Photonics Platform", arXiv.
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- [5] John E. Bowers, "Silicon Photonics Integrated Circuits", DesignCon 2016.

Acknowledgements

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  - TF Goth from FoundPac
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