SEVENTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

March 6 - 9, 2016

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive- Session 8

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BiTS Burn-in & Test Strategies Workshop 2016

Session 8
Jason Mroczkowski
Session Chair

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 9 - 10:30 am

Cell-ebrating Test Too

"Modeling Socket Thermal Performance Inside a Burn-In Chamber"
Jason Cullen – Plastronics
Rob Caldwell - Delta V Instruments

"Established the first WLCSP Testing at Tri-temp for RF and Non-RF Products"
Edwin Valderama & Jin Sheng Tan -Intel Technologies

"A Silicon Photonics Wafer Probing Test Cell"
Roberto Aranzulla, Daniele Sala, Roberto Barbon - ST Microelectronics
Giuseppe Astone, Maurizio Rigamonti, Massimo Galli - ST Microelectronics
Jean Luc Jeanneau, Dario Adorni, Paul Mooney - Tokyo Electron
Hubert Werkmann, Fabio Pizza - Advantest Europe GmbH
Jose Moreira, Zhan Zhang - Advantest

BiTS 2016 Burn-in & Test Strategies Workshop

Establish WLCSP Testing at Tri-temp for RF and non-RF products

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Intel Technology Asia Pte Ltd
Edwin Valderama
Intel Value Engineering/Technology

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Background

- First WLCSP product was a digital product that required ambient temperature test on a V93K tester.
- A team was formed to figure out how to test a WLCSP package

Objectives

- To enable the first WLCSP test setup
- To enable WLCSP test for follow-on products across temperature range.

The Outcome

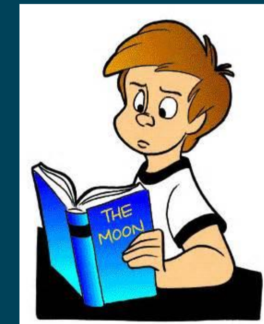
- The team manage to successfully put together the first WLCSP test setup
- More products follow, each bringing with them their own set of unique challenges
- Various test cells ranging from non-RF to RF test, from Hot to Cold test, has since been set up

Key Aspects

1. Type of Tester and Prober Required
2. Product Test Nature – RF or Non-RF Product
3. Testing Temperature
4. Tester-Prober Docking Mechanism
5. Bump/Solder Ball Pitch and Size
6. Bump/Solder Ball Material
7. Contactor – Pogo Pin or Probe Needle
8. PCB Warpage during Test
9. Testing Parallelism and Site Layout

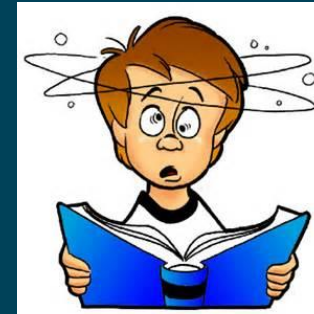
Homework

- Carry out market benchmark
- Analyse paper studies
- Understand material properties
- Consider potential mechanical stresses
- Review past experiments
- Plan future experiments



Studies & Experiments

1. Market Benchmark
2. Pogo Tower Setup vs Direct Docking
3. (V93K) Bridge Beams
4. Effects of Temperature on Hardware
5. Bump/Solder Ball Hardness
6. Probe Needle vs Pogo Pin
7. Hardware Planarity
8. PCB Warpage
9. Optimum Test Site Layout

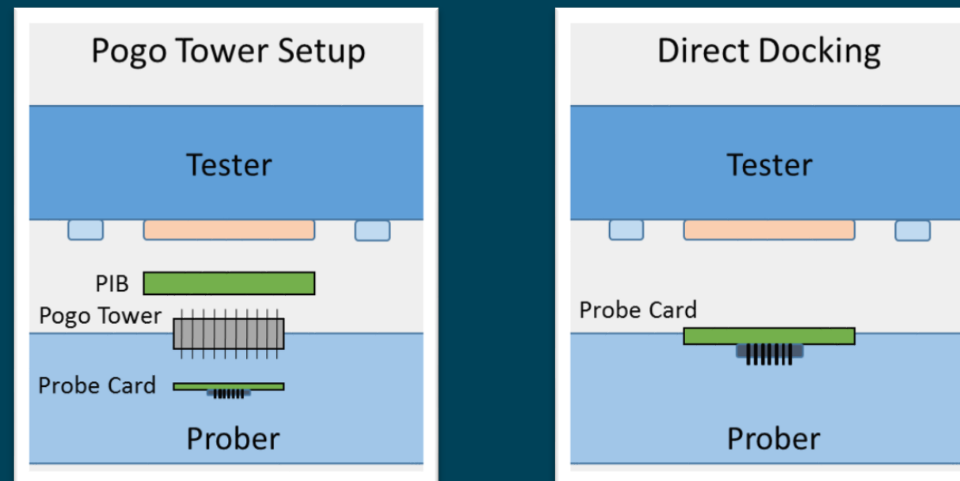


Market Benchmark

- Approach the hardware vendors and OSATs for common market practices and setup “styles”
- Examples of info gathered:
  - Bear resemblance to Wafer Sort process
  - Wafer prober is used
  - Traditional setup with pogo tower and direct docking method are both in used
  - Traditional probe cards and sockets are both in used

Pogo Tower Setup vs Direct Docking

- There are 2 types of setup being used:
  - Pogo Tower Setup
  - Direct Docking
- Depends on the need and restrictions of each product and tester/prober platform

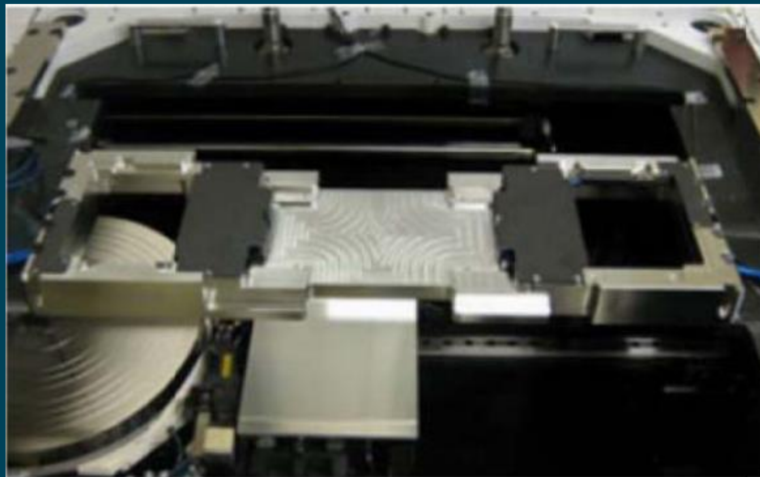


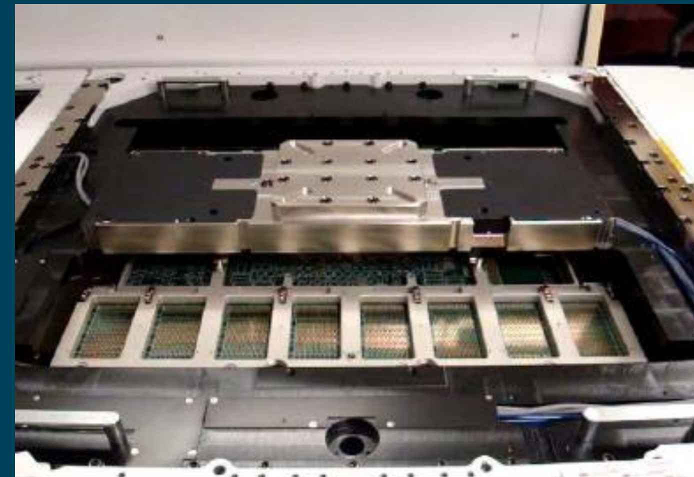
Pogo Tower Setup vs Direct Docking

Pogo Tower Setup	Direct Docking
Pro: - It's more readily available across multiple platform - Well familiar by most production sites	**Pro:** - Reduces the signal path length, lesser interface connection issues - Lower overall hardware cost
Con: - Introduces more variable with more interface layers - Higher overall hardware cost	**Con:** - Not (yet) available for every tester platform - Not all production sites are familiar with it

(V93K) Bridge Beams

- There are 2 types of bridge beams for V93K:
  - RF Bridge Beam
  - Digital Bridge Beam
- Which one to use? That IS the question!





(V93K) Bridge Beams

RF Bridge Beam	Digital Bridge Beam
Pro: - Can be used for products with any type of test nature - More spaces for mounting big components	**Pro:** - For products with digital and/or analog test - Much more rigid
Con: - Less rigid to support very high (overall) probe force	**Con:** - Cannot be used for products with RF test - Restricted space for mounting big components

Effect of Temperature on Hardware

- **Hot expands, cold contracts!**
- All hardware are affected by testing temperature, especially after prolonged usage
- Need to ensure all the operating temperature range of hardware used, especially probe needle and pogo pin, are well above the testing temperature range

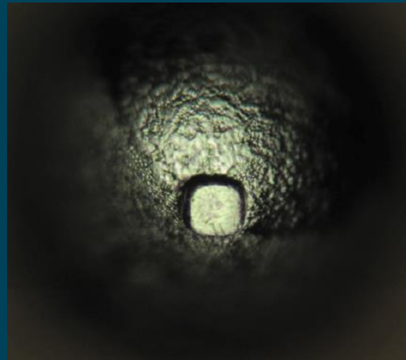
Bump/Solder Ball Hardness

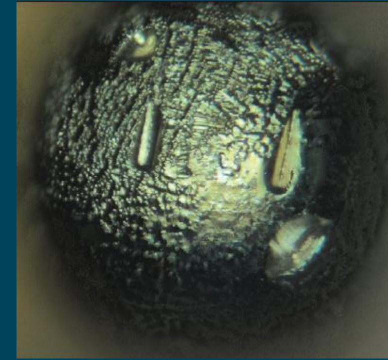
- To figure out the required probe/contact pin force for the each bump/solder ball material

Type	Composition				Hardness (HVN)
	Sn	Ag	Cu	Ni	
SAC387	95.5	3.8	0.7	-	21.9
SAC259	96.6	2.5	0.9	-	19.3
SAC219	97	2.1	0.9	-	17.7
SAC405 (LF31)	95.5	4.0	0.5	-	17.4
SAC355	96	3.5	0.5	-	17
SAC305 (LF45)	96.5	3.0	0.5	-	16.7
SAC205	97.5	2.0	0.5	-	15.7
SAC255	97	2.5	0.5	-	15.6
SAC125-0.05Ni (LF35)	98.25	1.2	0.5	0.05	14.9
SAC107	98.3	1.0	0.7	-	13.8
SAC105 (LF38)	98.5	1.0	0.5	-	13.3
SAC155	98	1.5	0.5	-	12.9

Probe Needle vs Pogo Pin

- Both types are usable, but which one is more suitable for the application?





Probe Needle vs Pogo Pin

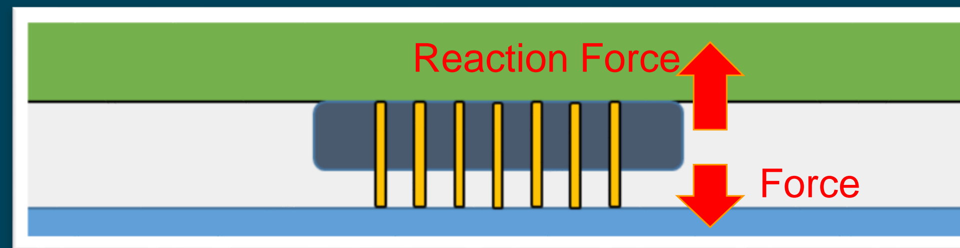
Probe Needle	Pogo Pin
Pro: - Available for very fine pitch application - Easy for probe-pad alignment to probe tip - Better planarity control	**Pro:** - Generally cheaper - Much easier to perform replacement in production - High contact force - Higher overdrive range
Con: - Generally more expensive - More troublesome to perform maintenance - Low probe force - Lower overdrive range	**Con:** - Only available down to certain pitch (for now) - Probe-pad alignment for crown tip is challenging - Harder to control planarity

Hardware Planarity

- It is important for the hardware used to have a good control on the planarity after assembly
- This is applicable to docking, the board (PCB), the needles/pins in the probe head/socket
- The higher the planarity variance, the higher the prober overdrive required
- **Risk** : Probe card damaged and/or wafer damaged (due to over travel)

PCB Warpage

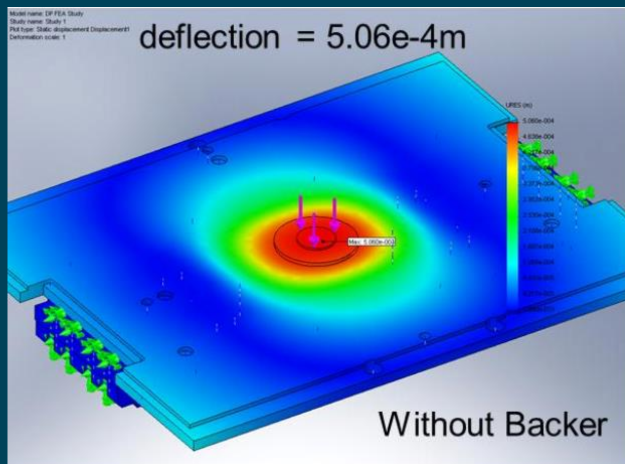
- **Newton's 3rd Law of Motion : For every action there is an equal and opposite re-action !**

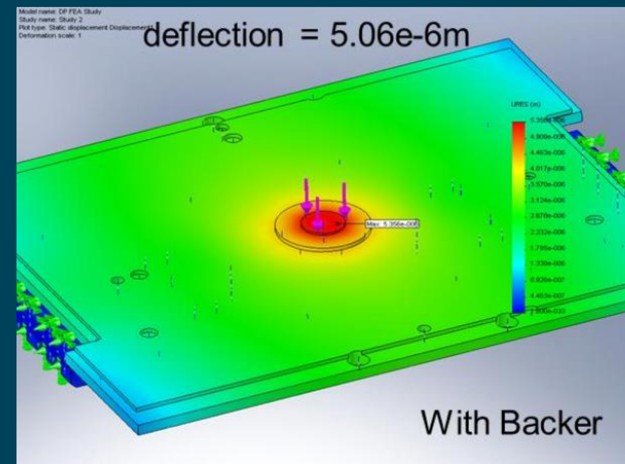


- This reaction force is bad! It has the potential to warp/bend the PCB upwards.

PCB Warpage

- Solutions:
  - Thicker PCB and/or more robust reinforced PCB stiffener designed to counter the warpage
  - For V93K, make use of the Bridge Beam with the help of an additional “backer”

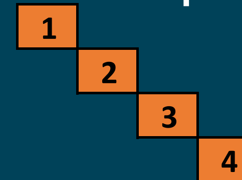




Optimum Test Site Layout

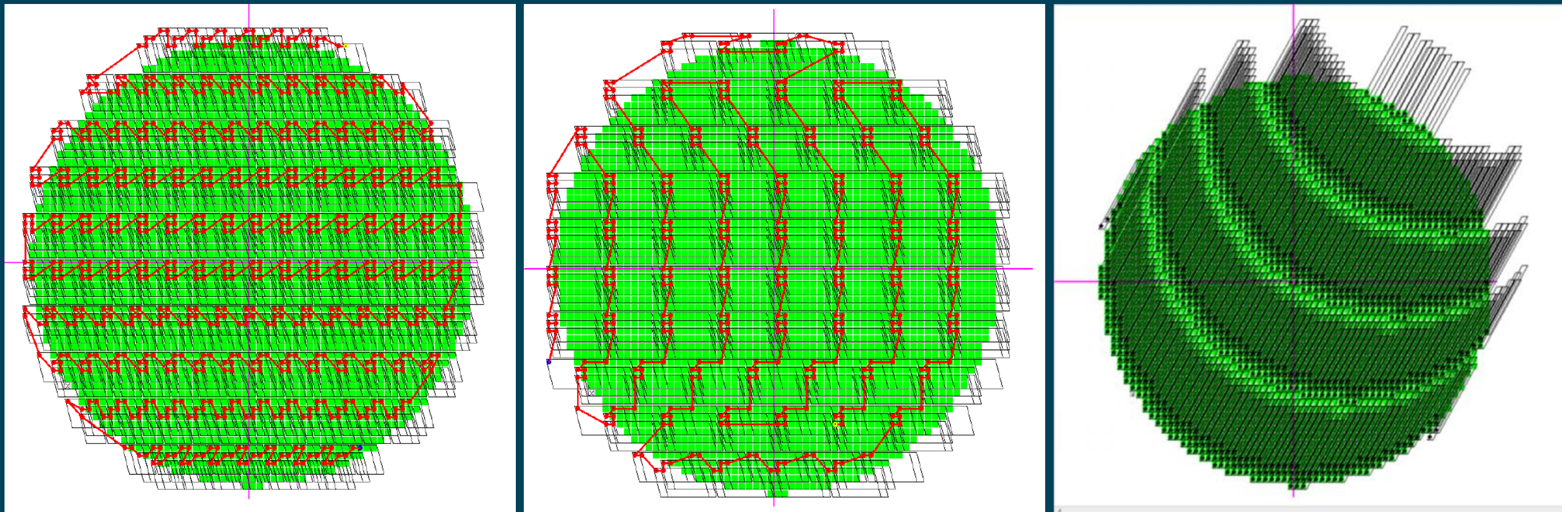
- The optimum test site layout is achieved when the whole wafer goes through testing with the least steps or touchdowns
- Theoretically, the optimum layout would be a square/rectangular shape without any skip dies

- But in reality, this is hard to achieve due to the PCB design constraint (traces and components)

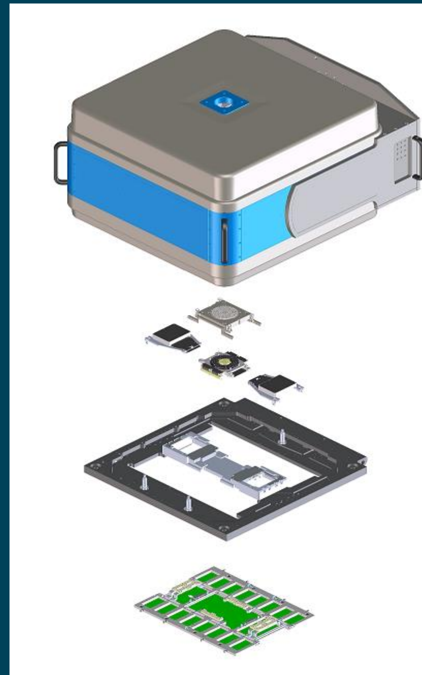


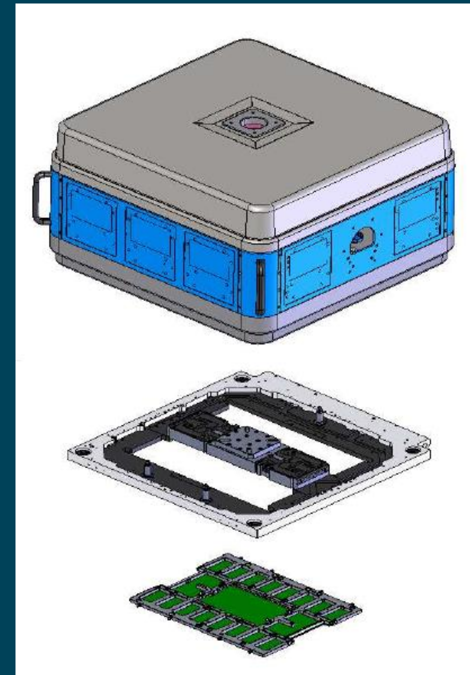
Optimum Test Site Layout

- Fear Not ! There are software and services available in the market that can help with this analysis



The Final Setup





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Conclusion

- Good understanding of WLCSP product test and challenges with proper consideration of key aspects had helped to enable first and subsequent WLCSP test for Intel products.

Next Steps

- To further fine tune the setup to achieve healthy and cost effective manufacturing goal
- To make the RF Bridge Beam more rigid and universal across product types (on V93K)
- To improve the planarity control of pogo pins in the socket