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BiTS
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 6
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BiTS 2016 Burn-in & Test Strategies Workshop

Session 6

Jason Mroczkowski

Session Chair

BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 8 - 1:30 pm

Cell-ebrating Test

"Vision Assist Method for Common Change Kit"

Brad Emberger, Zain Abadin – Advantest

"Test Cell Thermal Solution"

Gianluca Lombardi - Advantest

"Testing Magnetic Sensors"

Paul Ruo - Aries Electronics, Inc.

Larre Nelson - Kita USA

"Magnetically shielded test-cell for an integrated fluxgate sensor"

Gert Haensel - Texas Instruments

Loren Hillukka - Johnstech International Ltd.

BiTS 2016 Burn-in & Test Strategies Workshop

Test Cell Thermal Solution

Gianluca Lombardi
Advantest

2016 BiTS Workshop
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Overview

- First things first: acronyms!
- Why temperature control?
- Challenges
- Test Cell approach

Acronyms!

M4871	Advantest SoC P&P Handler
93K	Advantest SoC tester
ATC	Active Thermal Control
DFT	Design For Testability
DUT	Device Under Test
θ_{JC}	Thermal resistance junction/case
T_J	Junction Temperature
T_C	Case Temperature
T_P	Pusher temperature
T_{HS}	Heat Sink Temperature

Why Thermal Control?

- Increasingly temp-sensitive tests
  - VMIN
  - FMAX/speed binning
  - PMIC trimming
  - IDDQ
- Deviations from desired temperature set point lead to incorrect measurements, wrong binning, resulting in either yield loss or RMAs

Passive/Active Thermal Control

- Passive
  - The control system maintains the same heat sink temperature at all times
- Active
  - The control system changes the heat sink temperature in response to temperature variations, to more quickly supply/sink heat to/from the DUT and restore the desired temperature

Why Active Thermal Control?

- Performance
  - Faster response to temperature variations, everything else being equal
- Correlation
  - Empirical temperature control solutions tend to lead to inconsistent yields from production site to production site

Thermal Stack

Temperature control quality is the result of all the following contributors

- ATC heat sink
- Package
- Socket
- Handler change kit
- Loadboard

Continuity vs Thermal Contact

Factors limiting temperature control quality w/Continuity already established

- High thermal resistance between ATC heat sink and package
  - Limited or missing gimbaling
- Package –more on this in the next slide

Package Challenges

- Junction/case thermal resistance, θ_{JC}
- Top side roughness/markings
  - Roughness = air gaps= higher θ_{JC}
- Planarity
  - Thin packages warping/flattening over T_J
- Contamination

DUT Challenges

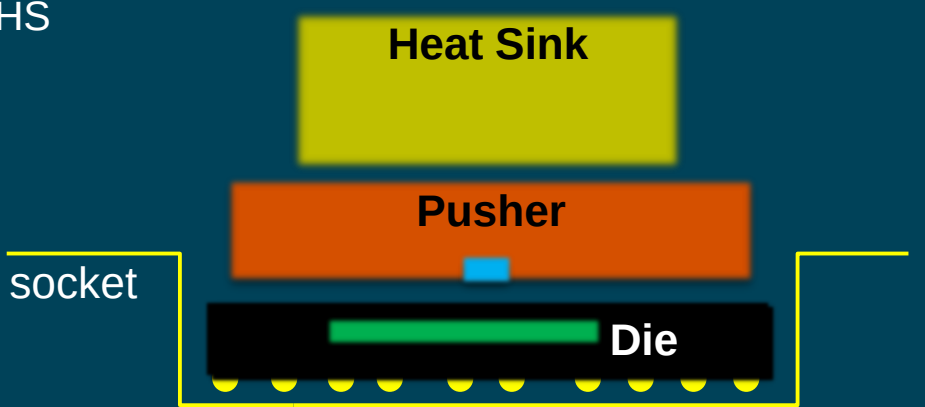
- Temperature feedback availability
  - Thermal diode: always
  - Temp sensors: generally after initialization and ATPG
    - Need additional DFT/resources

Test Cell Challenges

- Socket/loadboard/DUT/tester can quickly get damaged by thermal runaways
  - Must detect early signs of failure, wherever it may come from
  - Even more so with high power applications, 100W and above

Where to Sense DUT Temperature

- DUT thermal diode (T_J)
  - One in the whole chip, always available
- DUT embedded temp sensors
  - Multiple available generally after init/ATPG
  - Temperature gradients can be quantified
- Heat Sink, T_{HS}
- Pusher, T_P
- Case, T_C



ATC Challenges (I)

- ATC response time within milliseconds range
  - Limited by heat transfer time constants through stack
- Very fast DUT T_J rise transients may come and go before the they get detected and corrected by best-in-class ATC
  - Slow heat propagation through thermal stack
- ATC can only do so much, if the thermal stack is highly thermally resistive
  - Slow to detect, slow to respond to $\Delta T/\Delta t$

ATC Challenges (II)

- T_{HS} is M4871 default T measurement source
- T_{HS} may NOT follow T_J very closely
  - with just 10W power being dissipated, T_J can raise by 10-12C, while T_{HS} hardly moves by 1-2C,

Test Cell Example

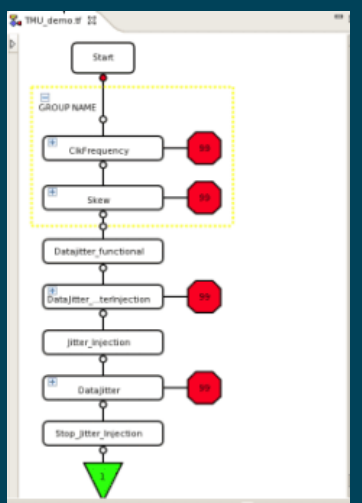
Advantest M4871 handler

Advantest 93K tester

Real-Time Junction Control (T_J)

ATC CONTINUOSLY…

- Measures junction temperature T_J and detects over/under shoots
- Reacts to ΔT_J driven by **ALL DUT power domains**



Sample testflow

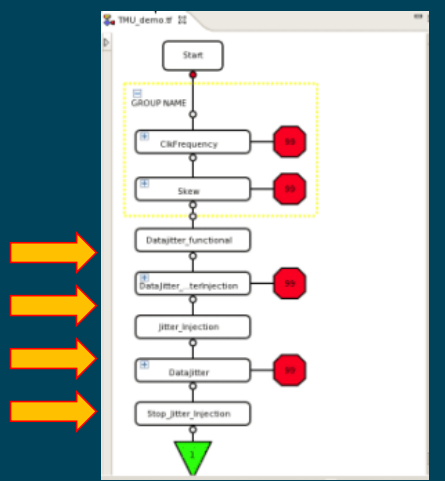
- **Patterns applied to DUT**
- **Sequencers running**
- **Power being dissipated**
- **During & in-between testsuite execution**

T_J Control while device is under test

Supported T_J Feedback Types

93K test program controls temperature feedback signal used by M4871

- T_J ANA (diff/SE)
- PWM
- I2C

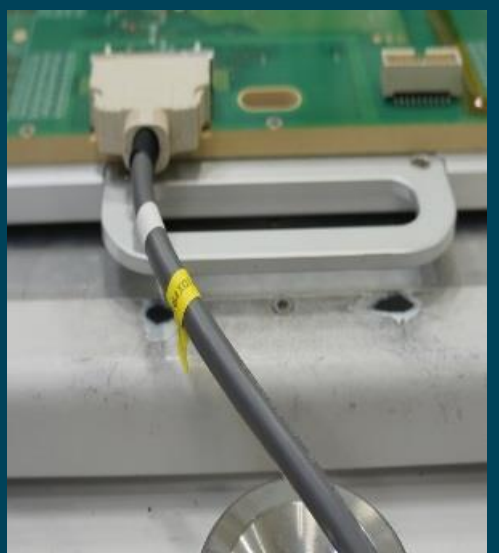


Sample testflow

Feedback mode can be changed testsuite by testsuite

M4871/93K ATC Interface (I)

93K loadboard ATC connector



M4871 front panel ATC connector

M4871/93K ATC Interface (II)

Signal	Direction
ANA_TEMP+	Driven by DUT
ANA_TEMP-	Driven by DUT
I2C_DTA	Driven by DUT
I2C_CLK	Driven by DUT
PWM	Driven by DUT

M4871/93K ATC Interface (III)

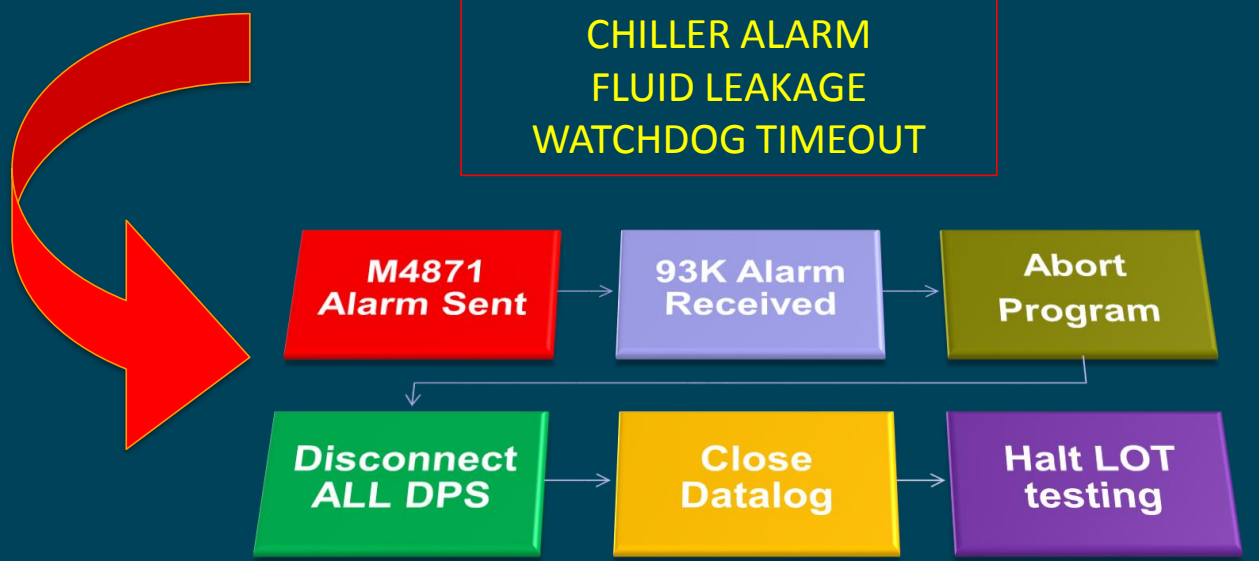
Signal	Direction
PROFILE_PRETRIGGER	Driven by 93K
T-CASE_B	Driven by 93K
T-PWM_B	Driven by 93K
M4871_OK_B	Driven by M4871
UHC4_SAFETY_LINE_B	Driven by M4871
CABLE_OK_B	Monitored by 93K

Equipment Protection

Test Cell Thermal Alarm

Handler failures will halt tester

COMMUNICATION ERROR
TEMP. SENSOR FAIL
CHILLER ALARM
FLUID LEAKAGE
WATCHDOG TIMEOUT



WITH direct UHC4 (160A) shutdown control

Device Temperature Calibration

DUT T/V Calibration (I)

Concept

- Accurate T_J measurement required only during calibration
  - Provided by temperature monitor IC or DUT, once per insertion
- When DUT is at set point (e.g. T_J = 85C), thermal diode voltage $\overline{V_{BE}}$ is measured and ATC calibrated

$\overline{V_{BE}}$: thermal diode voltage measured when DUT @ set point

DUT T/V Calibration (II)

Concept (cont.)

- After calibration, $V_{BE}(\mathrm{t})$ is monitored by M4871
  - Biasing current supplied by loadboard circuitry or tester channel
- $V_{BE}(\mathrm{t})$ is now the ATC feedback signal, not $T_J(t)$

ATC will minimize $\Delta V_{BE} = \{V_{BE}(\mathrm{t}) - \overline{V_{BE}}\}$

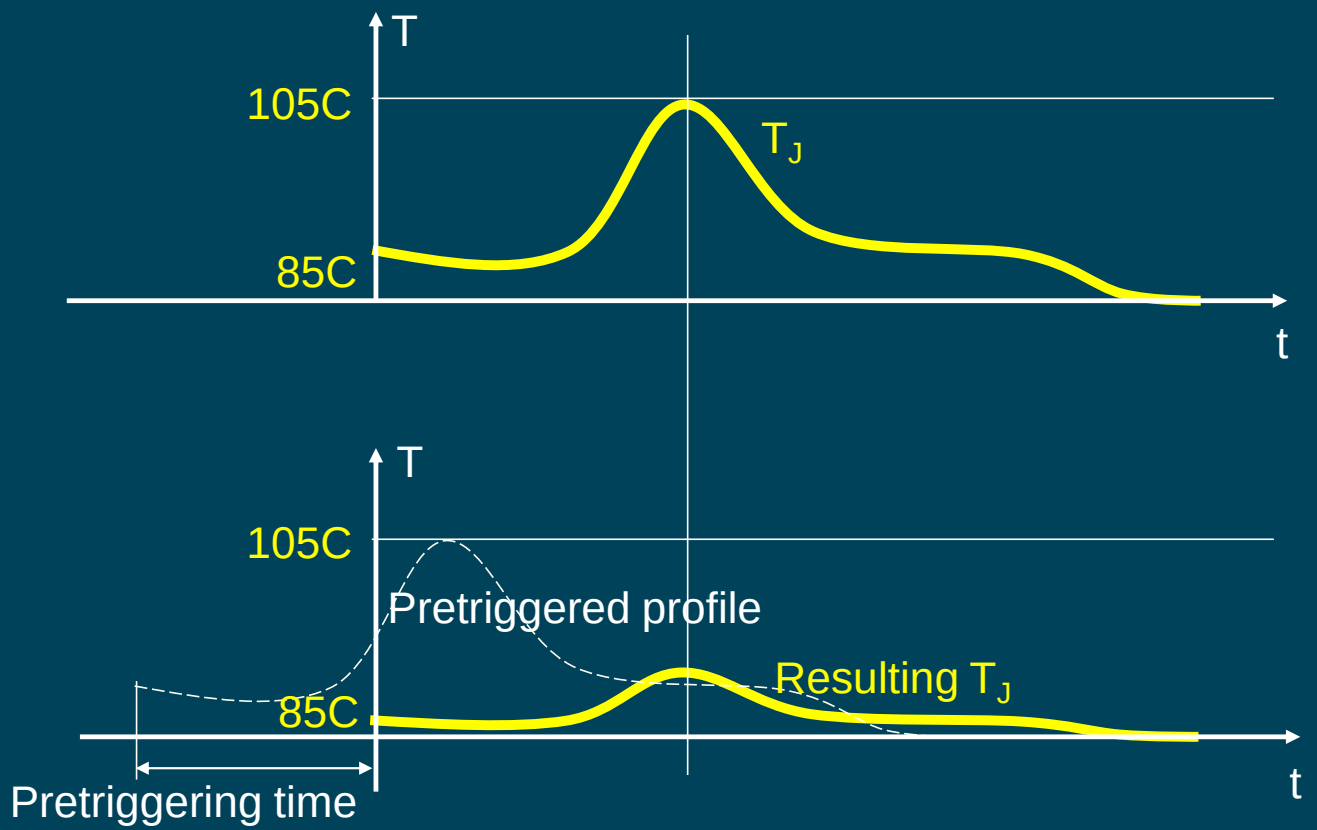
DUT T/V Calibration (III)

Advantages

- Measuring is faster than calculating $T_J(t)$
- NO add'l voltage/temp conversion required after T/V calibration
- Immune to silicon process and ESR
  - Relies on accurate thermal diode ideality factor

Profiling & Pre-Triggering

The Concept



Test Cell Thermal Solution

Profiling/Pre-triggering API Support

Temperature profile management

– Download/Select/Query profiles

- **PH_DOWNLOAD_PROFILE**
- **PH_SELECT_PROFILE_BY_SITE**
- **PH_QUERY_PROFILE**

Profiling/Pre-triggering TML Support

Zero-overhead → hides pre-triggering time behind low power pattern