

SEVENTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop

TM

March 6 - 9, 2016

**Hilton Phoenix / Mesa Hotel
Mesa, Arizona**

Archive- Session 5

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Session 5

Ashok Kabadi
Session Chair

BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 8 - 10:30 am

West Meets East & Cutting Edge

"LPDDR4 Signal & Power Performance Optimization By Hardware"

"通过测试硬件的优化来提升LPDDR4信号和电源的性能"

Yuanjun Shi - Twinsolution Technology

Xiao Yao - HiSilicon Technologies Co

"Reliability Characterization of Unpackaged (bare) die for Silicon Photonics module"

Sujata Paul, Andrew Fong, Samir Alqadhy, Huy Nguyen, Zoe Conroy - Cisco

Tom Elliot, Jag Jassal - Evans Analytical Group

"Advanced High Energy CO2 Spray Cleaning Technology for Burn-In Test Substrate Cleaning Applications"

Nelson Sorbo - Cool Clean Technologies

"Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution"

James Tong, Hisashi Ata - Texas Instruments

Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution

James Tong, Hisashi Ata
Texas Instruments



2016 BiTS Workshop
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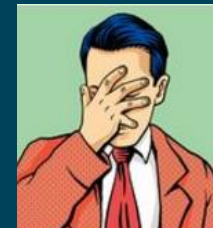
Contents

- What's the Problem?
- Problem Statement
- Technical Solution and Challenges
- Learning the Pin Type
- Learning the Pin Design
- Learning the BGA contactor design
- Learning the QFP contactor design
- TI contactor qualification process
 - Step1: Vendor's factory evaluation
 - Step2: TI technical qualification
 - Step3: TI production qualification
 - Step4: Qualification data review and deployment
- Summary
- Acknowledgements

What's the problem?



Fix the Problem?



OMG

- Objective
- Main Goal

Problem Statement

- Legacy contact technologies cannot support today's test application requirements.
- Different approach to deal with the short fall from every A/T sites
 - Incompatibility performance
 - Localized support to each A/T site
 - yield correlation problem
 - Multi-factories loading limitation.
- Resulting in customized pin design by device by user.
- Work against cost reduction model to benefit TI worldwide

Application	Legacy Pin [High Profile, <15GHz]		Custom Pin [High Profile, <15GHz]	
	Cost/Pin	<500K Life	Cost/Pin	~1M Life
0.4 BGA	Vendor A		-49% Vendor D	
0.5/0.65 BGA	Vendor A		-15% Vendor C	
0.8/1.0 BGA	Vendor A		-14% Vendor D	
0.5 QFP	Vendor A		-10% Vendor D	

Strategy

2014 Execute and gain share

- ✓ High Performance pins
 - Low Cres
 - High CCC (Current Carrying Capability)
 - High bandwidth
- ✓ Common use across tester platforms, pin pitches and A/Ts
 - Volume pricing
 - Sameness across A/Ts
- ✓ Low COO (Low Cost, Long Life > 1,000K insertions)
- ✓ PCB footprint compatibility
- ✓ WW TI support

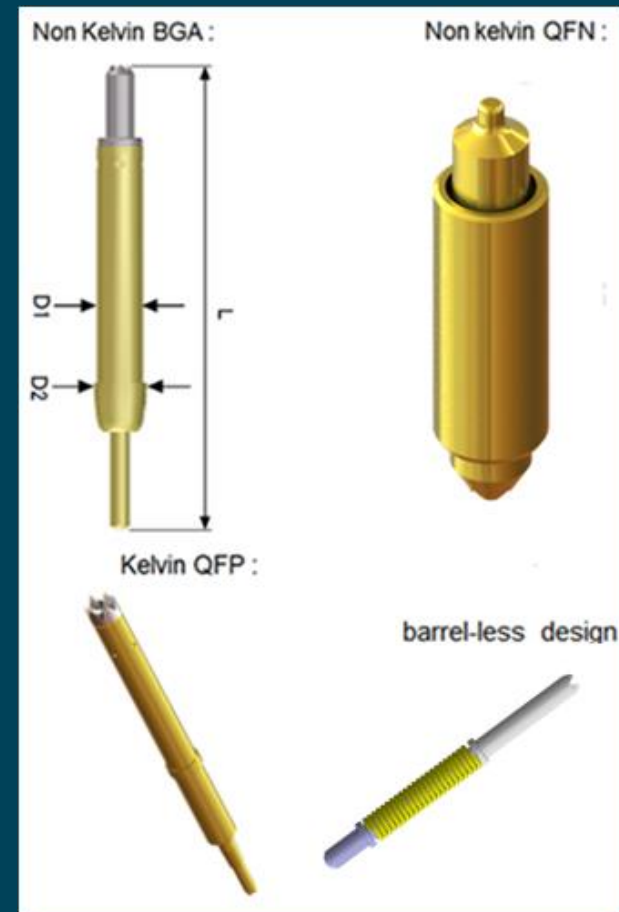
Technical Solution and Challenges

Solution

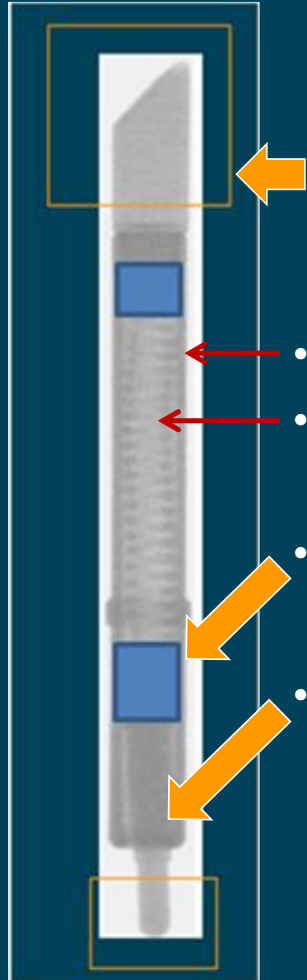
- Shorter pin resulting in less metal between the load-board and the Device-Under-Test (DUT)
- Lower pin inductance
- Better signal integrity

Challenges

- High current carrying capability (CCC)
- Reliable contact resistance (Cres)
- Pin manufacturability: Low cost

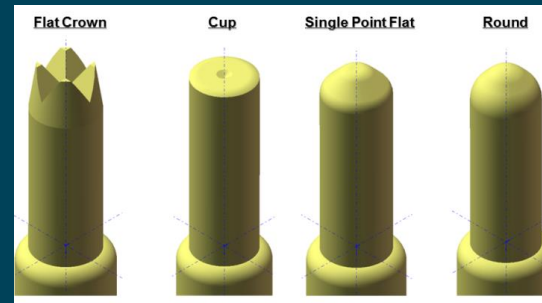


Learning the Pin Type

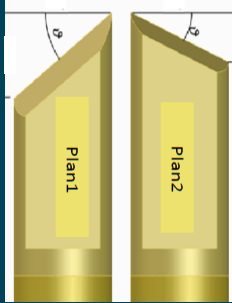


- Unlimited tip shape and design.
- Tip material: Homogenous, plated core material, etc.

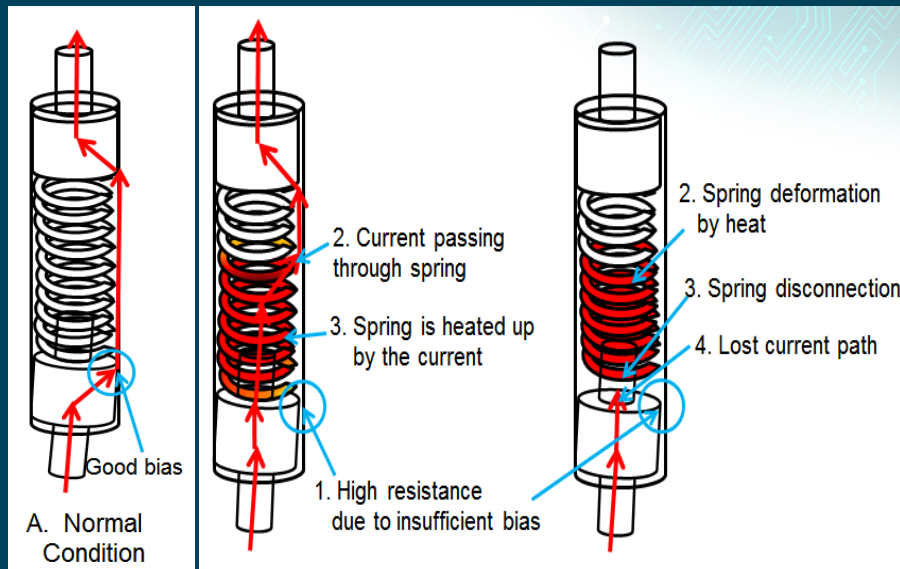
- Barrel: diameter and plating thickness
- Spring design and material: Total force, life, contact reliability and temperature rating
- Biasing mechanism
 - CRes, CCC, spring performance and lifetime
- Bottom Plunger design
 - Material
 - Unlimited Shape
 - Plating recipe
 - PCB pad damage



Learning the Pin Design

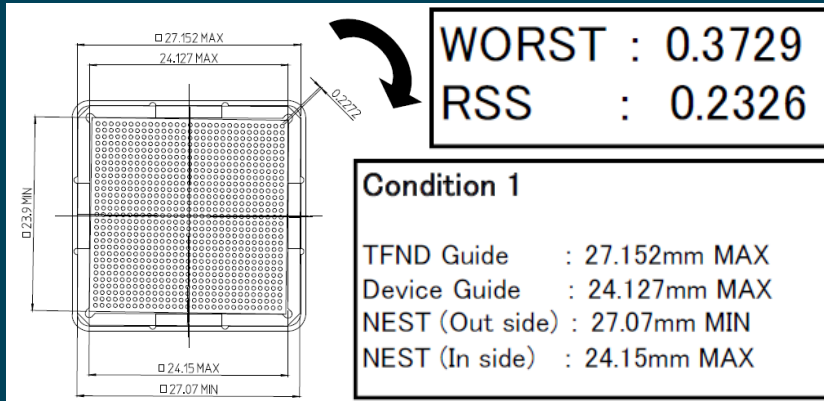


- Top plunger design → contact reliability & DUT contact surface damage
- Shape and volume of material → Wear rate / life
- Material composition → contact reliability and life



- Bottom plunger design → reliability of the pin internal structure
 - Shape
 - Plating thickness / material
 - Spring force / material
 - Biasing method
- Define the CCC performance

Learning the BGA Contactor Design



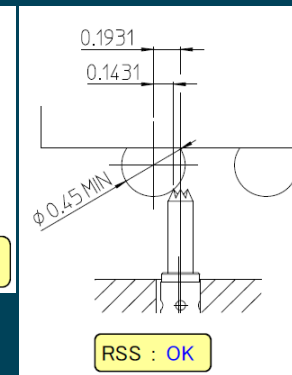
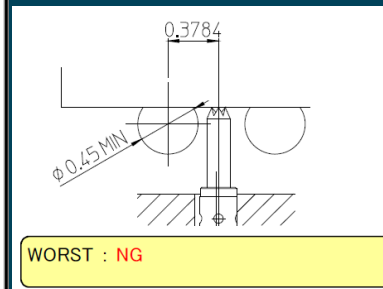
Condition 1

TFND Guide	: 27.152mm MAX
Device Guide	: 24.127mm MAX
NEST (Out side)	: 27.07mm MIN
NEST (In side)	: 24.15mm MAX

Condition 2

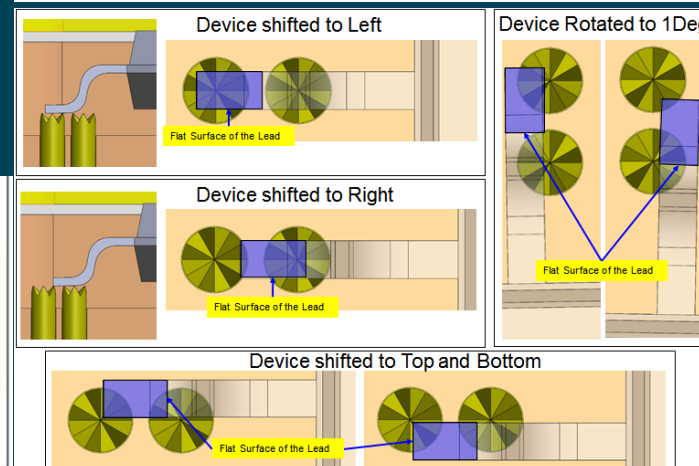
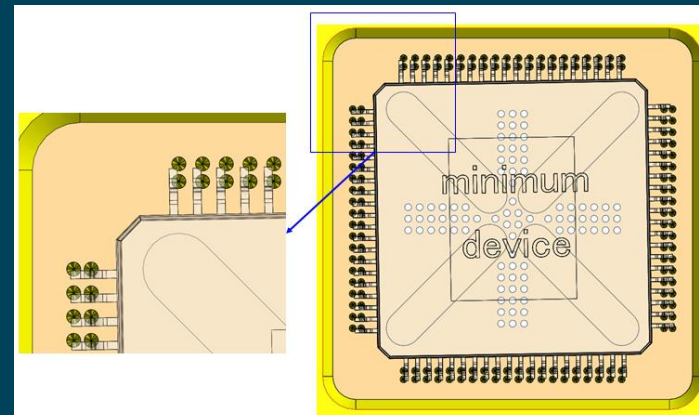
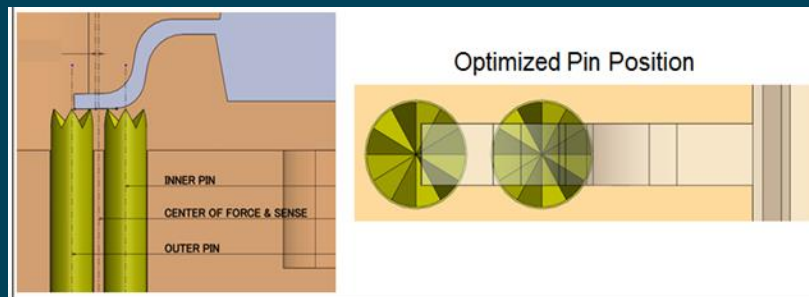
1.Alignment hole of Guide true position	: $0.01 * \sqrt{2}$
2.Alignment hole of Guide VS Dowel pin	: 0.02
3.Dowel pin for Plate true position	: $0.01 * \sqrt{2}$
4.Alignment hole of Plate true position	: $0.01 * \sqrt{2}$
5.Alignment hole of Plate VS Dowel pin	: 0.0125
6.Dowel pin for Pin Block true position	: $0.01 * \sqrt{2}$
7.Probe hole true position	: $0.01 * \sqrt{2}$
8.Probe tip accuracy	: 0.0175
9.PKG shift length	: 0.2272

- Nest guide → coarse alignment
- BGA Package guide provides the final alignment
- Positional simulation – RSS



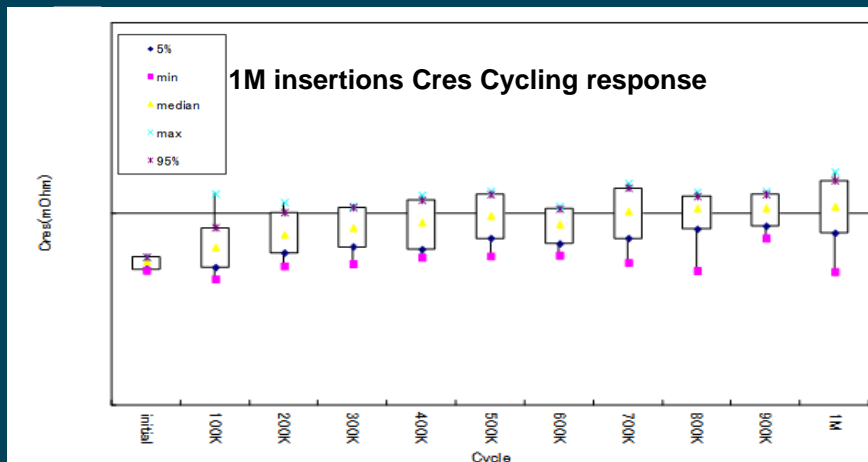
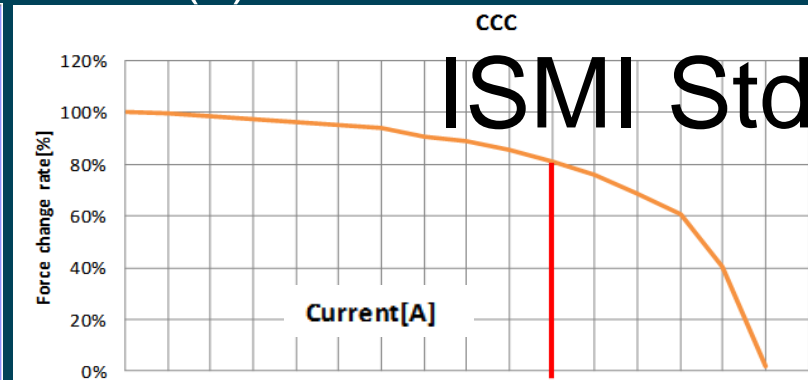
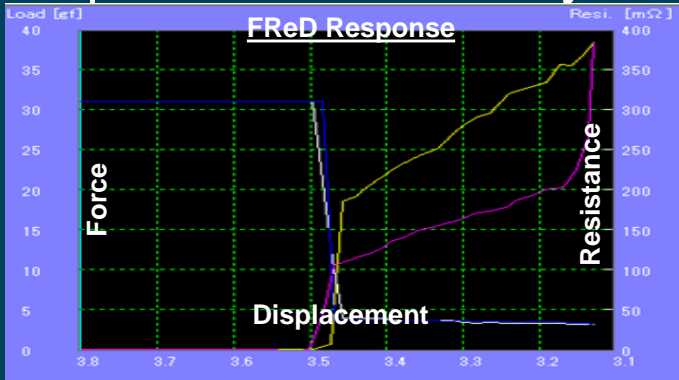
Learning the QFP Contactor Design

- Dual pin strategy
 - Common use for Kelvin and non-Kelvin application
 - Kelvin – Force/Sense
 - Non-Kelvin – Mechanical and Electrical redundancy
- Pin gap: Smaller the better
- Contact position: Optimized
 - Flat area of the lead contact
 - PCB contact area



TI Contactor Qualification Process:

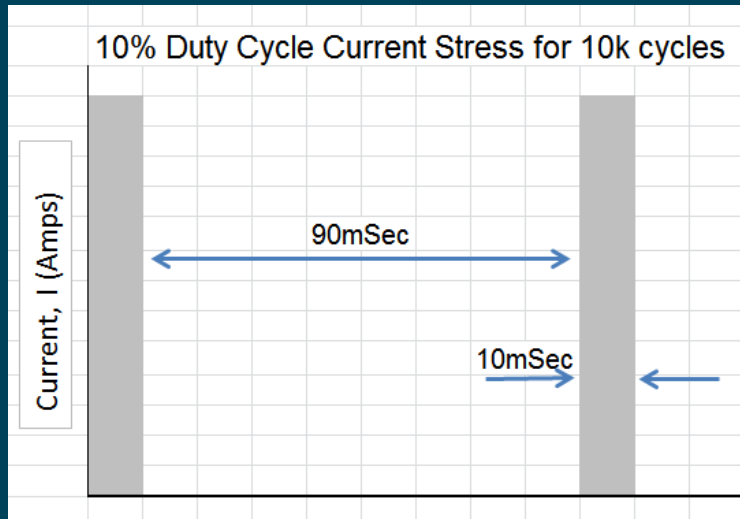
Step 1. Vendor's factory evaluation (1)



- Vendor's Pin reliability performance
 - FReD chart
 - Current capability based on ISMI test method
 - Contact resistance stability

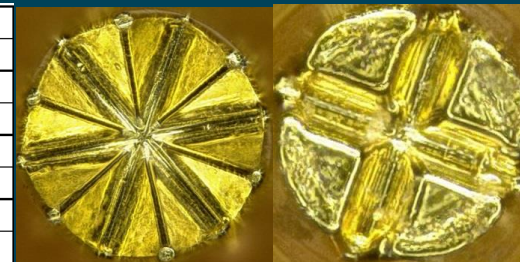
TI Contactor Qualification Process:

- Step 1. Vendor's factory evaluation (2)



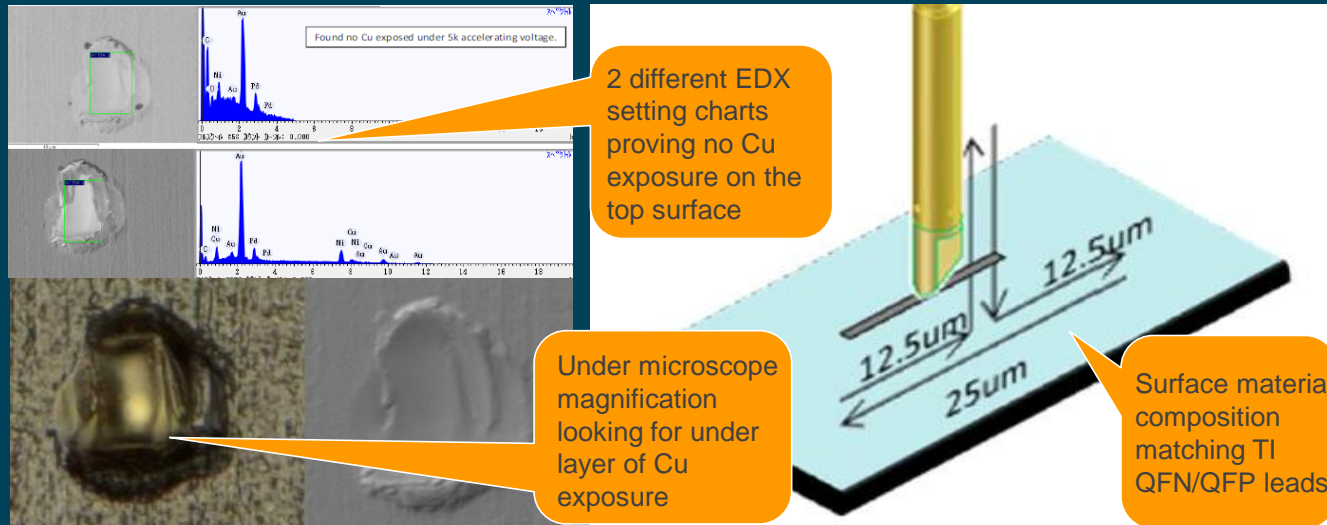
- Electrical Stress Test
 - Stress pin thru high current
 - Pass → Force drop less than 20% and no discoloration / burned tips
- Emulate device test application

Current (A)	# of pulses	On time (ms)	Off time (ms)	Duty Cycle	Temp (C)	pin force (gf)	Result
7	1	10	90	10%	32.5	24.7	OK
7	1	10	90	10%	31	25.3	OK
7	100	10	90	10%	30.6	24.8	OK
7	1,000	10	90	10%	40.9	23.3	OK
7	2,000	10	90	10%	41	21.7	OK
7	5,000	10	90	10%	39.7	22.9	OK
7	10,000	10	90	10%	42	23.7	OK



TI Contactor Qualification Process:

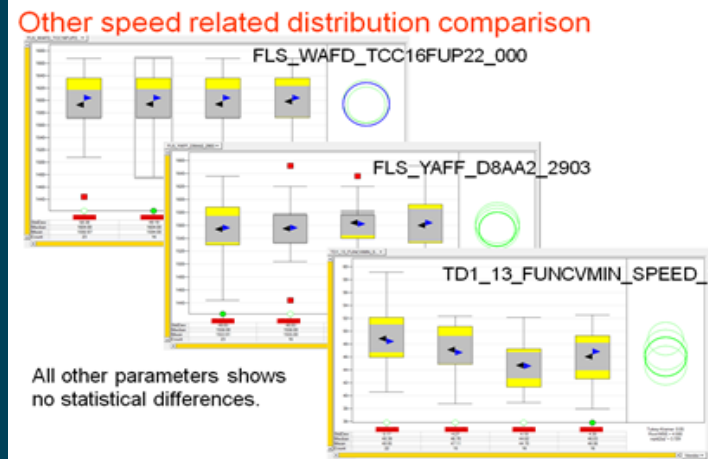
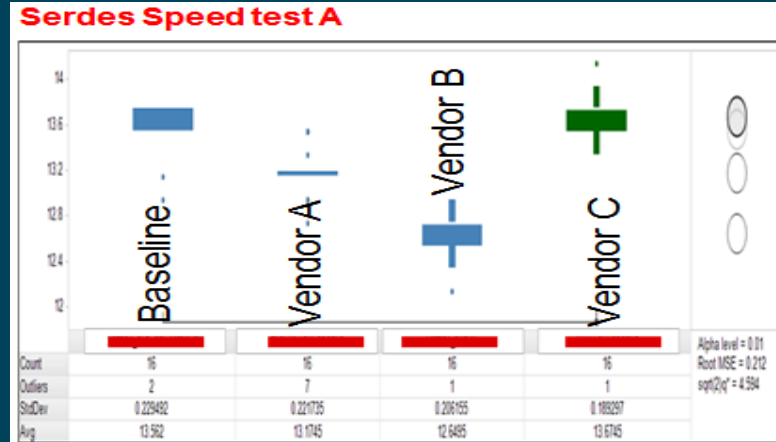
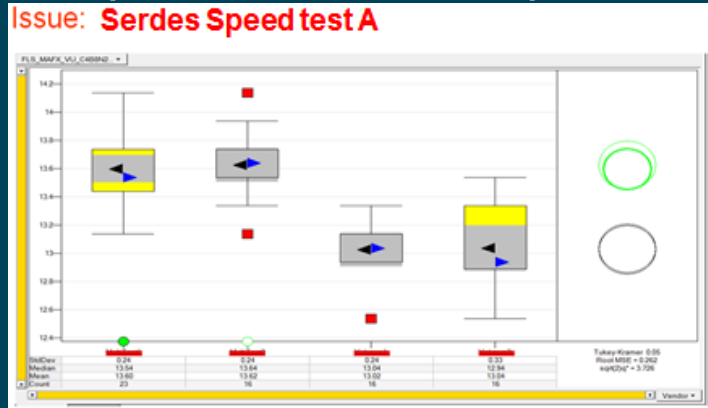
Step 1. Vendor's factory evaluation (3)



- Mechanical contact wear simulation
 - Effect of tip shape
 - pin wear rate
 - Cu exposure / damage on DUT pads/leads

TI Contactor Qualification Process:

Step 2. TI technical qualification



- Serdes loop back test is a good test method to validate solution w.r.t. its speed characteristic (High Speed Digital)
- Adopted this form of test method to ensure that qualified solution will be able to deliver the promised performance

TI Contactor Qualification Process:

Step 3. TI production qualification (1)

- Engineering Evaluation
 - Prove in using actual device
- Production qualification in A/T site (Volume data and lifetime)
 - Yield, Miss-contact, lifetime, etc.

Engineering Checkout

2013 TI Priority
Execute and gain share.

VLCT Tester 1 Loadboard 1

Site 1, Site 2, Site 4 is not working, Cotactor

Test Sequence

Unit	Site 1	Site 2	Site 1	Site 2	Site 1	Site 2
A1	Pass	Pass	Pass	Pass	Pass	Pass
A2	Pass	Pass	Pass	Pass	Pass	Pass
A3	Pass	Pass	Pass	Pass	Pass	Pass
A4	Pass	Pass	Pass	Pass	Pass	Pass
A5	Pass	Pass	Pass	Pass	Pass	Pass
A6	Pass	Pass	Pass	Pass	Pass	Pass
A7	Pass	Pass	Pass	Pass	Pass	Pass
A8	Pass	Pass	Pass	Pass	Pass	Pass
B1	Pass	Pass	Pass	Pass	Pass	Pass
B2	Pass	Pass	Pass	Pass	Pass	Pass
B3	Pass	Pass	Pass	Pass	Pass	Pass
B4	Pass	Pass	Pass	Pass	Pass	Pass
B5	Pass	Pass	Pass	Pass	Pass	Pass
B6	Pass	Pass	Pass	Pass	Pass	Pass
B7	Pass	Pass	Pass	Pass	Pass	Pass
B8	Pass	Pass	Pass	Pass	Pass	Pass

- Total 16 Bin #1 units will be tested on Site 1 and Site 2, using Baseline and labeled.
- Test unit (A1 to A8) on Site 1 and unit (B1 to B8) on Site 2.
- Re-test unit (B1 to B8) on Site 1 and unit (A8 to A1) on Site 2.
- Repeat the same test sequence for Vendor A and B Contactors.

#	Parameter	Units				
1	Manufacture					
2	Pin Model #					
3	Package		BG			
4	Pin Use		Non			
5	Status					
6	Price/pin	US\$				
7	Price/DUT Pin	US\$				
8	Socket Cost	US\$ ea@ 8 pcs				
9	Pin Drawing#					
10	Working CPH	mm	3.30	3.30	3.30	3.30
11	Force @ cph	grams	20	25	25	24.5
12	Min Pitch	mm	0.4	0.4		0.4
13	PCB Pre-Load	mm	0.20	0.20		0.2
14	DUT	mm	0.3	0.3		0.25
15	Tip Shape (PCB Side)	Radius	Radius	Flat-4		awn-rounded t
16	Tip Shape (Dut Side)	4 Pts Crown	4 Pts Crown	4 - Crown		pt crown
17	Temp	Deg C	-55 to 130	-40 to 150		to 155
18	Kelvin FIS Pin	mm	N.A.	N.A.		NA
19	Cres	mDhm	60	50		*51
20	CCC	Amps	2	2.75		2.7
21	Induct. - Self	nH				
22	Induct. - Mutual	nH				
23	Cap. - Gnd	pF				
24	Cap. - Mutual	pF				
25	Insertion Loss	GHz @ -1dB				
26	Return Loss (S11)	GHz @ -20dB				
27	DUT Tip Plating Material					
28	DUT Tip Base Material					
29	PCB Tip Plating Material					
30	PCB Tip Base Material					
31	Spring Matl					
32	Housing Matl					

Proprietary Information

Reduce to 1 Pin solution per vendor

Pin PN	Supplier	Pitch (mm)	Metall Comp / Plating	Pin Test Height (mm)	DUT / PCB TIP Shape	BW IND CCC CRES	Mis-Cont PPM	Life Cycles	Comments
a	Vendor A	0.4	BeCu / Au	5.05	Crown Green	4.75 1.09	3.9K	500K	San Purpose
b		0.5/ 0.65	BeCu / Au	5.2	Crown Green	1.00 0.10	1.24K	500K	San Purpose
c		0.5/ 0.65	Au Alloy	5.2	Crown Green	2.25 0.10	1.9K	700K	Low CRES
d		0.5/ 0.65	BeCu / Au	5.2	Crown Green	3.65 0.10	4.8K	700K	San Purpose
e	B	0.5/ 0.65	BeCu / Au	5.2	Crown Green	0.85 1.80	12.2K	700K	Drop In replacement
f	C	0.5/ 0.65	BeCu / NiRh+ECC	5.3	Crown Green	2.92 7.50	2.87K	1000K	Drop In replacement (High Cycle Life)

TI Contactor Qualification Process:

Step 3. TI production qualification (2)



- Yield, Conti%, Speed downgrade, Rescreen%, 1M insertions life and Cres reliability comparison between candidates vs. baseline

TI Contactor Qualification Process: Step 4. Qualification data review and deployment

Package Type	QFP-1						QFP-2			QFP-3		BGA-1				Legend
	Vendor B	Vendor A	Baseline	Vendor B	Vendor A	Baseline	Vendor B	Vendor A	Baseline	Vendor B	Baseline	Vendor C	Vendor B	Vendor A	Baseline	
CPH (mm)	3.3		5.05	3.3		5.05	3.3		5.05	3.3	5.05	3.3			5.05	
Temp (C)	85			85			130			N45		Room				
Test Area	FT1			FT2			PB1			PB2		PB3				
FP_Yield%	+6.0	+3.9	Ref	+6.0	+5.1	Ref	+5.7	+6.1	Ref	+3.5	Ref	+1.2	+0.8	+0.1	Ref	
FT_Yield%	+1.3	+0.9		-0.5	-1.0		+1	+0.2		+0.6		+0.1	+0.1	+0.0		
FP_Cont%	-1.2	-1.3		-0.8	-0.9		-4.8	-4.6		-0.6		-2.6	-2.6	-2.2		
FT_Cont%	-0.2	-0.2		-0.1	-0.2		-0.1	-0.2		-0.2		-0.1	-0.0	-0.0		
Re-Screen%	-6.6	-4.5		-6.4	-6.1		-7.8	-8.5		-9.9		-11.5	11.1	-9.2		



Qualification Criteria

- ✓ Cost
- ✓ Improved Performance (FP_Yield, FP_Conti%, Rescreen% & Pin life)
- ✓ Onsite Support

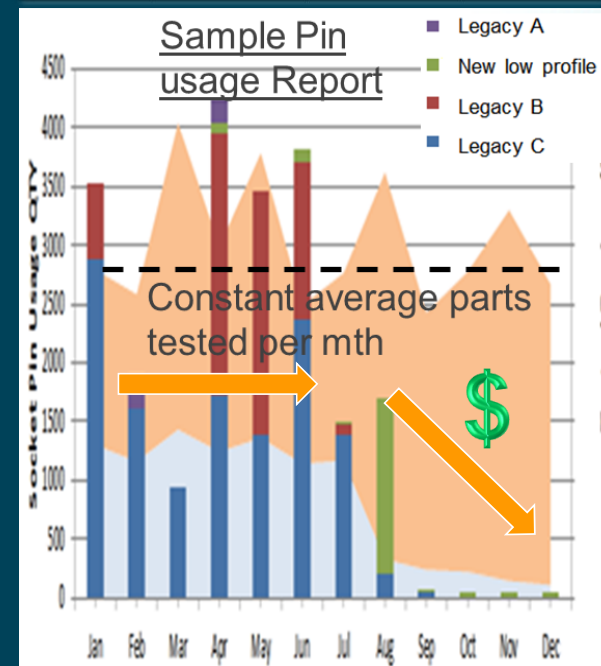
Qualification Boundary

- ✓ Temperature
- ✓ Pitch
- ✓ Test current
- ✓ Ω Trend (RDsOn/Cres)
- ✓ Test frequency / bandwidth

Summary

- Established a robust systematic qualification process
- Performance improvement
 - First Pass Yield improvement of 5%
 - Rescreen rate drops of 6%
 - ✓ Capacity recovery
 - ✓ Cost saving on labor and test equipment
- Achieving 1M or more insertion of Pin life
 - Cost saving from pin usage
 - Intangible labor cost saving
- Other intangible benefits
 - Better Yield correlation
 - Shorter Device start up time
 - Factories loading flexibility

Improvements	QFP		BGA
	General Purpose	High Current	General Purpose
First Pass Yield	5.10%	7.10%	2.90%
Rescreen	-7.40%	-9.20%	-5.30%



Acknowledgement

Texas Instruments A/T sites worldwide

