
SEVENTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 5
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BiTS 2016 Burn-in & Test Strategies Workshop

Session 5
Ashok Kabadi
Session Chair

BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 8 - 10:30 am

West Meets East & Cutting Edge

"LPDDR4 Signal & Power Performance Optimization By Hardware"
"通过测试硬件的优化来提升LPDDR4信号和电源的性能"
Yuanjun Shi - Twinsolution Technology
Xiao Yao - HiSilicon Technologies Co

"Reliability Characterization of Unpackaged (bare) die for Silicon Photonics module"
Sujata Paul, Andrew Fong, Samir Alqadhy, Huy Nguyen, Zoe Conroy - Cisco
Tom Elliot, Jag Jassal - Evans Analytical Group

"Advanced High Energy CO2 Spray Cleaning Technology for Burn-In Test Substrate Cleaning Applications"
Nelson Sorbo - Cool Clean Technologies

"Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution"
James Tong, Hisashi Ata - Texas Instruments

Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution

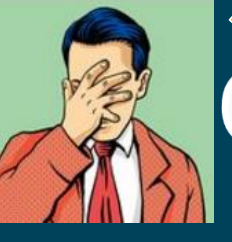
James Tong, Hisashi Ata
Texas Instruments

2016 BiTS Workshop
March 6 - 9, 2016

Contents

What's the problem?

Fix the Problem?



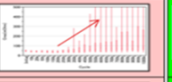
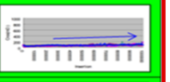
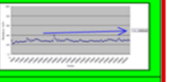
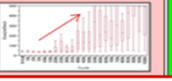
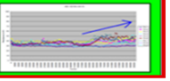
OMG

- Objective
- Main Goal

Problem Statement

- Legacy contact technologies cannot support today's test application requirements.
- Different approach to deal with the short fall from every A/T sites
  - Incompatibility performance
  - Localized support to each A/T site
  - yield correlation problem
  - Multi-factories loading limitation.
- Resulting in customized pin design by device by user.
- Work against cost reduction model to benefit TI worldwide

Legacy Contact Pin Solutions

Application	Legacy Pin [High Profile, <15GHz]		Custom Pin [High Profile, <15GHz]	
	Cost/Pin	<500K Life	Cost/Pin	~1M Life
0.4 BGA	Vendor A		-49% Vendor D	
0.5/0.65 BGA	Vendor A		-15% Vendor C	
0.8/1.0 BGA	Vendor A		-14% Vendor D	
0.5 QFP	Vendor A		-10% Vendor D	

Strategy

2014 Execute and gain share

- ✓ **High Performance pins**
  - Low Cres
  - High CCC (Current Carrying Capability)
  - High bandwidth
- ✓ **Common use across tester platforms, pin pitches and A/Ts**
  - → Volume pricing
  - → Sameness across A/Ts
- ✓ **Low COO (Low Cost, Long Life > 1,000K insertions)**
- ✓ **PCB footprint compatibility**
- ✓ **WW TI support**

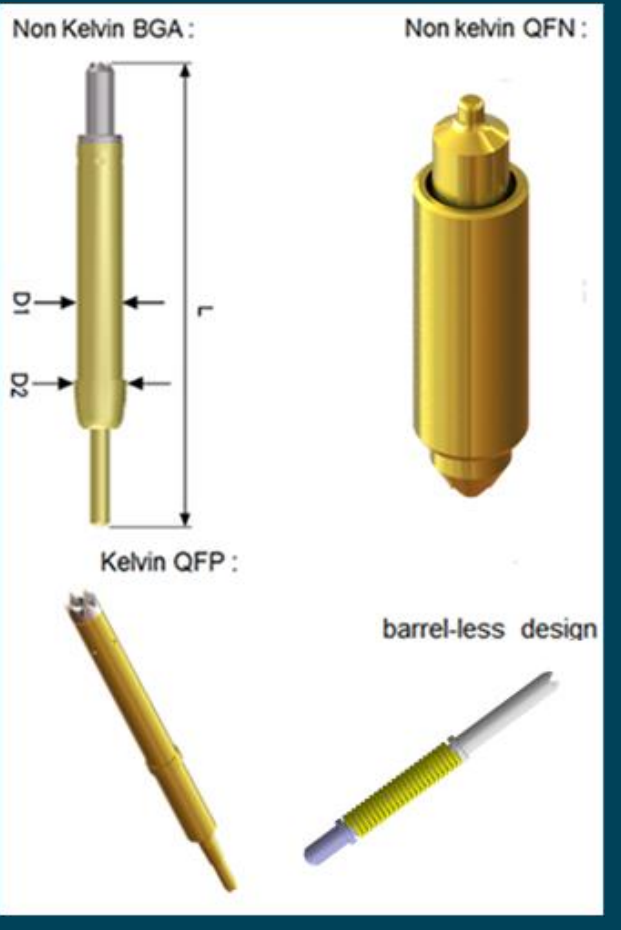
Technical Solution and Challenges

Solution

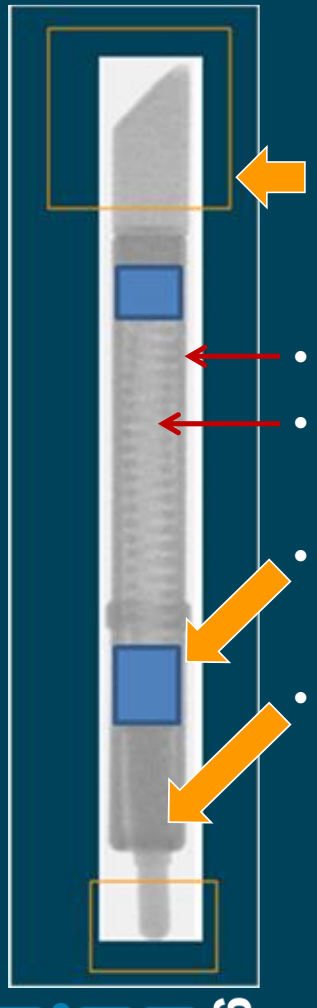
- Shorter pin resulting in less metal between the load-board and the Device-Under-Test (DUT)
- Lower pin inductance
- Better signal integrity

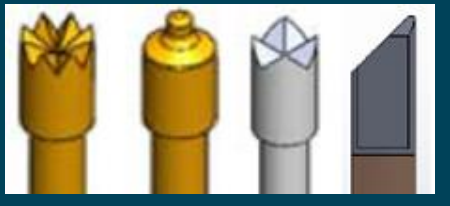
Challenges

- High current carrying capability (CCC)
- Reliable contact resistance (Cres)
- Pin manufacturability: Low cost



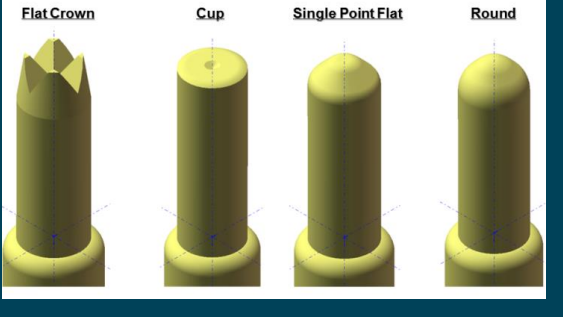
Learning the Pin Type



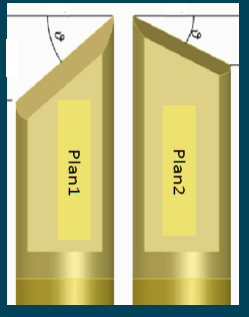


- Unlimited tip shape and design.
- Tip material: Homogenous, plated core material, etc.

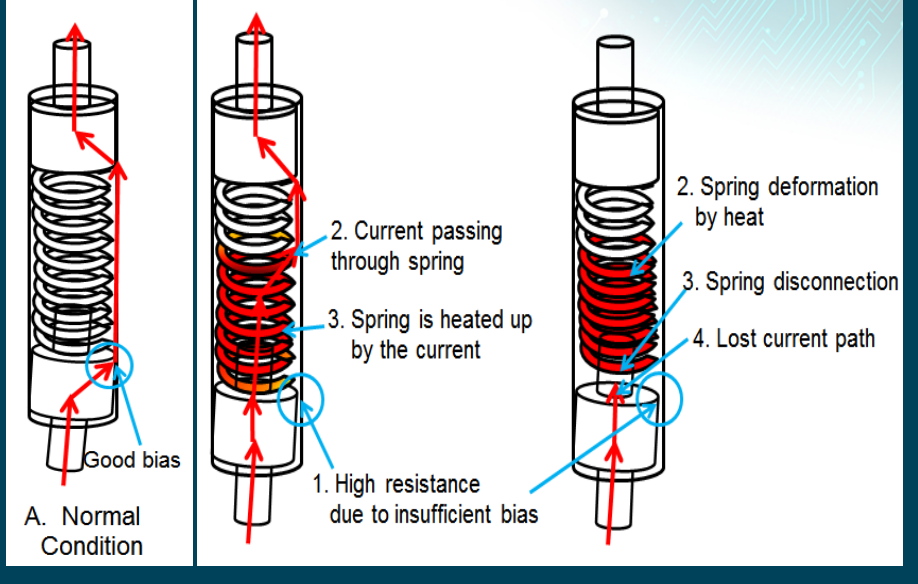
- Barrel: diameter and plating thickness
- Spring design and material: Total force, life, contact reliability and temperature rating
- Biasing mechanism
  - CRes, CCC, spring performance and lifetime
- Bottom Plunger design
  - Material
  - Unlimited Shape
  - Plating recipe
  - PCB pad damage



Learning the Pin Design

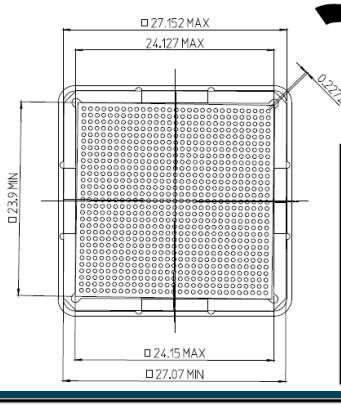


- Top plunger design → contact reliability & DUT contact surface damage
- Shape and volume of material → Wear rate / life
- Material composition → contact reliability and life



- Bottom plunger design → reliability of the pin internal structure
  - Shape
  - Plating thickness / material
  - Spring force / material
  - Biasing method
- Define the CCC performance

Learning the BGA Contactor Design



WORST : 0.3729
RSS : 0.2326

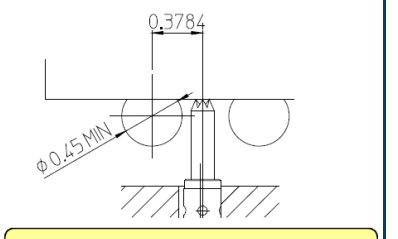
Condition 1

TFND Guide	: 27.152mm MAX
Device Guide	: 24.127mm MAX
NEST (Out side)	: 27.07mm MIN
NEST (In side)	: 24.15mm MAX

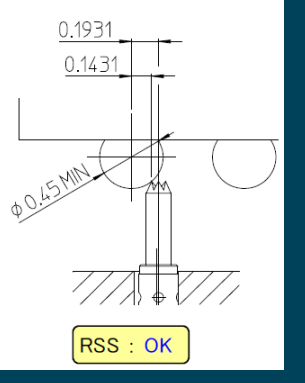
- Nest guide → coarse alignment
- BGA Package guide provides the final alignment
- Positional simulation – RSS

Condition 2

1.Alignment hole of Guide true position	: 0.01*√2
2.Alignment hole of Guide VS Dowel pin	: 0.02
3.Dowel pin for Plate true position	: 0.01*√2
4.Alignment hole of Plate true position	: 0.01*√2
5.Alignment hole of Plate VS Dowel pin	: 0.0125
6.Dowel pin for Pin Block true position	: 0.01*√2
7.Probe hole true position	: 0.01*√2
8.Probe tip accuracy	: 0.0175
9.PKG shift length	: 0.2272



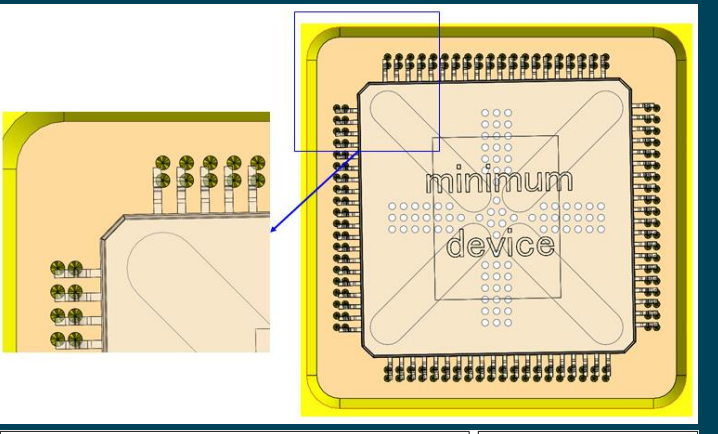
WORST : NG

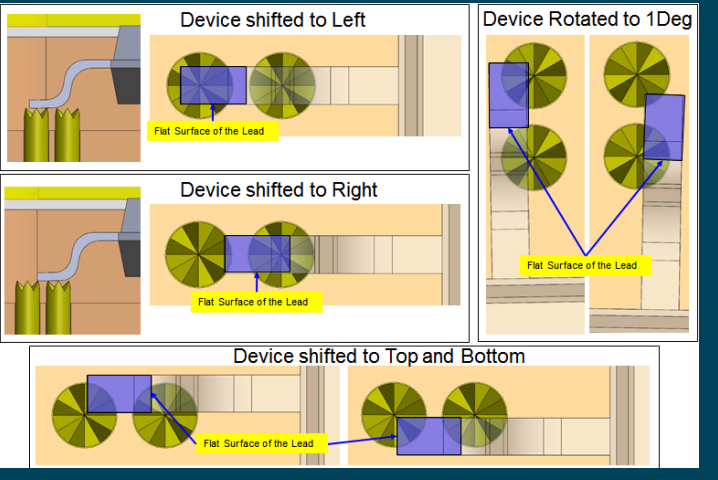


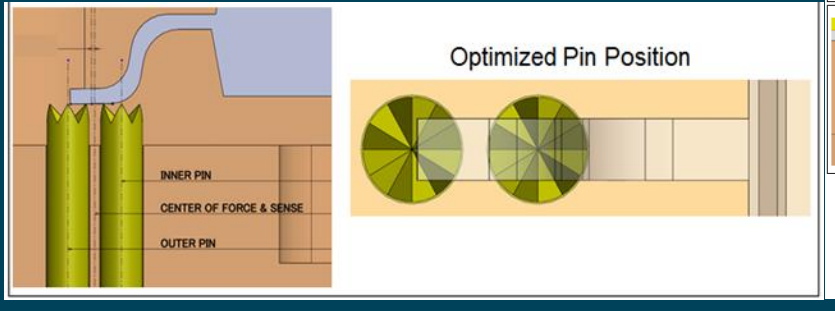
RSS : OK

Learning the QFP Contactor Design

- Dual pin strategy
  - Common use for Kelvin and non-Kelvin application
    - Kelvin – Force/Sense
    - Non-Kelvin – Mechanical and Electrical redundancy
- Pin gap: Smaller the better
- Contact position: Optimized
  - Flat area of the lead contact
  - PCB contact area

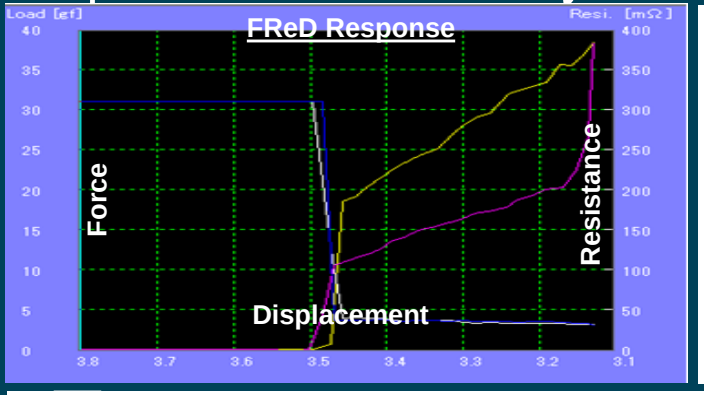


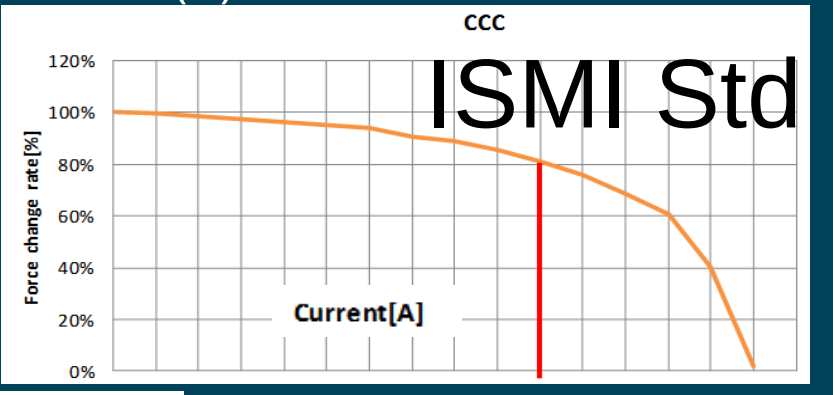


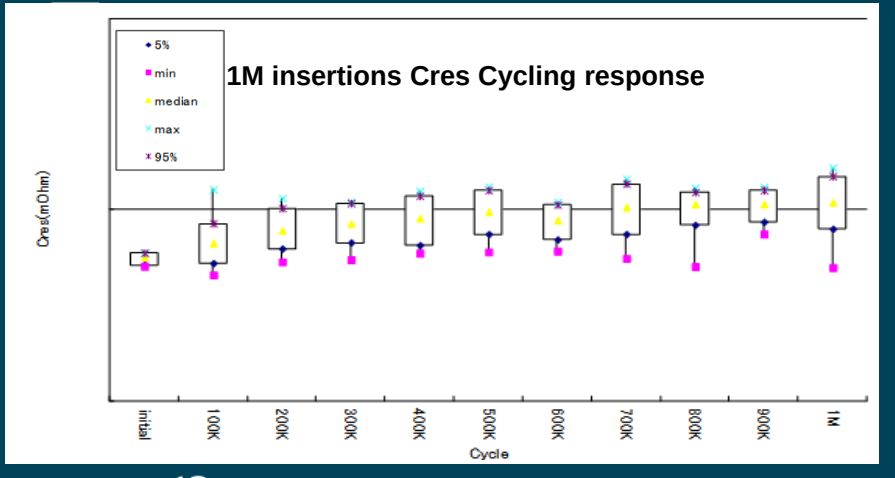


TI Contactor Qualification Process:

Step 1. Vendor's factory evaluation (1)



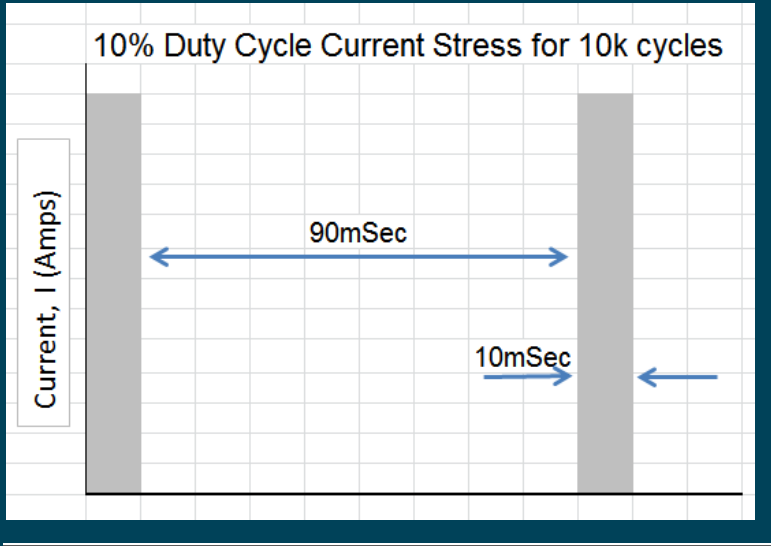




- Vendor's Pin reliability performance
  - FReD chart
  - Current capability based on ISMI test method
  - Contact resistance stability

TI Contactor Qualification Process:

- Step 1. Vendor's factory evaluation (2)

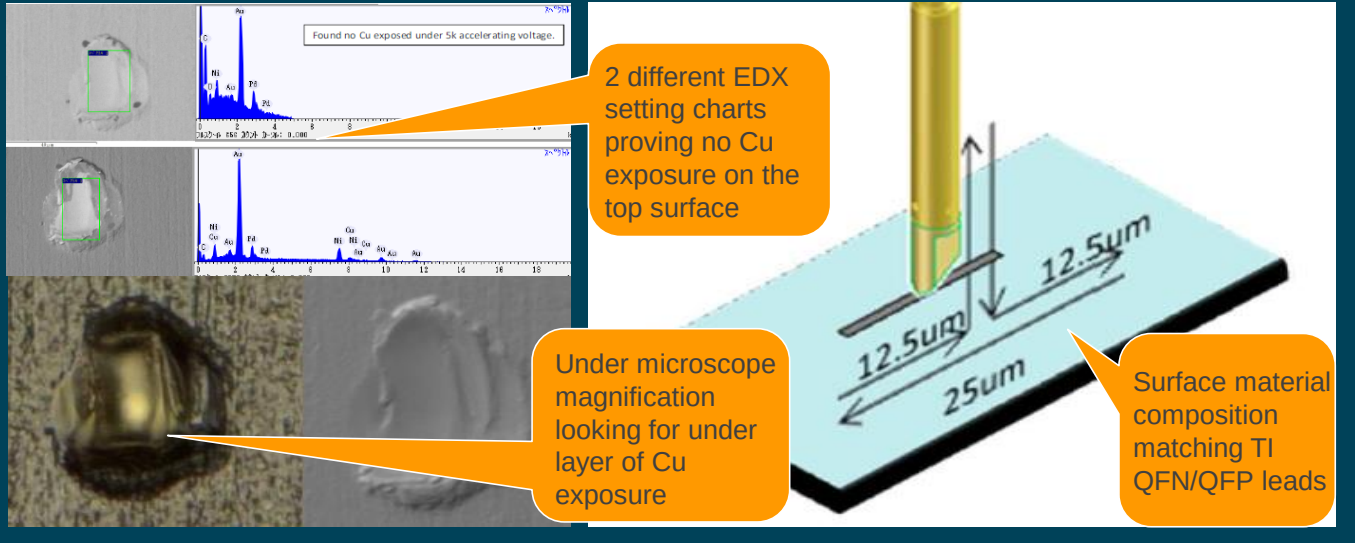


- Electrical Stress Test
  - Stress pin thru high current
  - Pass → Force drop less than 20% and no discoloration / burned tips
- Emulate device test application

Current (A)	# of pulses	On time (ms)	Off time (ms)	Duty Cycle	Temp (C)	pin force (gf)	Result
7	1	10	90	10%	32.5	24.7	OK
7	1	10	90	10%	31	25.3	OK
7	100	10	90	10%	30.6	24.8	OK
7	1,000	10	90	10%	40.9	23.3	OK
7	2,000	10	90	10%	41	21.7	OK
7	5,000	10	90	10%	39.7	22.9	OK
7	10,000	10	90	10%	42	23.7	OK

TI Contactor Qualification Process:

Step 1. Vendor's factory evaluation (3)

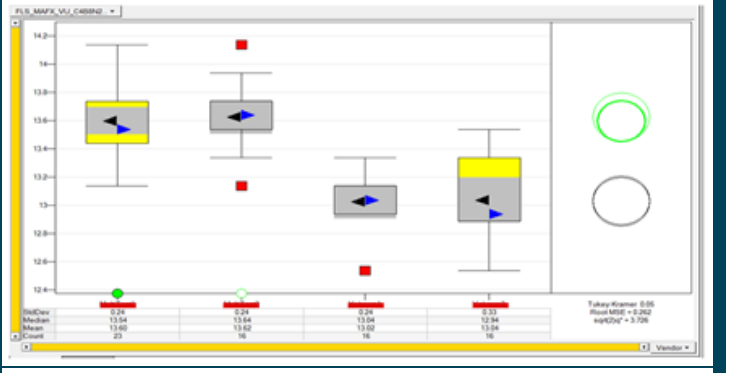


- Mechanical contact wear simulation
  - Effect of tip shape
  - pin wear rate
  - Cu exposure / damage on DUT pads/leads

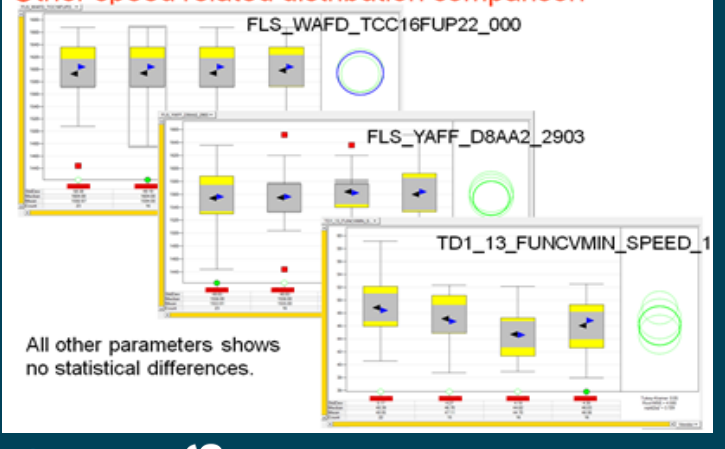
TI Contactor Qualification Process:

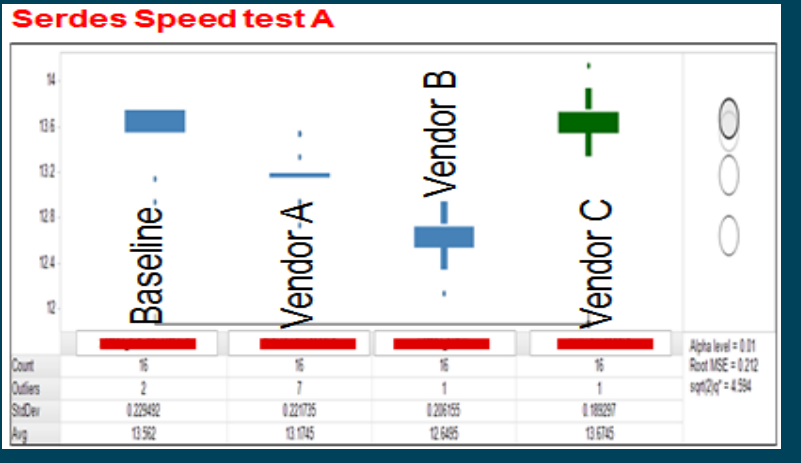
Step 2. TI technical qualification

Issue: **Serdes Speed test A**



Other speed related distribution comparison



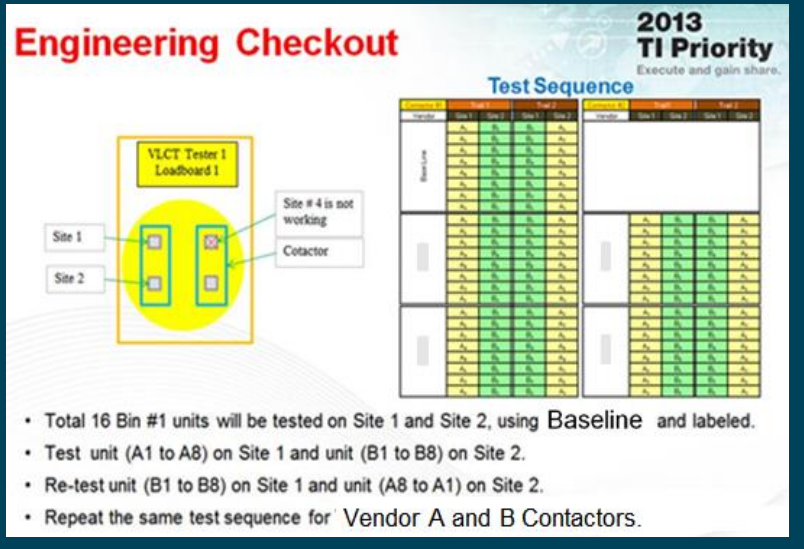


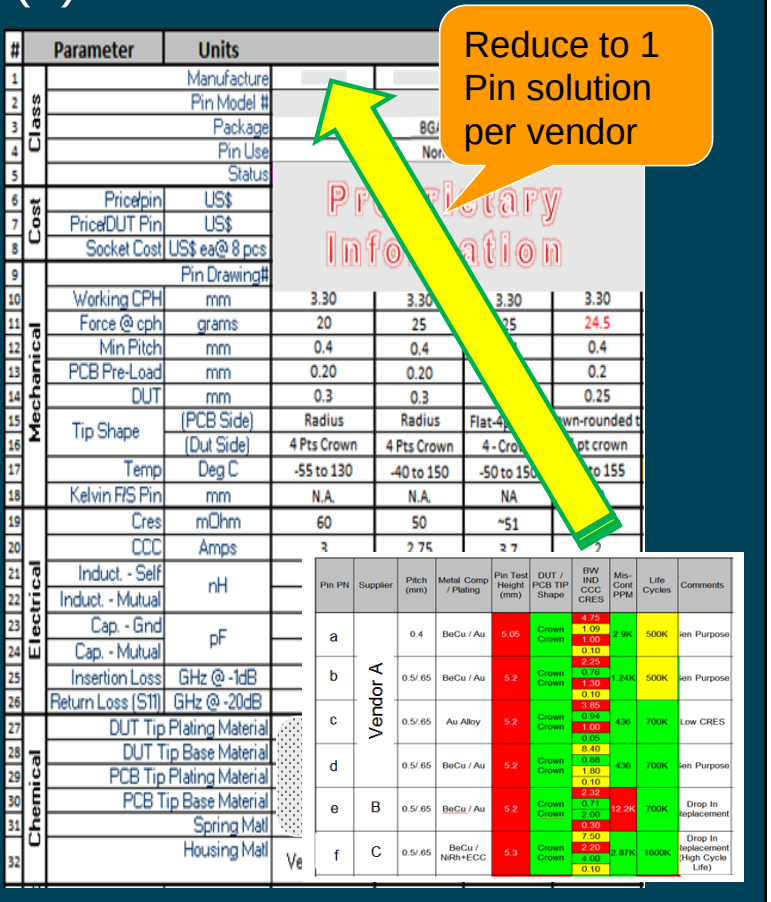
- Serdes loop back test is a good test method to validate solution w.r.t. it's speed characteristic (High Speed Digital)
- Adopted this form of test method to ensure that qualified solution will be able to deliver the promised performance

TI Contactor Qualification Process:

Step 3. TI production qualification (1)

- Engineering Evaluation
  - Prove in using actual device
- Production qualification in A/T site (Volume data and lifetime)
  - Yield, Miss-contact, lifetime, etc.





TI Contactor Qualification Process:

Step 3. TI production qualification (2)

- Yield, Conti%, Speed downgrade, Rescreen%, 1M insertions life and Cres reliability comparison between candidates vs. baseline

TI Contactor Qualification Process:

Step 4. Qualification data review and deployment

Package Type	QFP-1						QFP-2			QFP-3		BGA-1			
Eval. Contactor / Base Line Contactor	Vendor B	Vendor A	Baseline	Vendor B	Vendor A	Baseline	Vendor B	Vendor A	Baseline	Vendor B	Baseline	Vendor C	Vendor B	Vendor A	Baseline
CPH (mm)	3.3		5.05	3.3		5.05	3.3		5.05	3.3	5.05	3.3			5.05
Temp (C)	85			85			130			N45		Room			
Test Area	FT1			FT2			PB1			PB2		PB3			
FP-Yield%	+6.0	+3.9		+6.0	+5.1		+5.7	+6.1		+3.5		+1.2	+0.8	+0.1	
FT_Yield%	+1.3	+0.9		-0.5	-1.0		+.1	+0.2		+0.6		+0.1	+0.1	+0.0	
FP_Cont%	-1.2	-1.3	Ref	-0.8	-0.9	Ref	-4.8	-4.6	Ref	-0.6	Ref	-2.6	-2.6	-2.2	Ref
FT_Cont%	-0.2	-0.2		-0.1	-0.2		-0.1	-0.2		-0.2		-0.1	-0.0	-0.0	
Re-Screen%	-6.6	-4.5		-6.4	-6.1		-7.8	-8.5		-9.9		-11.5	11.1	-9.2	

Exceed requirement

Better than Baseline but fall short of expectation

Not meeting expectation

Qualification Criteria

- ✓ Cost
- ✓ Improved Performance (FP_Yield, FP_Conti%, Rescreen% & Pin life)
- ✓ Onsite Support

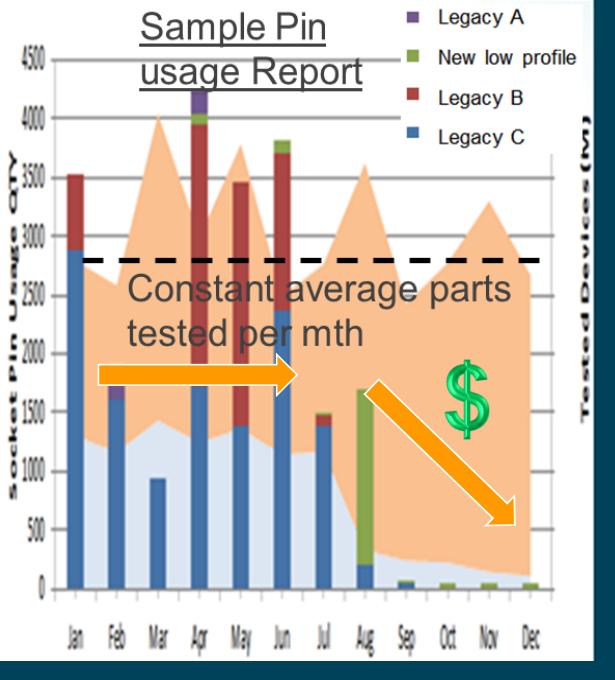
Qualification Boundary

- ✓ Temperature
- ✓ Pitch
- ✓ Test current
- ✓ Ω Trend (RDsOn/Cres)
- ✓ Test frequency / bandwidth

Summary

- Established a robust systematic qualification process
- Performance improvement
  - First Pass Yield improvement of 5%
  - Rescreen rate drops of 6%
    - ✓Capacity recovery
    - ✓Cost saving on labor and test equipment
- Achieving 1M or more insertion of Pin life
  - Cost saving from pin usage
  - Intangible labor cost saving
- Other intangible benefits
  - Better Yield correlation
  - Shorter Device start up time
  - Factories loading flexibility

Improvements	QFP		BGA
	General Purpose	High Current	General Purpose
First Pass Yield	5.10%	7.10%	2.90%
Rescreen	-7.40%	-9.20%	-5.30%



Acknowledgement

Texas Instruments A/T sites worldwide

Texas Instruments LBEs and WPL

Delta Design

iDi

ADVANTEST

YOKOWO

Enplas

Xcerra

LEENO

NHKニッパツ

Johnstech

EQT