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BiTS
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 5
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BiTS 2016 Burn-in & Test Strategies Workshop

Session 5
Ashok Kabadi
*Session Chair*

BiTS Workshop 2016 Schedule

# Performance Day

Tuesday March 8 - 10:30 am

## West Meets East & Cutting Edge

"LPDDR4 Signal & Power Performance Optimization By Hardware"
"通过测试硬件的优化来提升LPDDR4信号和电源的性能"
Yuanjun Shi - Twinsolution Technology
Xiao Yao - HiSilicon Technologies Co

"Reliability Characterization of Unpackaged (bare) die for Silicon Photonics module"
Sujata Paul, Andrew Fong, Samir Alqadhy, Huy Nguyen, Zoe Conroy - Cisco
Tom Elliot, Jag Jassal - Evans Analytical Group

"Advanced High Energy CO2 Spray Cleaning Technology for Burn-In Test Substrate Cleaning Applications"
Nelson Sorbo - Cool Clean Technologies

"Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution"
James Tong, Hisashi Ata - Texas Instruments

BiTS 2016 Burn-in & Test Strategies Workshop

# LPDDR4 Signal & Power Performance Optimization By Hardware

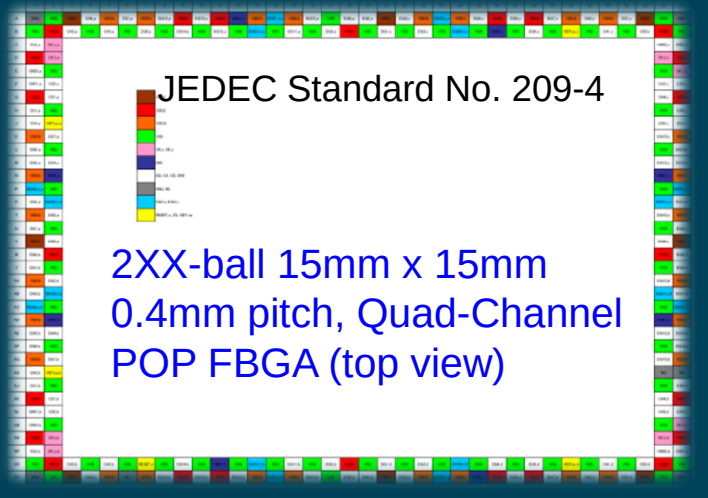
Yuanjun Shi / Twinsolution R&D
Xiao Yao / Hisilicon Test Solution R&D


2015 BiTS Workshop
Shanghai
October 21, 2015


# Contents

- DDR4 JEDEC Standard
- LPDDR4 PCB Channel & Socket SI Simulation
- LPDDR4 PCB and Socket Power Integrity Simulation
- Summary

# DDR4 JEDEC Standard




**Partial Enlarge Map of DDR**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| A | DNU | VSS | VDD1 | CA4_a | VDDQ | ZQ1_a | VDDQ | DQ15_a | VDD2 | DQ13_a |
| B | VSS | VDD2 | CA3_a | VSS | CA5_a | VSS | ZQ0_a | VSS | DQ14_a | VSS |

This case only study one group signal pin across all four group signal pins, and only include DQ pin.

| Symbol | Type | Description |
|---|---|---|
| CK_t_A, CK_c_A, CK_t_B, CK_c_B | Input | Clock |
| CA[5:0]_A CA[5:0]_B | Input | Command/Address Inputs |
| DQ[15:0]_A, DQ[15:0]_B | I/O | Data Input/Output: Bi–direction data bus. |
| DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B | I/O | Data Strobe |
| VDDQ, VDD1, VDD2 | Supply | Power Supplies |
| VSS, VSSQ | GND | GND |

# DDR4 JEDEC Standard

Clock Jitter Specification

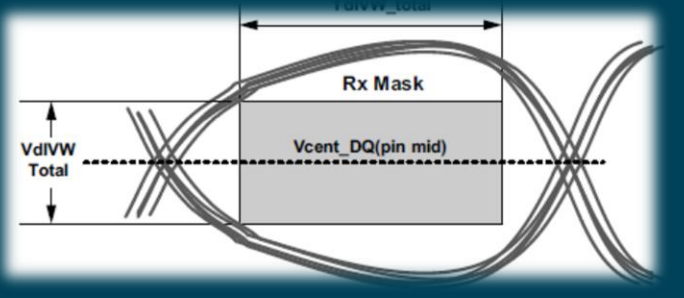
Table 88 — Clock AC Timings

| Parameter | Symbol | LPDDR4-1600 | | LPDDR4-2400 | | LPDDR4-3200 | | LPDDR4-4266 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| Clock Timing | | | | | | | | | | | |
| Clock period jitter | tJIT(per) | -70 | 70 | -50 | 50 | -40 | 40 | - | TBD | ps | |

Eye Diagram Specification

| | | 1600/1867[A] | | 2133/2400 | | 3200 | | 4266 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | min | max | | |
| VdIVW_total | Rx Mask voltage - p-p total | - | 140 | - | 140 | - | 140 | - | 120 | mV | 1,2,3,5 |
| TdIVW_total | Rx timing window total (At VdIVW voltage levels) | - | 0.22 | - | 0.22 | - | 0.25 | - | 0.25 | UI* | 1,2,4,5 |

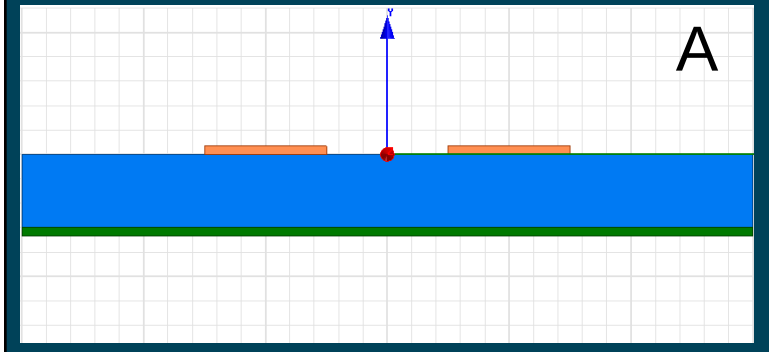
Eye diagrams are a very successful way of quickly and intuitively assessing the quality of a digital signal, for example **Overlaying of bit** and **noise level**. So Eye diagrams is a very important tools to analysis signal integrity of high speed interconnectors. On other hand we also can utilize the Eye diagram to minimize the delaying of bit as well as the transmission performance of system.



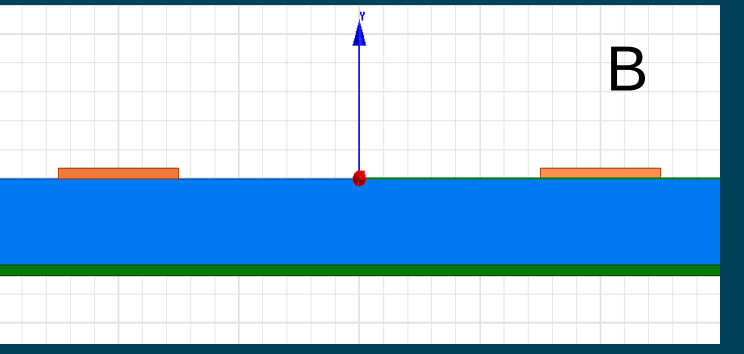
# LPDDR4 PCB Channel & Socket SI Simulation

- PCB routing optimization
- Single Bit Performance
- S-Parameter Comparison Across Different Socket Structure
- Eyediagm analysis across different socket structure

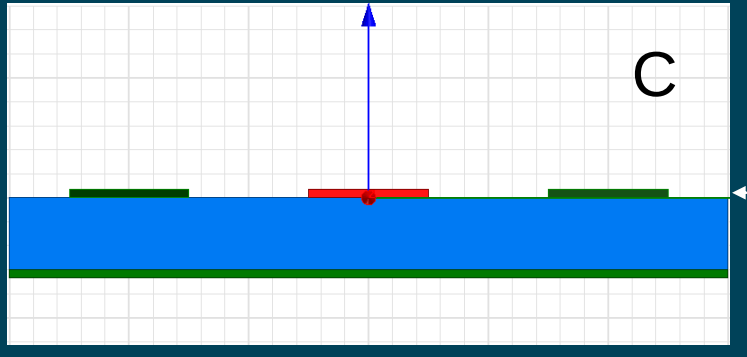
# PCB Routing Optimization




1W （1 Time/1倍线宽）




3W （3 Times/3倍线宽）




CPW （Coplanar waveguide/共面波导）

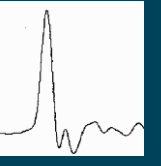
# Cross Talk Simulation Circuitry

Pulse Drive Signal

Active Line

Near End

Far End

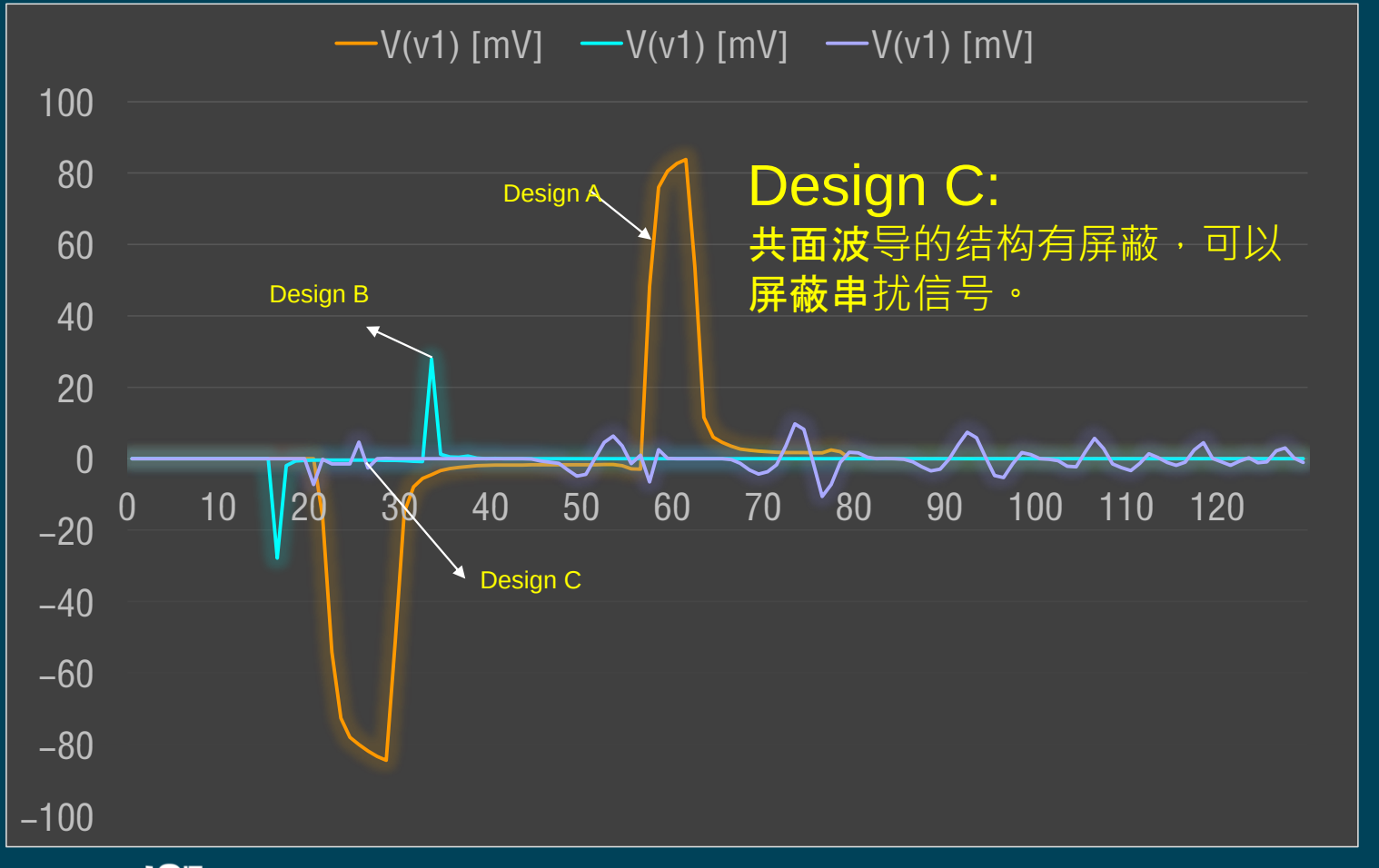


Quite Line

Measurement

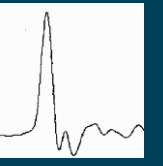
Drive a pulse from active line, and using the voltage measurement probe to check the far end cross talk, and compare with different design.

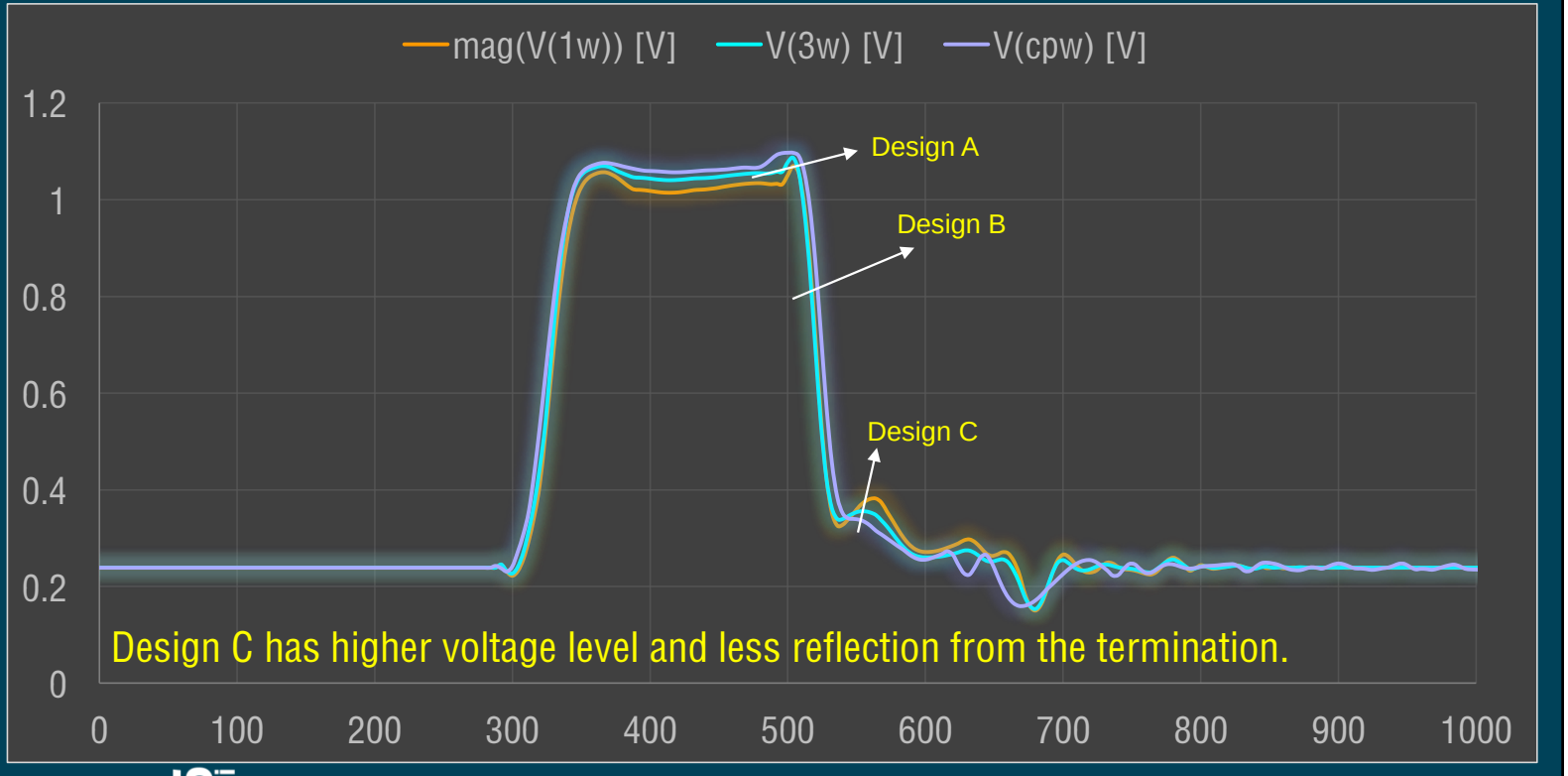
# PCB Cross Talk



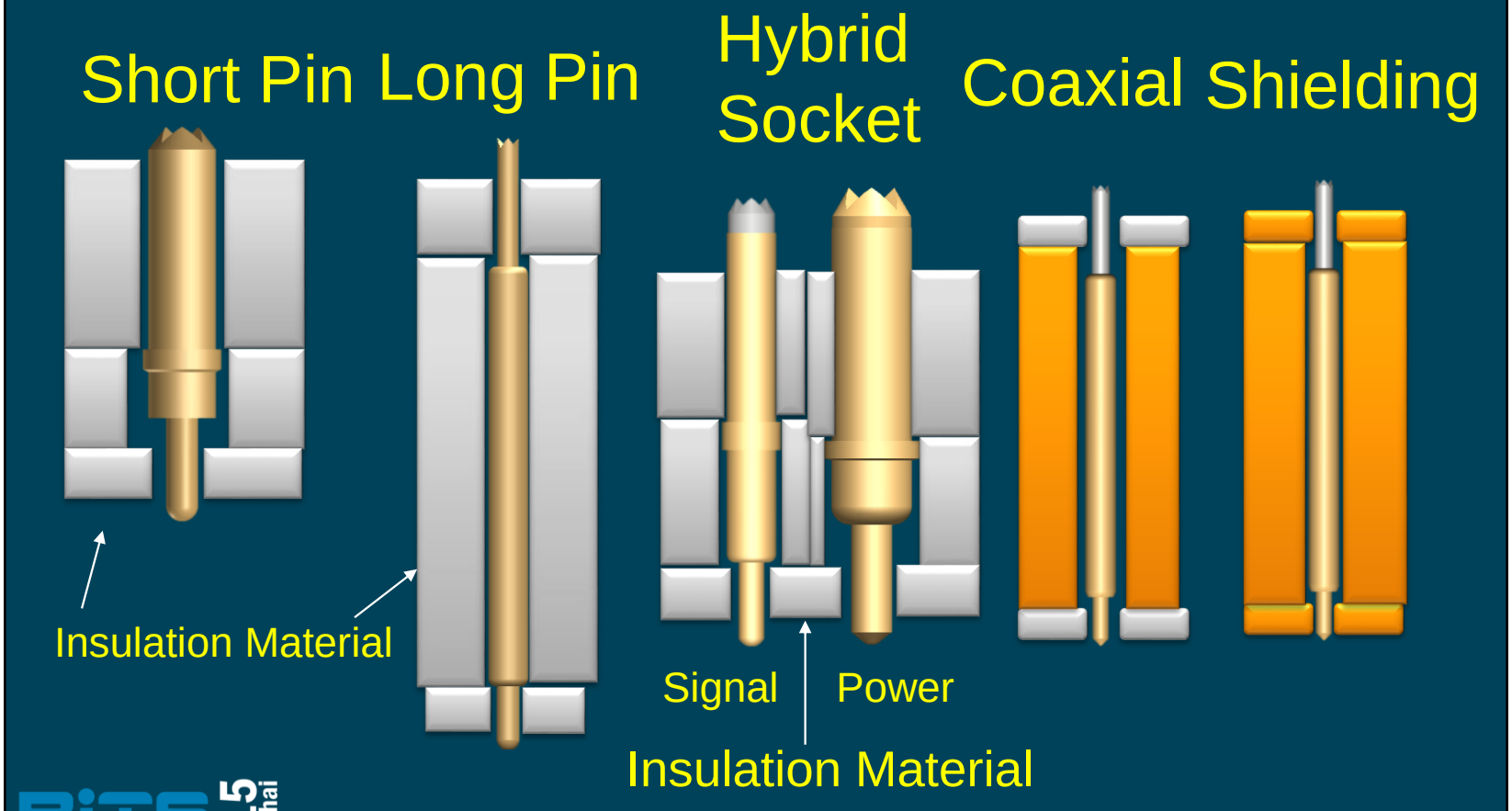
# Single Bit Simulation Circuitry


Measurement





# Socket Structure

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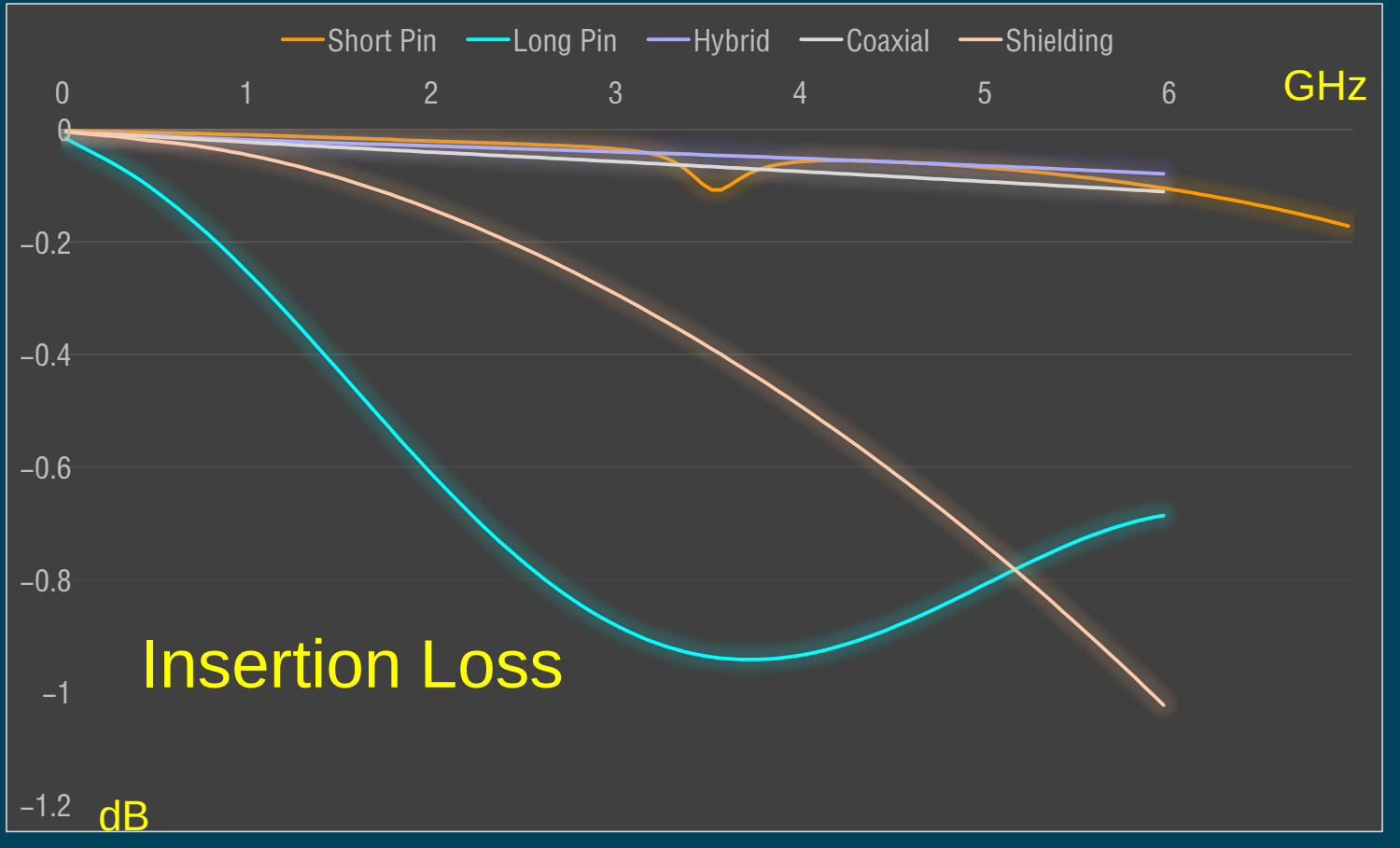
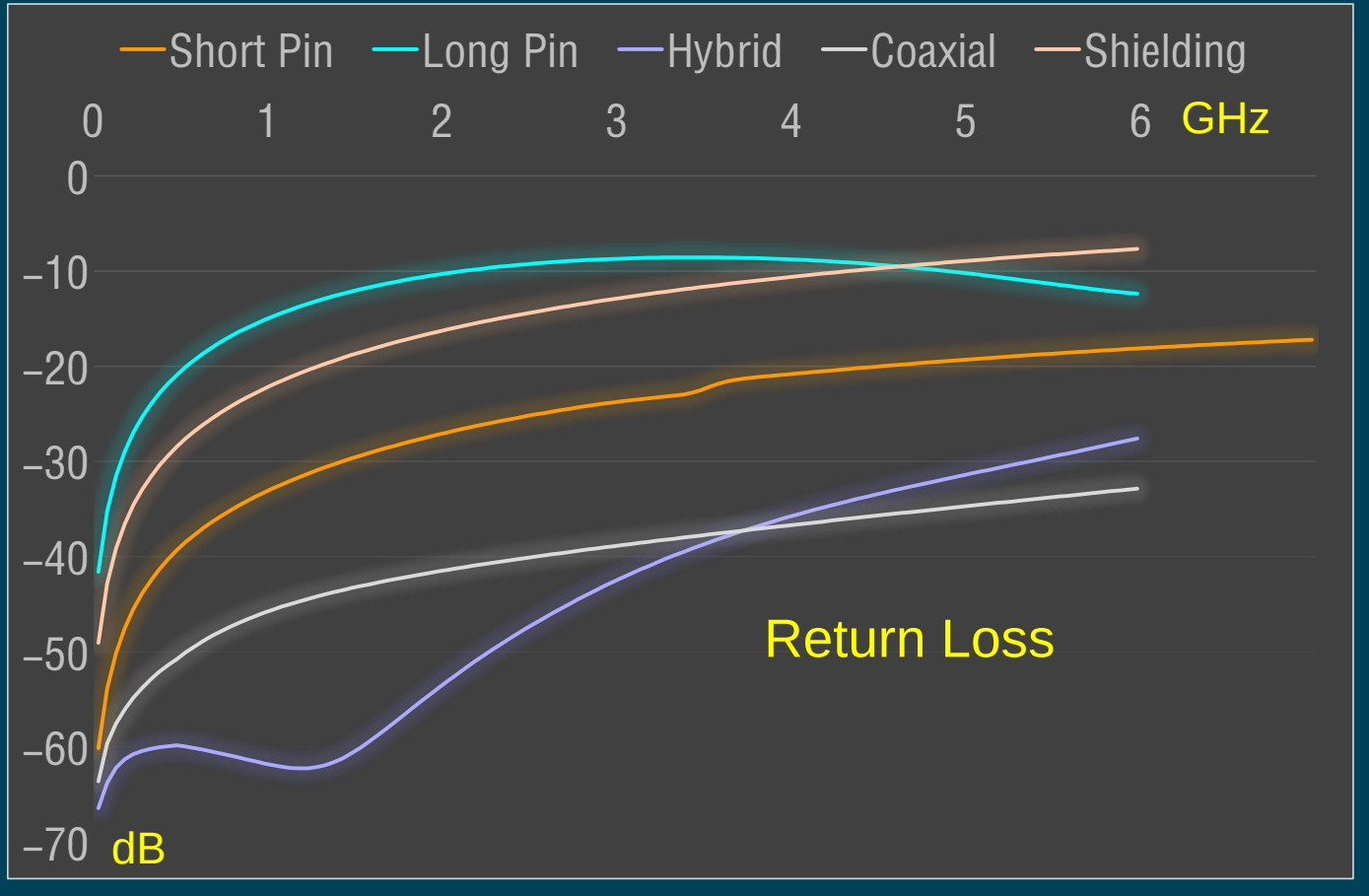
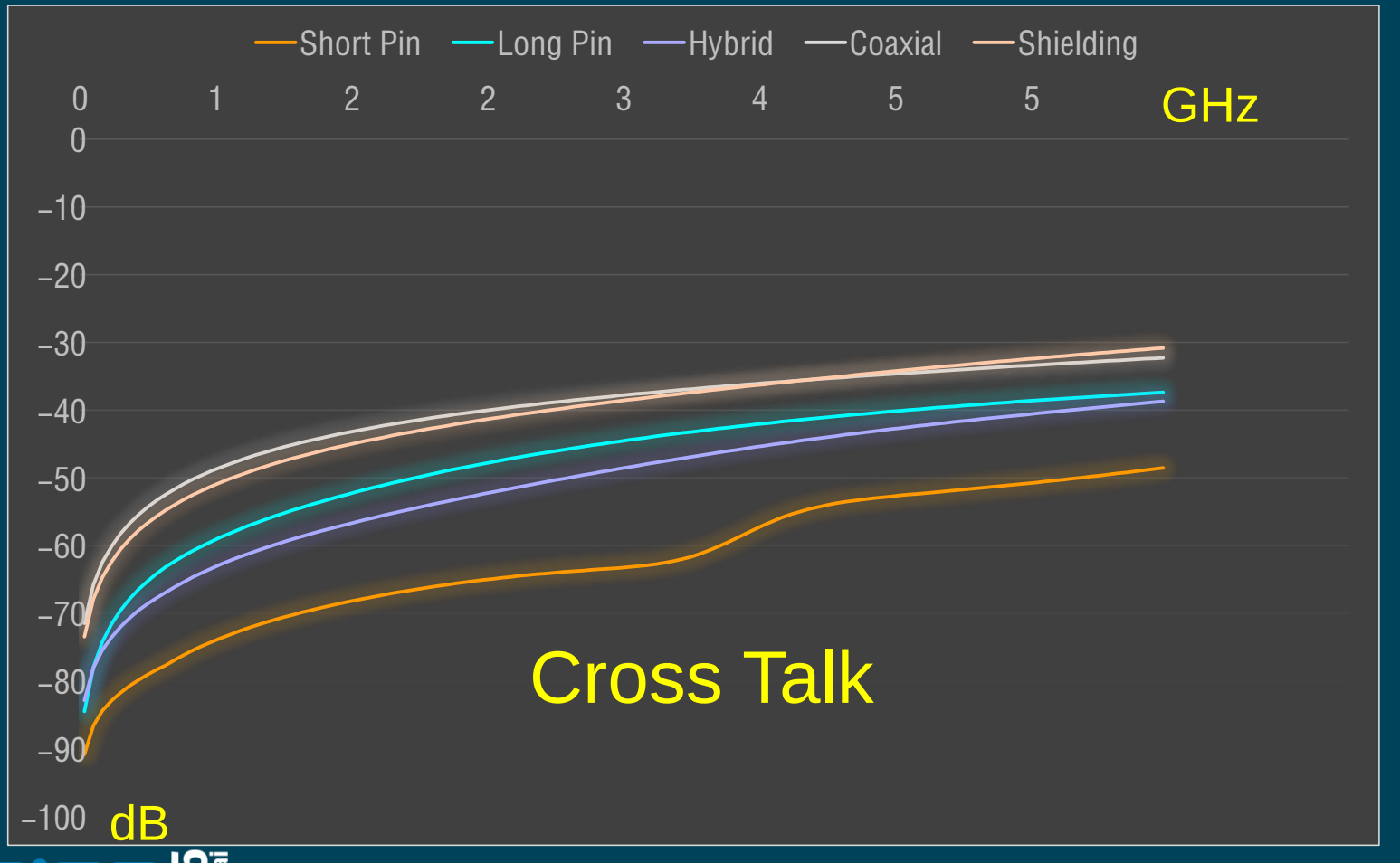
# Socket S-Parameters



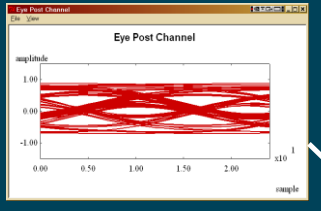
# Socket S-Parameters



# Socket S-Parameters



# Eye Diagram Loop




Eye-Probe

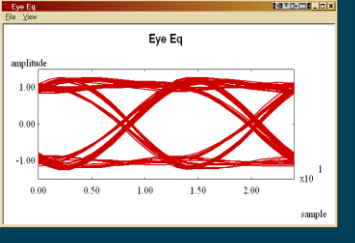
DDR

Package

DDR Controller

Package

Socket

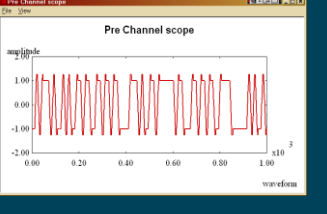



Board

Channel Adaptation

Pattern Generator

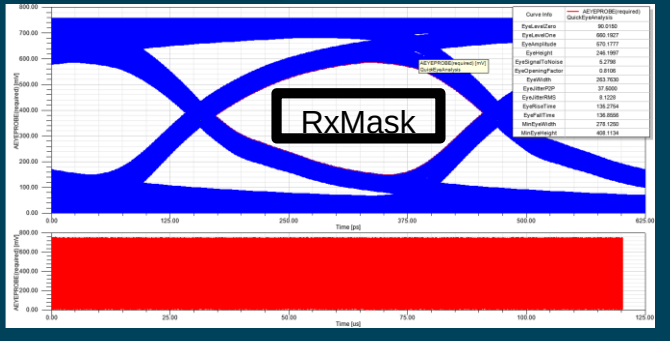
Encoder



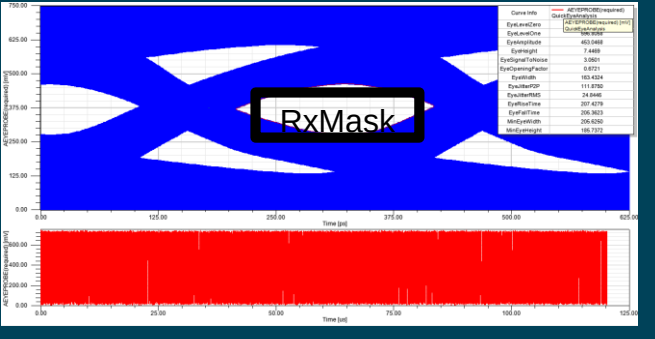

Pre-emphasis / Driver

# Eye diagram Compare

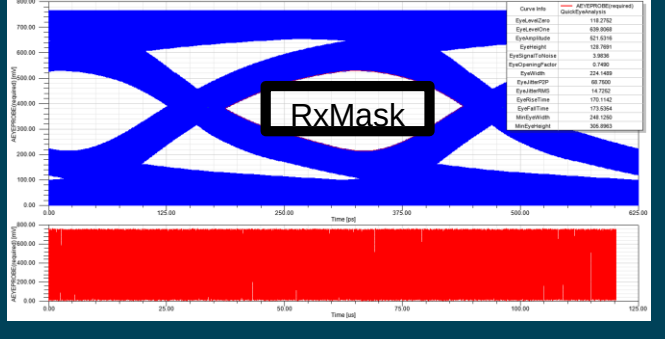
Short Pin



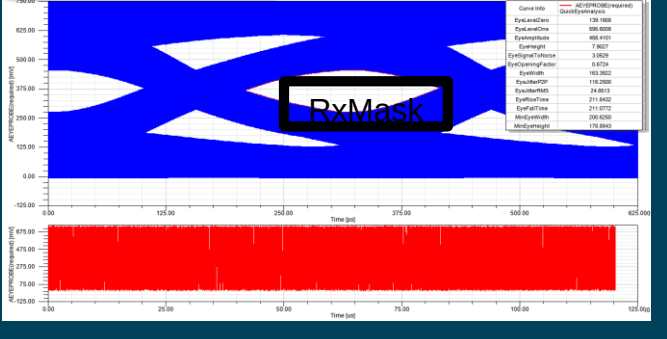

Long Pin




Hybrid Pin




Shield



# Eye diagram Summary

| Structure | Jitter | VdiVW mV |
|---|---|---|
| Short Pin | 0.038 | 247 |
| Long Pin | 0.112 | 7.5 |
| Hybrid | 0.069 | 129 |
| Coaxial | 0.031 | 298 |
| Shielding | 0.117 | 7.9 |

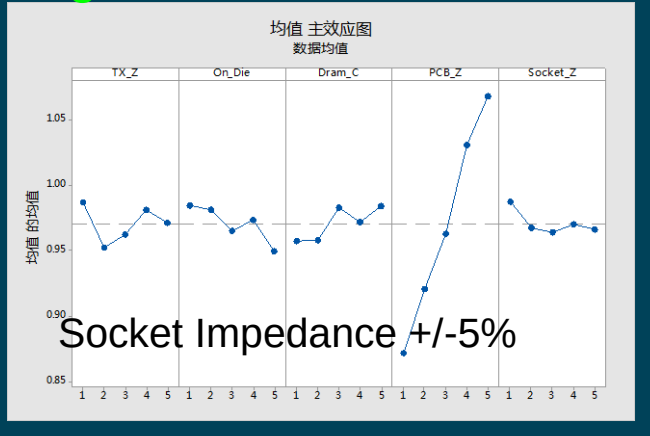
Jitter Spec: 0.04
TdivW: 79ps
VdiVW: 140mV

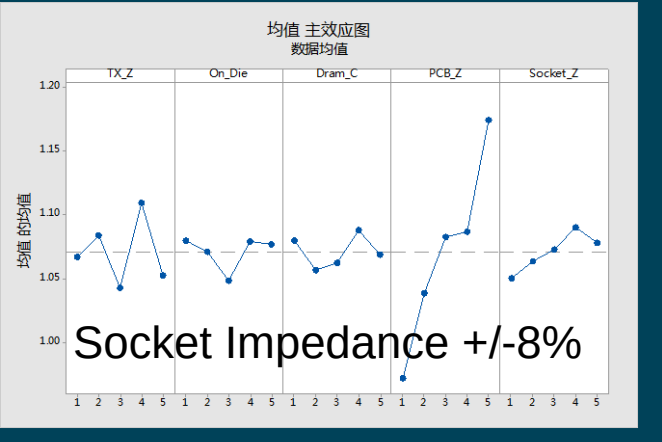
# High volume manufacturing sensitivity analysis

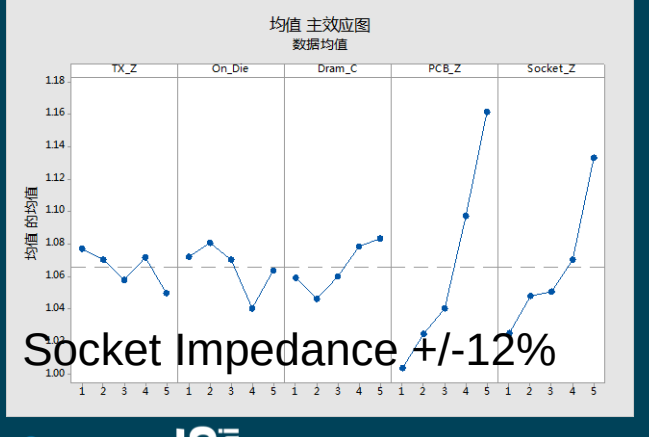
| Channel Parameters | Variation |
|---|---|
| Tx driver impedance (ohm) | 34 +/– 10% |
| On–die–termination (ohm) | 60 +/– 20% |
| DRAM Ci (pF) | 2 +/– 10% |
| PCB trace impedance (ohm) | 55 +/– 15% |
| Socket Impedance(ohm) | 50+/–5% |

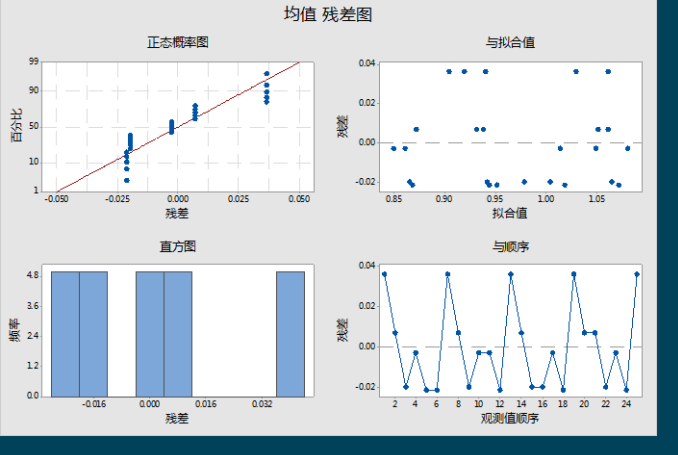
# High volume manufacturing sensitivity analysis

## Taguchi DOE/田中实验

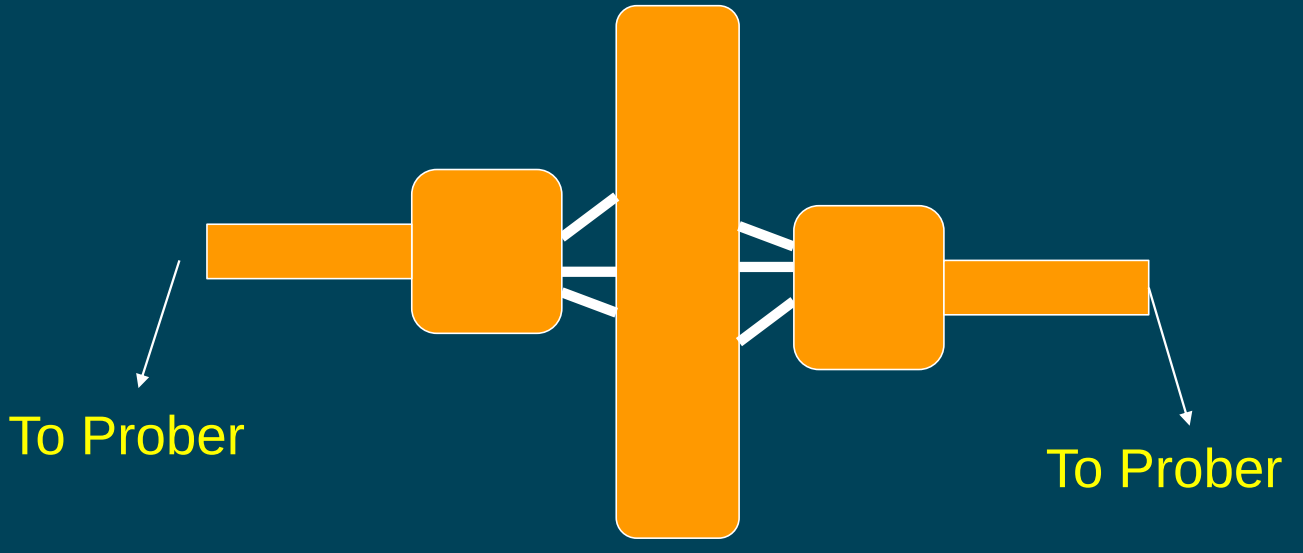


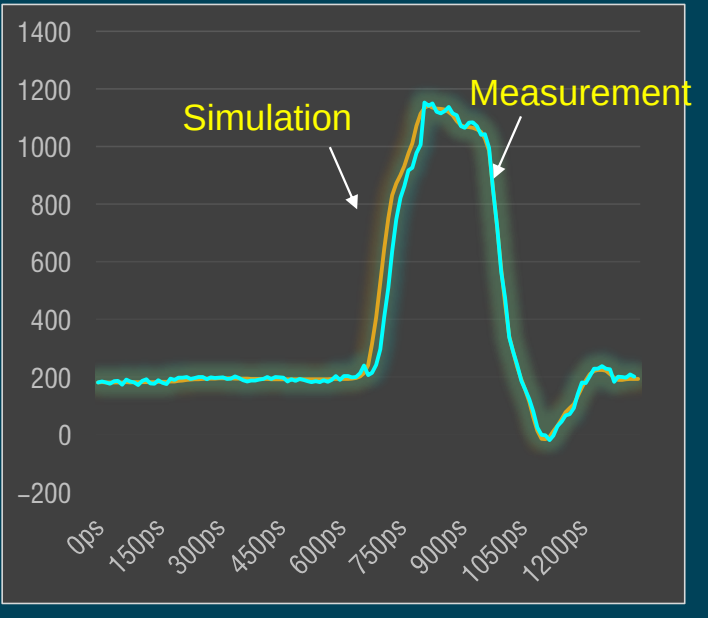
# Simulation Vs Measurement Correlation

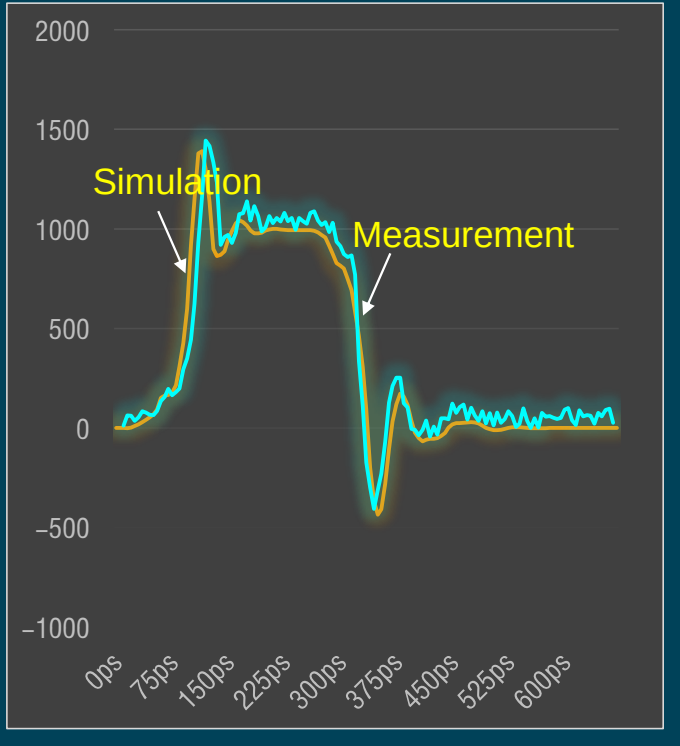



Socket Build Base on Pin Map

# Simulation Vs Measurement Correlation

Pulse Configuration A

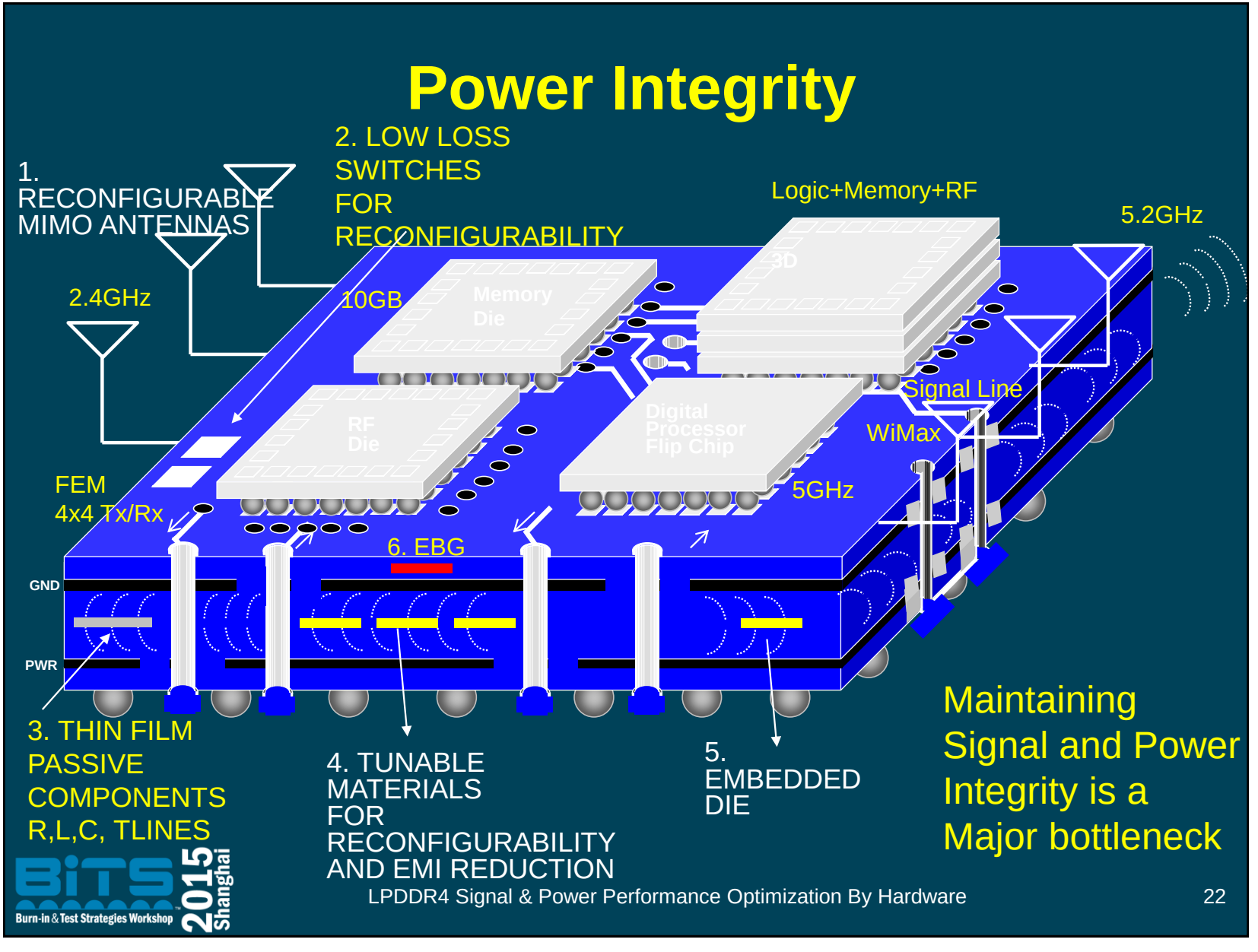



Pulse Configuration B

# LPDDR4 PI Simulations

- PI Basic
- PCB Impedance
- Socket Power Impedance Vs System Impedance
- Impedance Optimization


Power Integrity
1. RECONFIGURABLE MIMO ANTENNAS
2. LOW LOSS SWITCHES FOR RECONFIGURABILITY
2.4GHz
10GB
Memory Die
Logic+Memory+RF
3D
5.2GHz
Signal Line
WiMax
RF Die
Digital Processor Flip Chip
5GHz
FEM 4x4 Tx/Rx
6. EBG
GND
PWR
3. THIN FILM PASSIVE COMPONENTS R,L,C, TLINES
4. TUNABLE MATERIALS FOR RECONFIGURABILITY AND EMI REDUCTION
5. EMBEDDED DIE
Maintaining Signal and Power Integrity is a Major bottleneck
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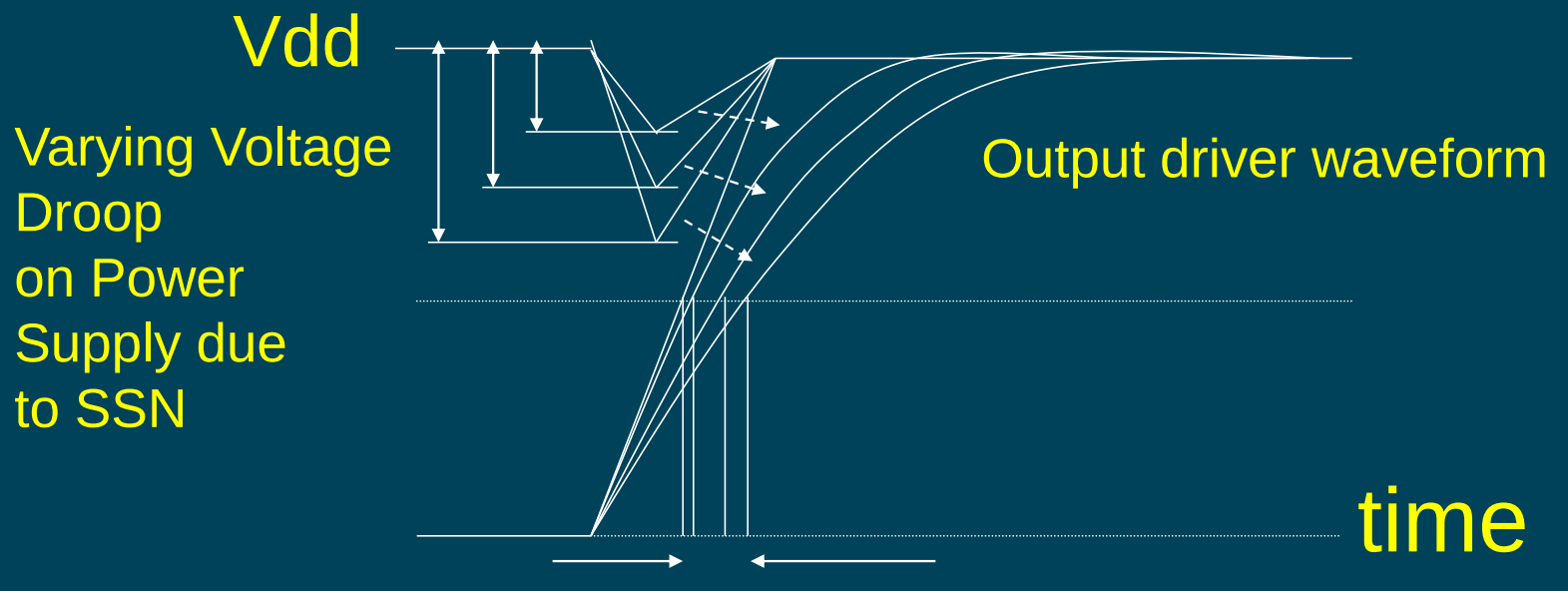
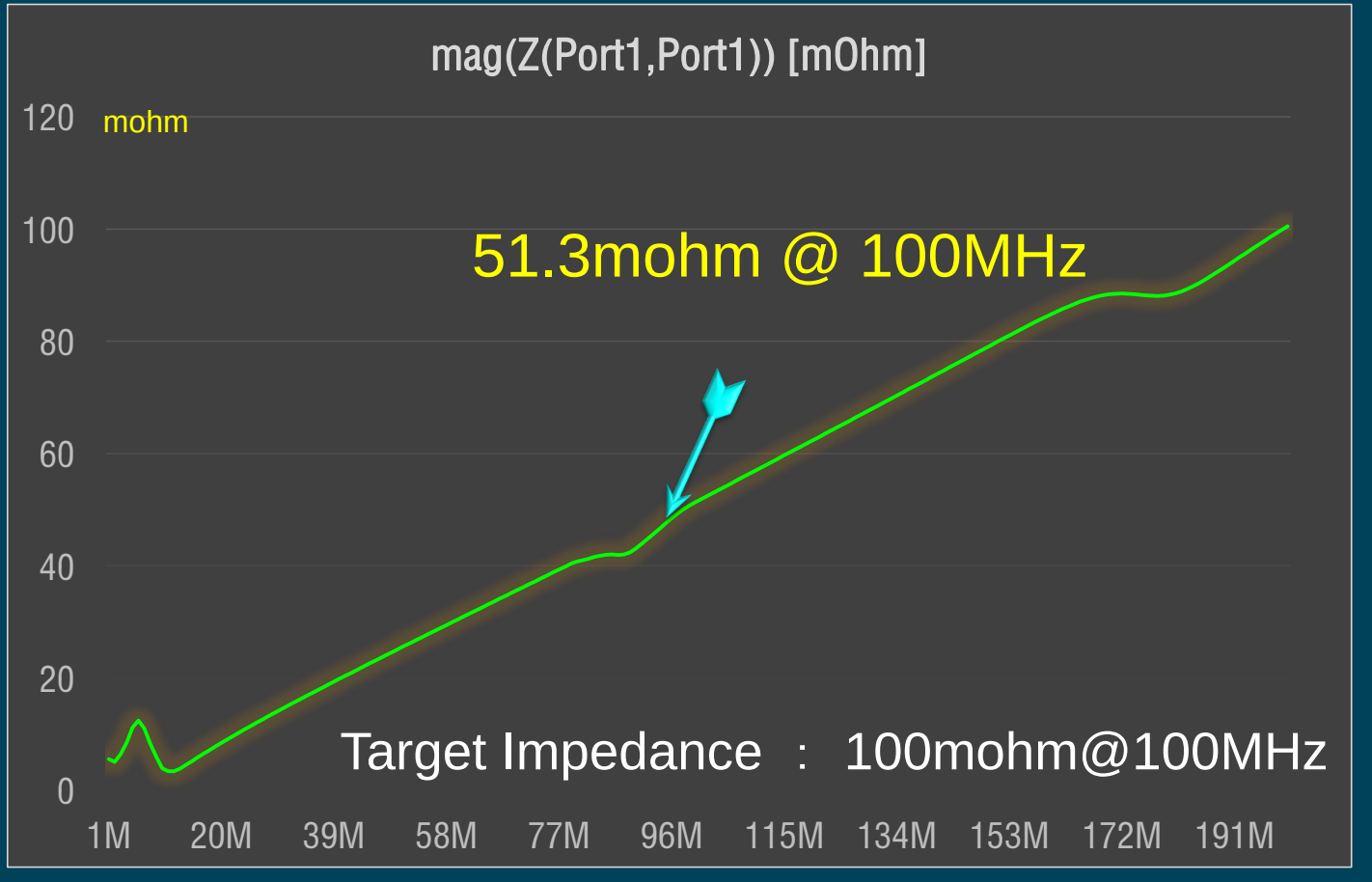
# Jitter caused by SSN for I/O



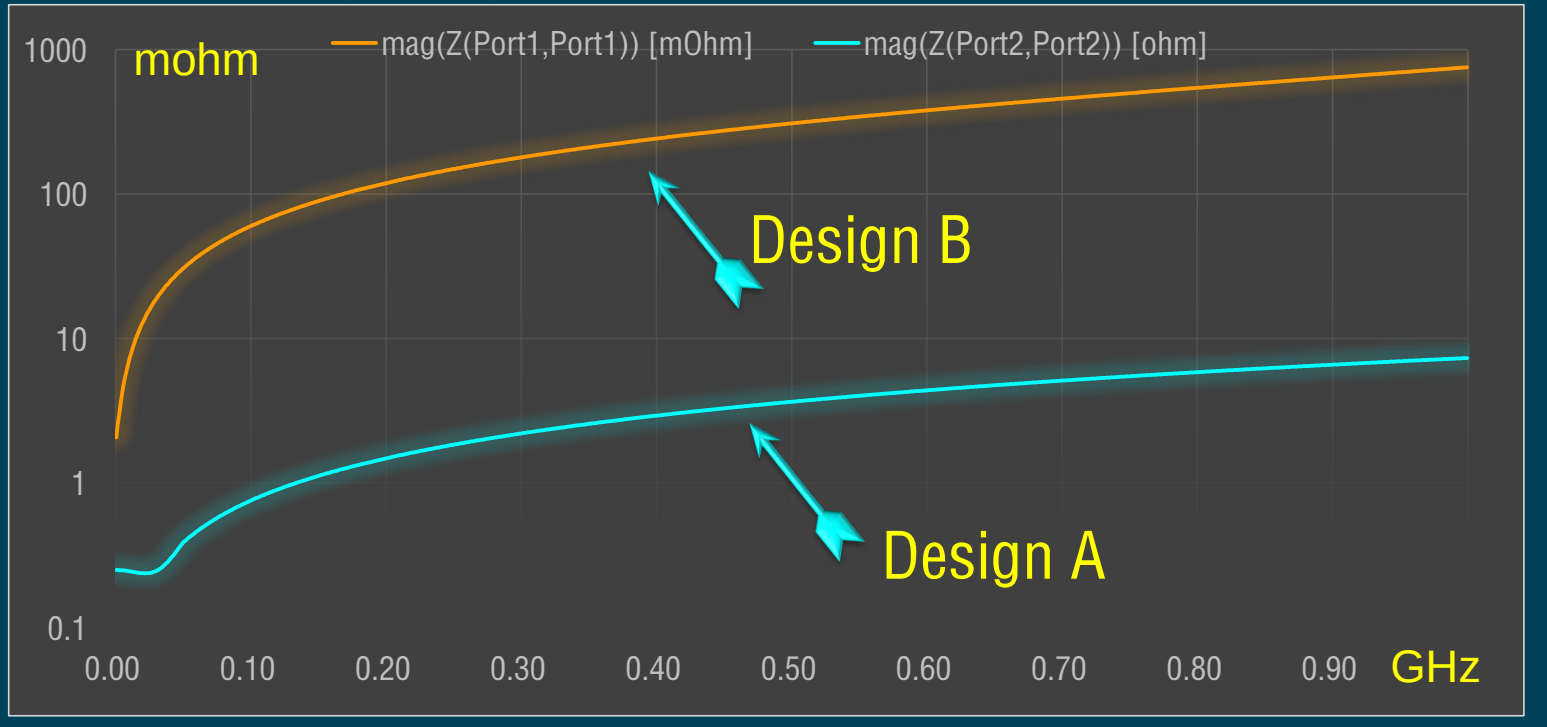

Uncertainty in Delay due to SSN causing Jitter

# PCB Power Impedance



# Socket Power Impedance

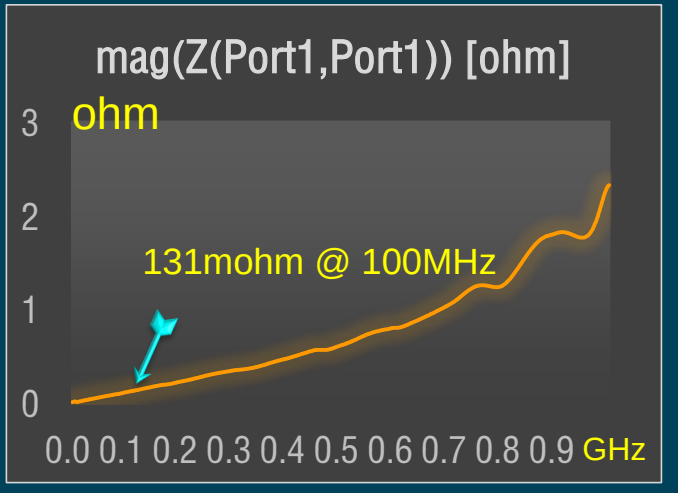
Target Impedance : 100mohm@100MHz

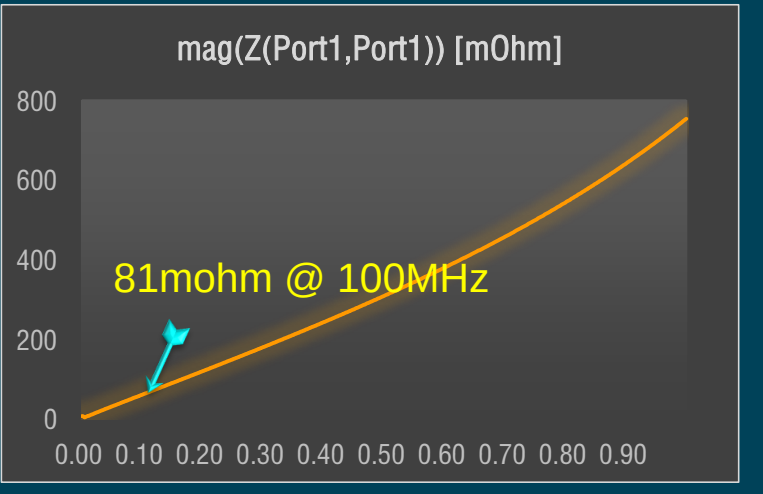



Long pin and short pin has significant difference in terms of power impedance if only measure socket only.

# PCB + Socket + Package Impedance

Target Impedance : 100mohm@100MHz



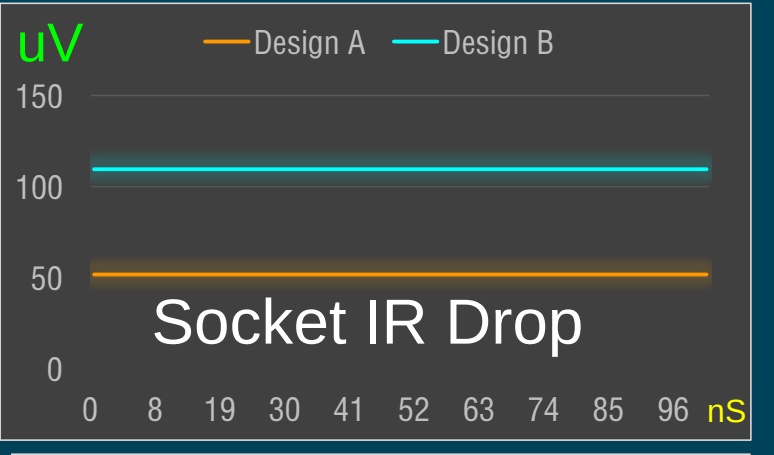

Before

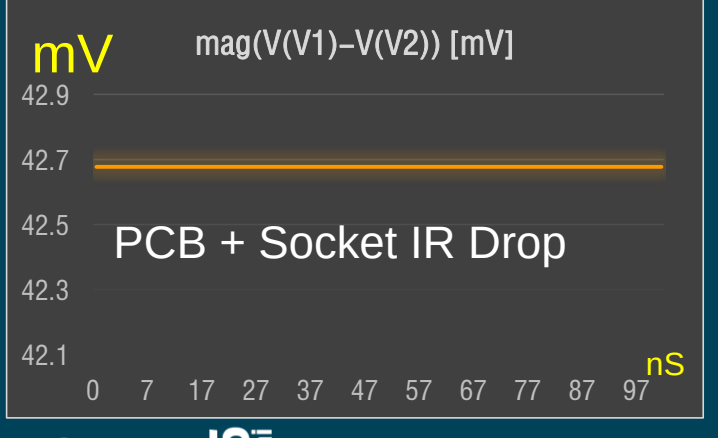
After optimized

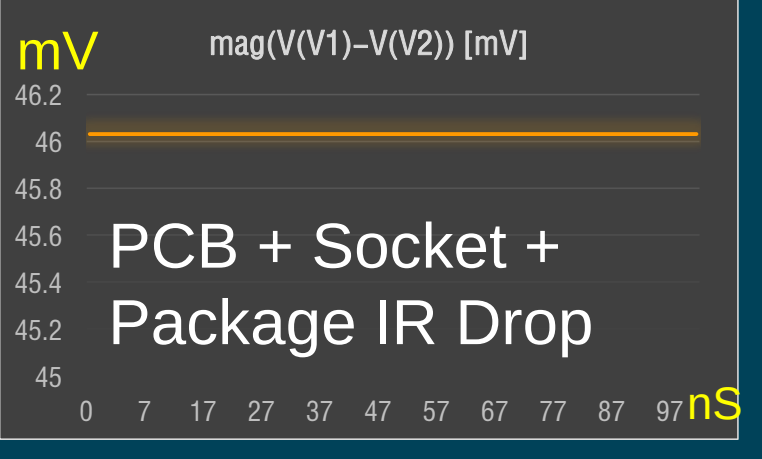
1. Increase the power pane width, and short the distribution length.
2. Optimize the pin length and diameter.
3. Although socket is not the main factor for the power impedance, however an optimized socket design and contactor selection also help the power impedance certain.

# IR Drop

Target Drop : <50mV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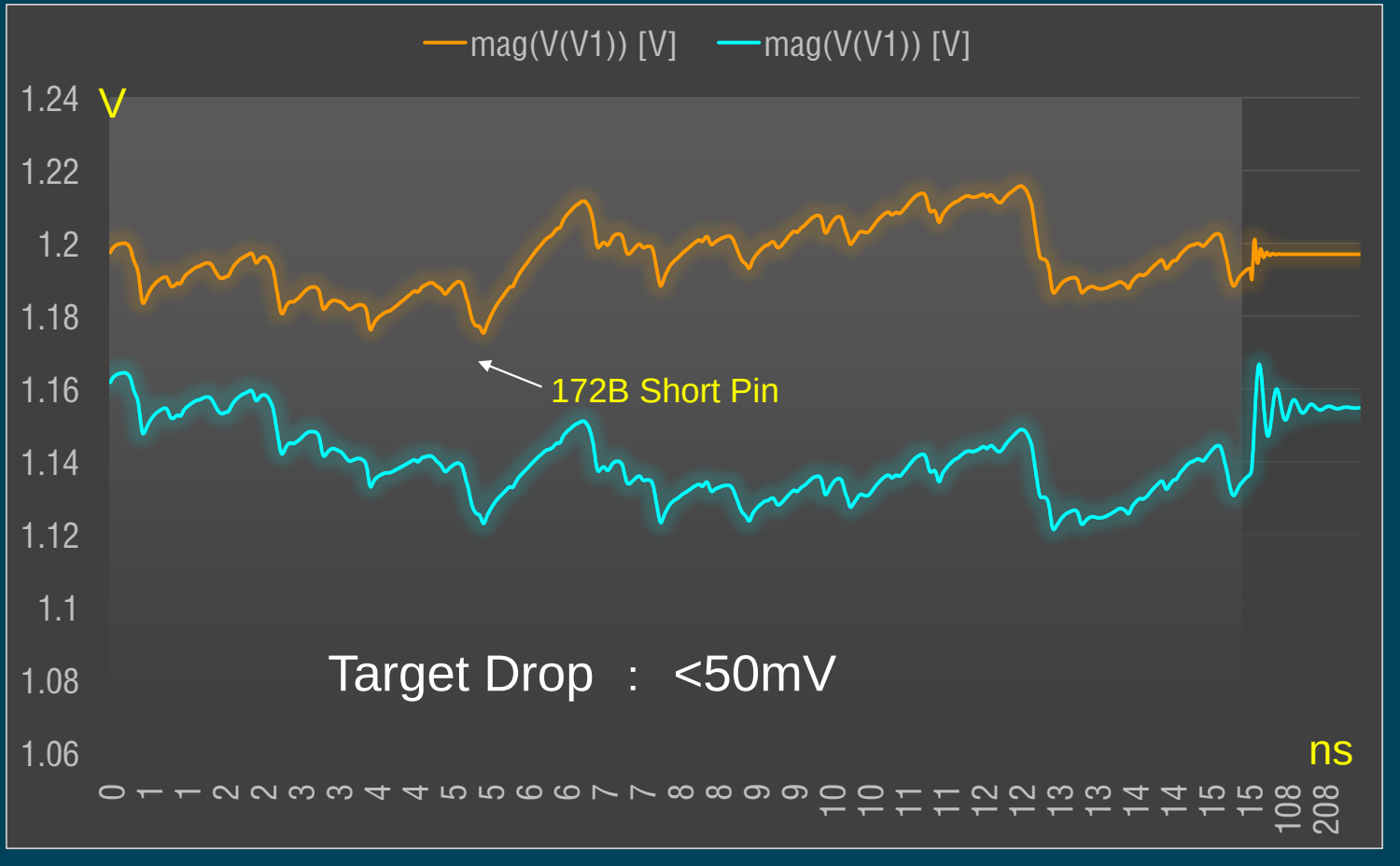
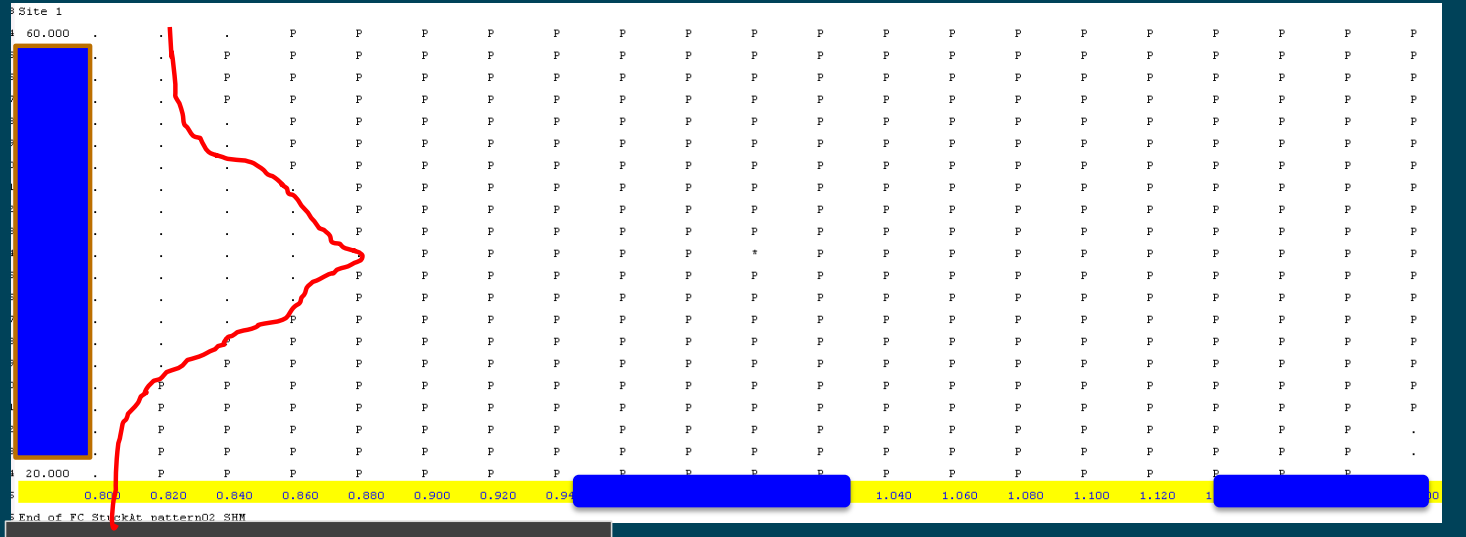
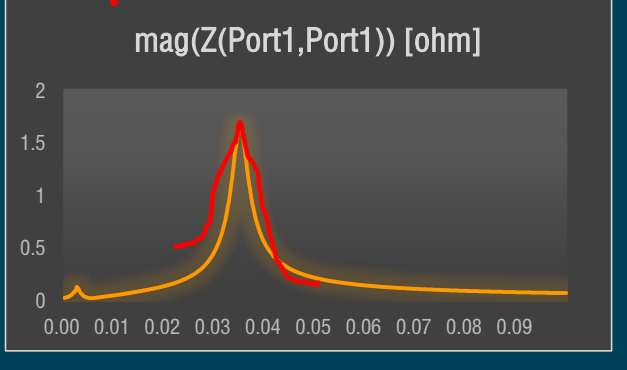
# Power Transient



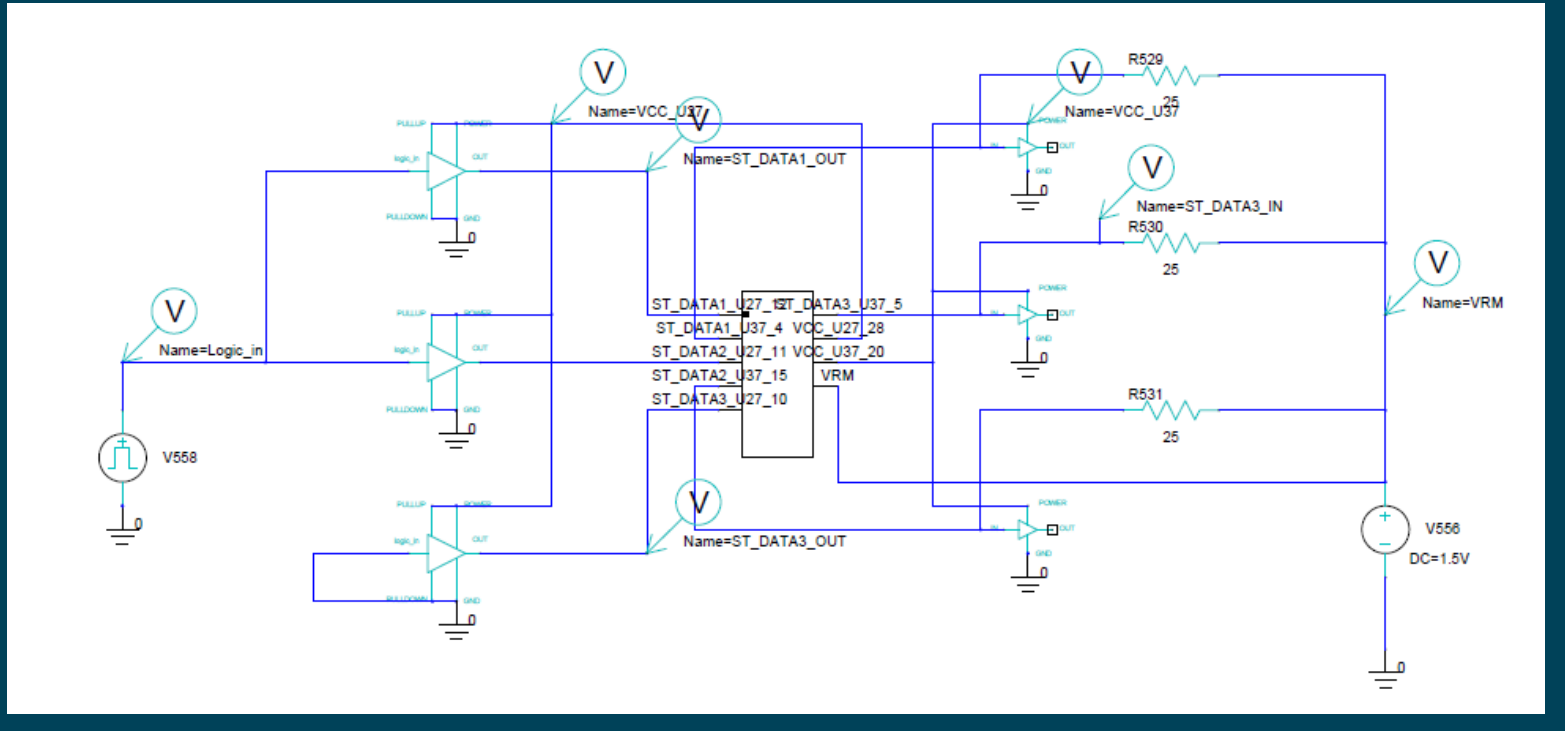
# Power Impedance Vs Shmoo Measurement




1. SHMOO shows the controller fail curve is quite close to the power impedance simulation data.
2. The resonance frequency for simulation and measurement is also close.

# Future Work


Name=VCC_U37
Name=ST_DATA1_OUT
Name=Logic_in
V558
Name=ST_DATA3_OUT
ST_DATA1_U27_1
ST_DATA1_U37_4
ST_DATA2_U27_11
ST_DATA2_U37_15
ST_DATA3_U27_10
ST_DATA3_U37_5
VCC_U27_28
VCC_U37_20
VRM
R529
25
Name=VCC_U37
Name=ST_DATA3_IN
R530
25
Name=VRM
R531
25
V556
DC=1.5V

# Summary

- Discussion one method to study whether the hardware can meet the LPDDR4 specification.
- Discussion one method to identify the main factor for the whole SI chain.
- Optimize the socket and pin layout to meet the power impedance performance.
- Utilize Shmoo to correlate the power impedance data.