
SEVENTEENTH ANNUAL
BiTS
TM
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 3
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BiTS Burn-in & Test Strategies Workshop 2016

Session 3

Morten Jensen

Session Chair

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 4:30 pm

Stimulating Simulating

"Optimizing the PCB-to-socket-to-DUT interface"

Gert Hohenwarter - GateWave Northern, Inc.

"Characterize Only the High Speed Interconnect Performance"

Carol McCuen - R&D Altanova

"Modelling, Materials, and Madness"

Mike Gedeon - Materion

Characterize Only the High Speed Interconnect Performance

Carol McCuen
R&D Altanova

2016 BiTS Workshop
March 6 - 9, 2016

Goal

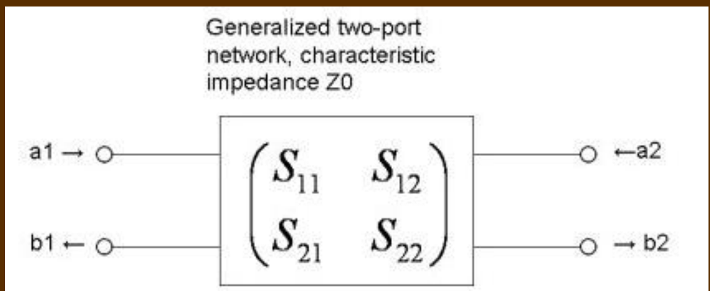
- To provide Signal Integrity Engineering with an accurate model of their particular High Speed Interconnect in the form of an S-parameter data file.
  - Where does the Interconnect begin and end?
  - Do we include the traces, vias, ground plane, PCB substrate in the model?
  - Can we use the measurement data to create Time Domain information, i.e. step impedance or eye diagrams?
  - What Signaling (Single-ended or Differential) and Pin configurations are needed?

Plan of Attack to Reach Goal

- Make Laboratory Measurements on PNA
  - What measurements do we want and how to set measurement parameters for success?
  - Frequency vs. Time Domain
- Create an accurate 3D model, using the measured data, and then use to predict new variations of Interconnect patterns of Signal pins, Aggressor pins and Grounding pins.

What are S-parameters? Network Analyzer measurements

- The Black Box --"Linear Networks can be completely characterized at the network terminals without regard to the contents of the networks…" Richard Anderson, author of the well know Agilent Application Note 95-1
- S-parameters are better than Z (impedance) or Y (admittance) parameters because of the problem of creating a good Open and Short at high frequencies.
- S-parameters are intrinsically a frequency domain measurement.



$$S_{11} = b1/a1$$
$$S_{12} = b1/a2$$
$$S_{21} = b2/a1$$
$$S_{22} = b2/a2$$

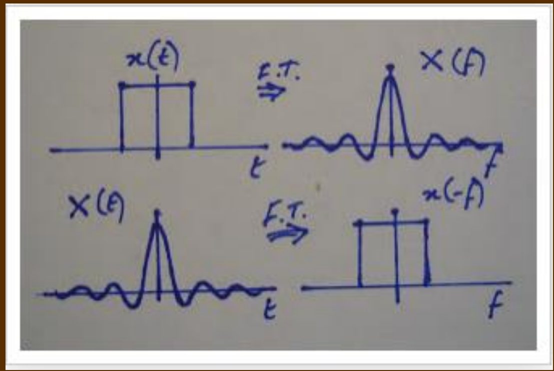
Basic Time Domain Considerations

- In the perfect world, we can use the Fourier Transform pair to convert from the frequency domain to the time domain, or visa versa.
- Our S-parameter are Band-Limited and only at Discrete Frequencies, use a DFT,
  - ±∞ Frequency is impossible which creates ringing and spreading (sinx/x) in the time domain response. See the Inverse Fourier Transform (IFT) of the rectangular function.
  - A Windowing function can be used to control side-lobes in the IFT by gradually reducing frequency data at the band edge, instead of abrupt edge. There are usually 3 choices for windowing – Min., Normal, Max.

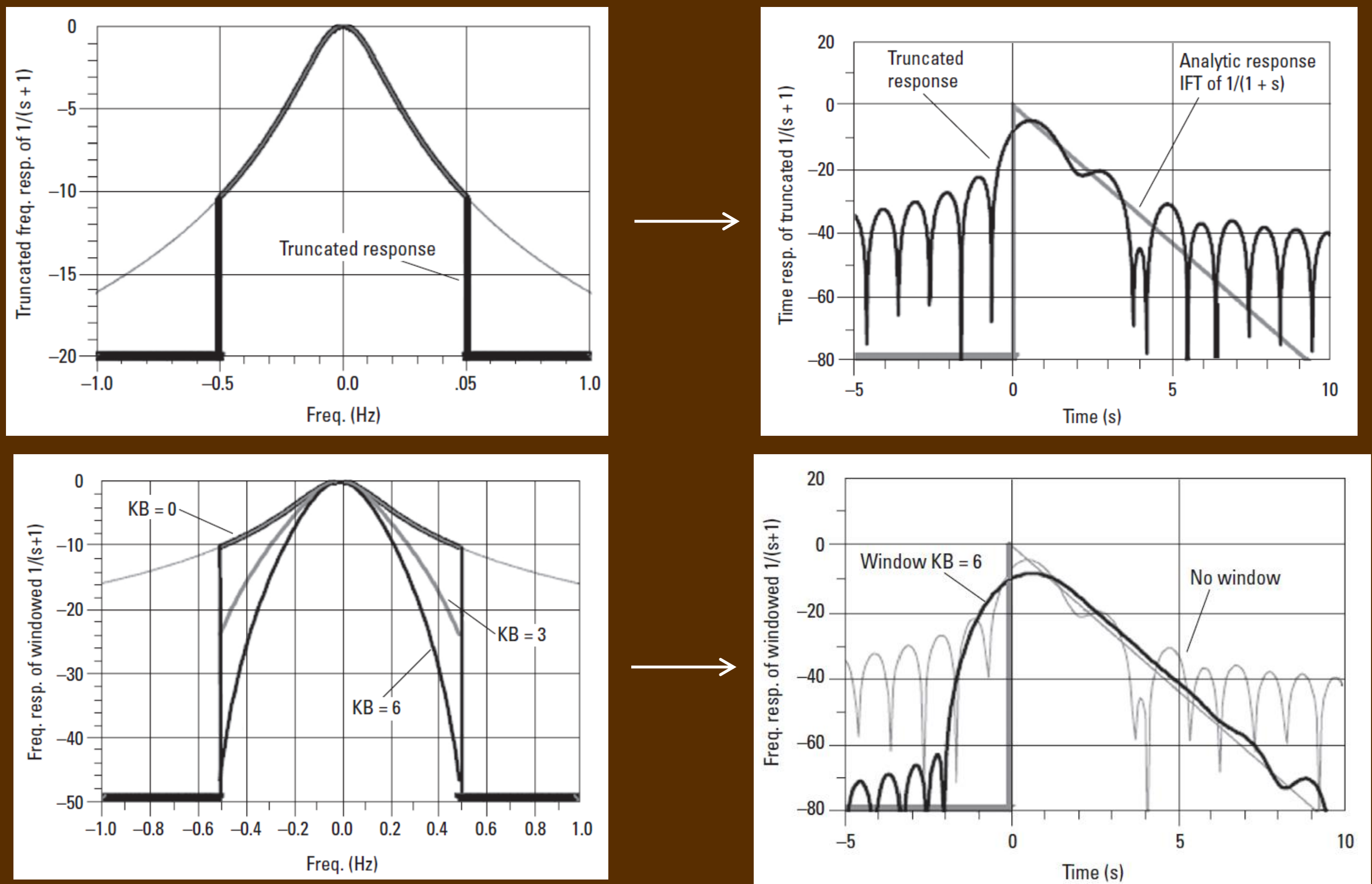
Continuous Function

$$X(\omega) = \int_{-\infty}^{\infty} e^{-j\omega t}\, x(t)dt$$

$$x(t) = \frac{1}{2\pi}\int_{-\infty}^{\infty} e^{j\omega t}\, X(\omega)d\omega$$



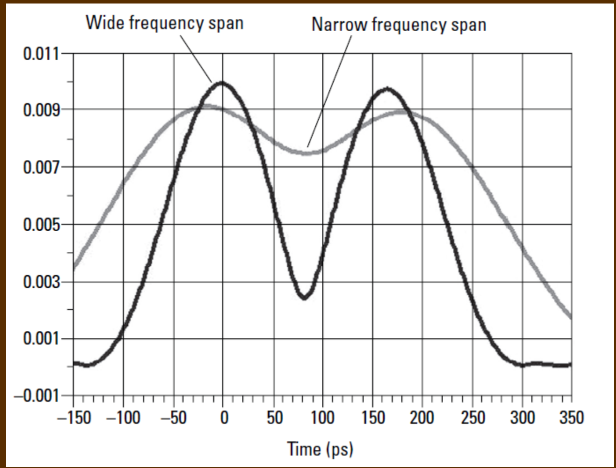
Example of Windowing



From Agilent (Keysight) Application Note 1287-12 *

Time Domain Considerations (cont.)

- Our S-parameters are Band-Limited and only at Discrete Frequencies
  - Response Resolution is the measure of how close two responses can be to each other and still be distinguished.
  - Response Resolution and Step Rise Time (RT) is also affected by Windowing. The more the control on the window roll-off the longer the RT and Response Resolution time.



Response Resolution

$$\frac{1}{2\times F_{max}},\ where\ F_{max} = 50\ GHz$$

$$= 10\ picoseconds$$

From Agilent (Keysight) Application Note 1287-12 *

Time Domain Considerations (cont.)

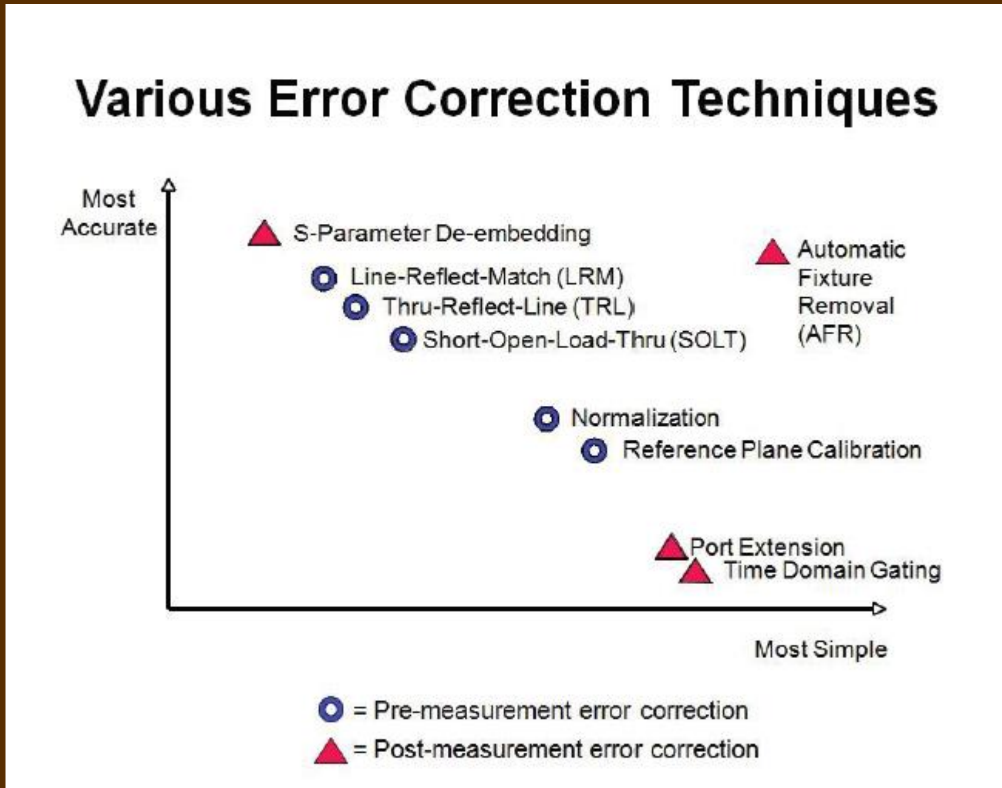
- Our S-parameter are Band-Limited and only at Discrete Frequencies
  - The sample frequencies must be equally spaced all the way down to DC, Zero Hertz + Frequency step.
  - Because the S-parameters are discrete frequencies, time domain is a Repeated pulse train - response will repeat at the inverse of the Frequency step, 10 MHz Vary step size to assure length of time for signal to travel across DUT.

$$5000\ Frequency\ samples$$
$$10MHz\ to\ 50\ GHz$$

$$Period = \frac{1}{10\ MHz} = 100\ ns$$

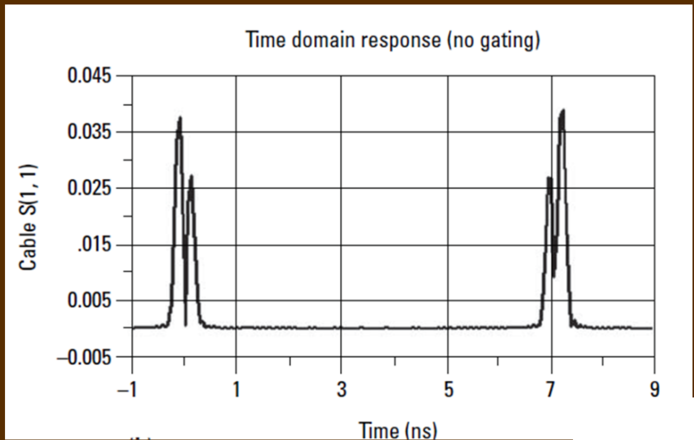
$$Total\ length\ of\ time\ IDTFT = 5000 \times 10ps = 50ns$$

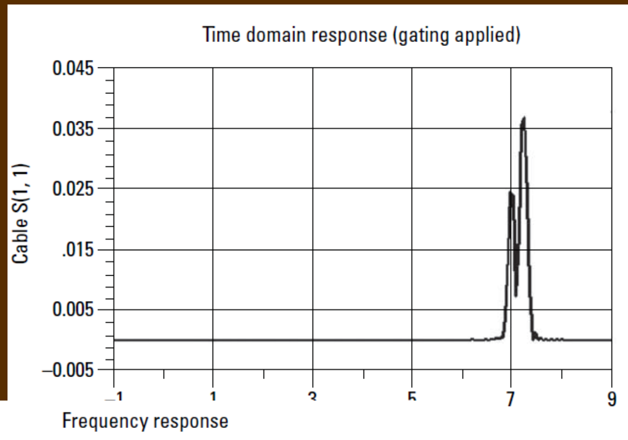
Accuracy in Characterizing Interconnect



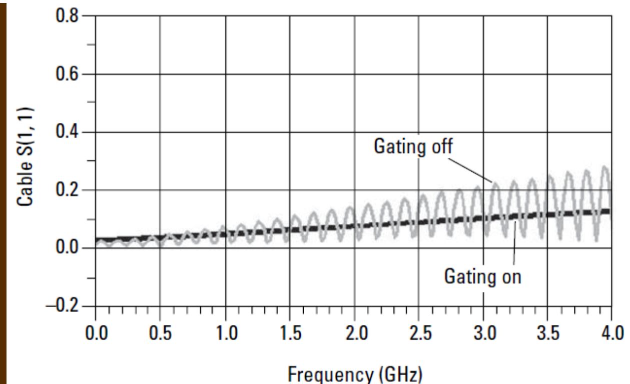
Methods to remove the Effects of the Test Fixture

- Time Domain Gating – least accurate





User defines 2 points in time which are then mathematically replaced with an ideal transmission line.

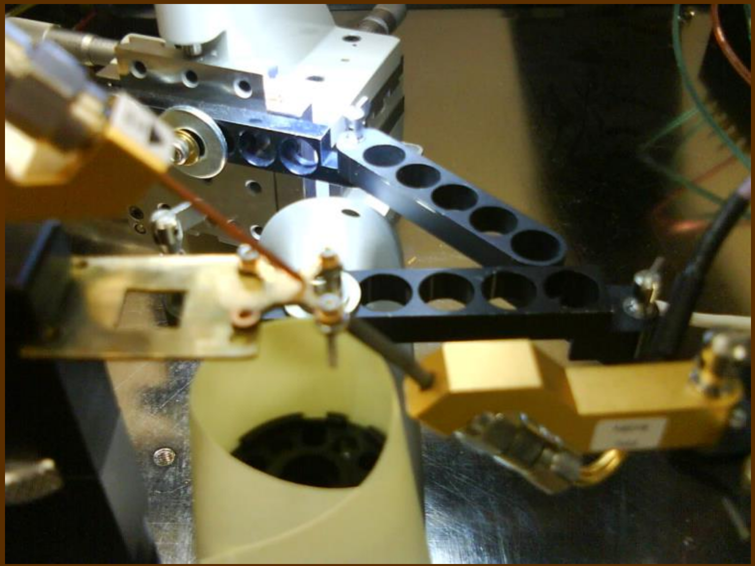


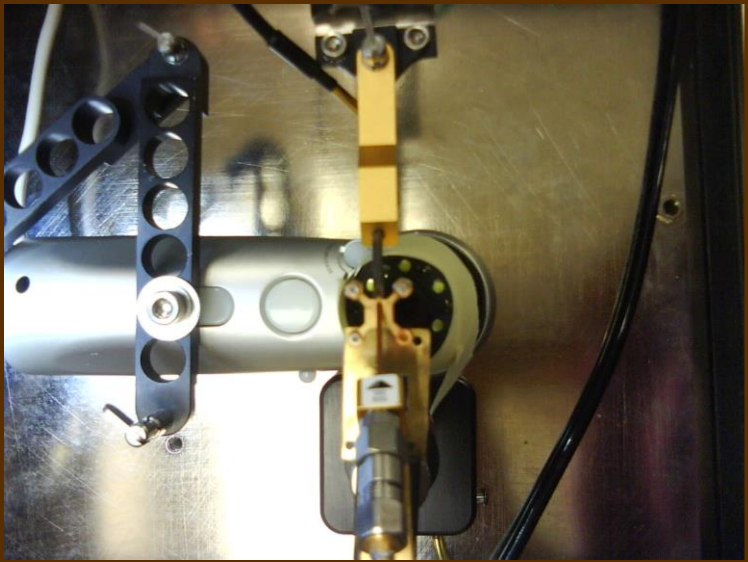
Port Extension or Phase Rotation

- Performs removal of a length (Phase) of perfect ideal transmission line.
- Some VNA's will add an Insertion Loss compensation for flat attenuation across the band of measurement.
- This can lead to inaccurate results because the reflected wave due to the Real Fixture's mismatch combines with the incident waves and create peaks and nulls in the response.
- These disturbances to the response will not be removed when using a simple port extension.

Direct measurement vs. De-embedding

- If we did a probe-tip calibration, a Direct measurement, De-embedding would be unnecessary.

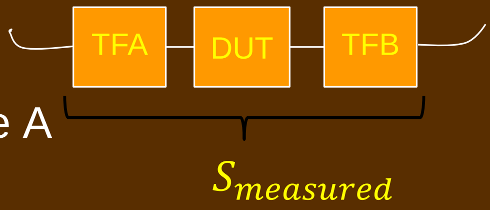




Direct measurement vs. De-embedding

- The probes alone will not be able to compress the contacts. Post-Measurement processing-De-embedding will be needed.

- **De-embedding procedure**



  1. Get 2-port S-parameters of Test Fixture A (TFA) and Test Fixture B (TFB).
  2. Measure DUT with TFA and TFB - called $S_{measured}$
  3. Convert to T-parameters -> $[T_{DUT}] = [T_A]^{-1}[T_{measure}][T_B]^{-1}$
  4. Convert T_{DUT} back to S-parameters, S_{DUT}.

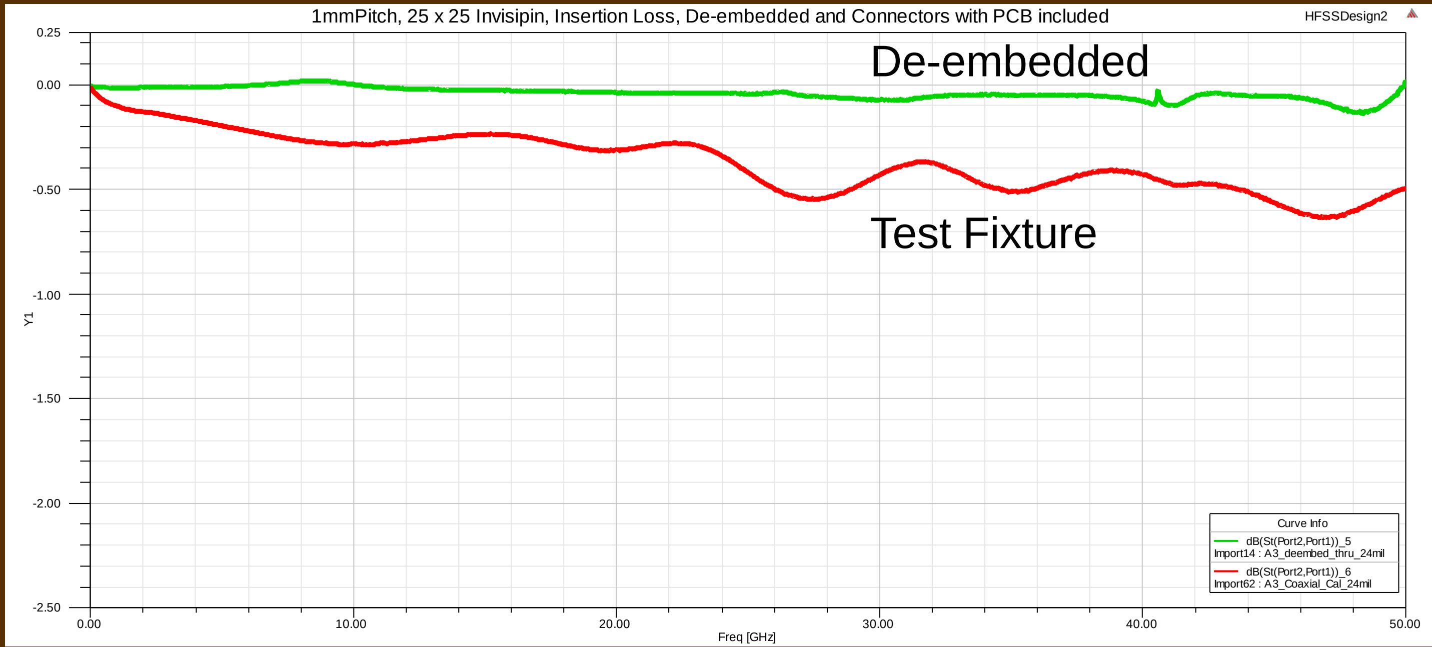
- The difficult part is getting the 2-port S-parameters for the Test fixtures A and B.
- Choose-> Coaxial Cal & Use Keysight's PNA ***Physical Layer Test System (PLTS) 2015, Automatic Fixture Removal.***

Automatic Fixture Removal (AFR)

- What is in the test Fixture that needs De-embedding?
  - A very flat device with very small separate conductors to contact all the pins evenly. – a PCB will work well along with a stiffening fixture.
    - Two - 30 mil Taconics TLY-5 with 2 mil thick copper Top and Bottom layers
    - Two Connectors – 2.4 mm 50 Ohm Vertical PCB Compression Jack

1. Assemble the test Fixture without the Interconnect pins soldered. Make Thru measurement.
2. The AFR will determine the Test fixture A and B 2-port S-parameters.
3. The PNA will do the matrix math to De-embed TFA and TFB, resulting in the DUT S-parameters..

Results Insertion Loss:
Test Fixture (Red) vs. De-embedded (Green)
1mm pitch, 25 x 25 pin, 24 mil hardstop thickness



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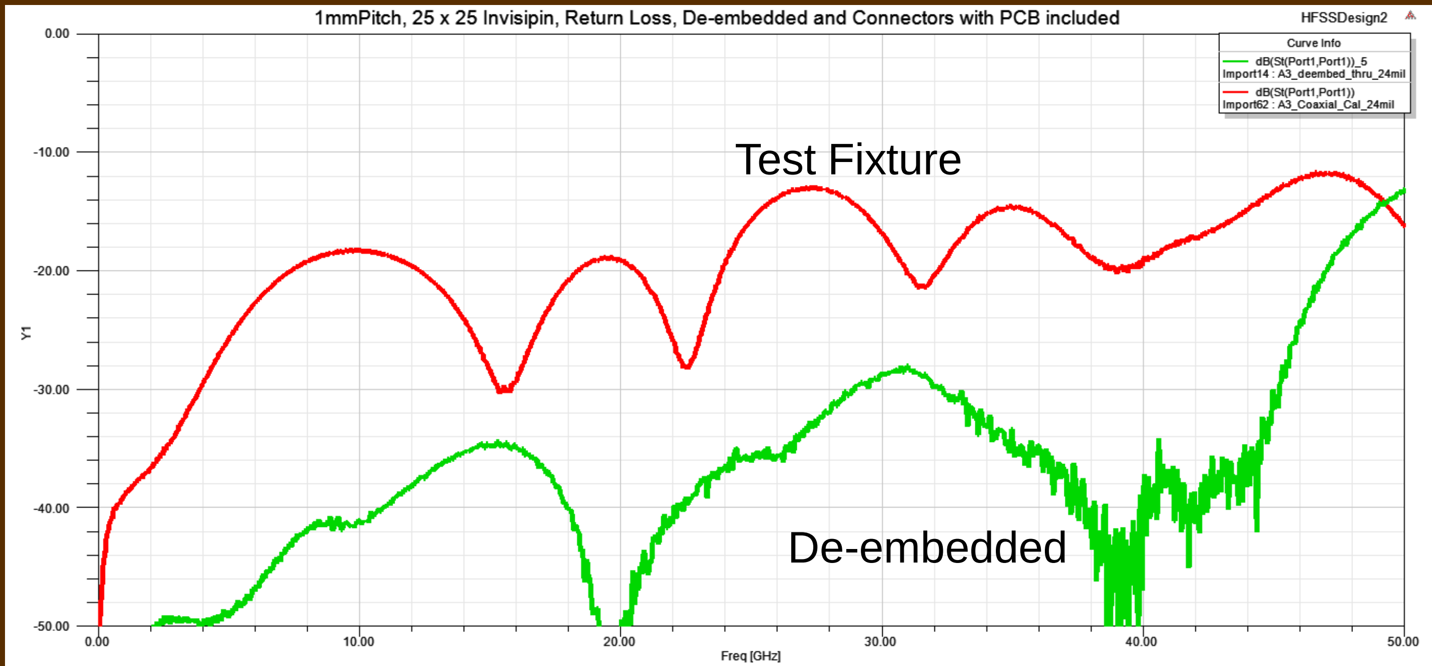
Results Insertion Loss:
Test Fixture (Red) vs. De-embedded (Green) 1mm pitch, 25 x 25 pin, 24 mil hardstop thickness

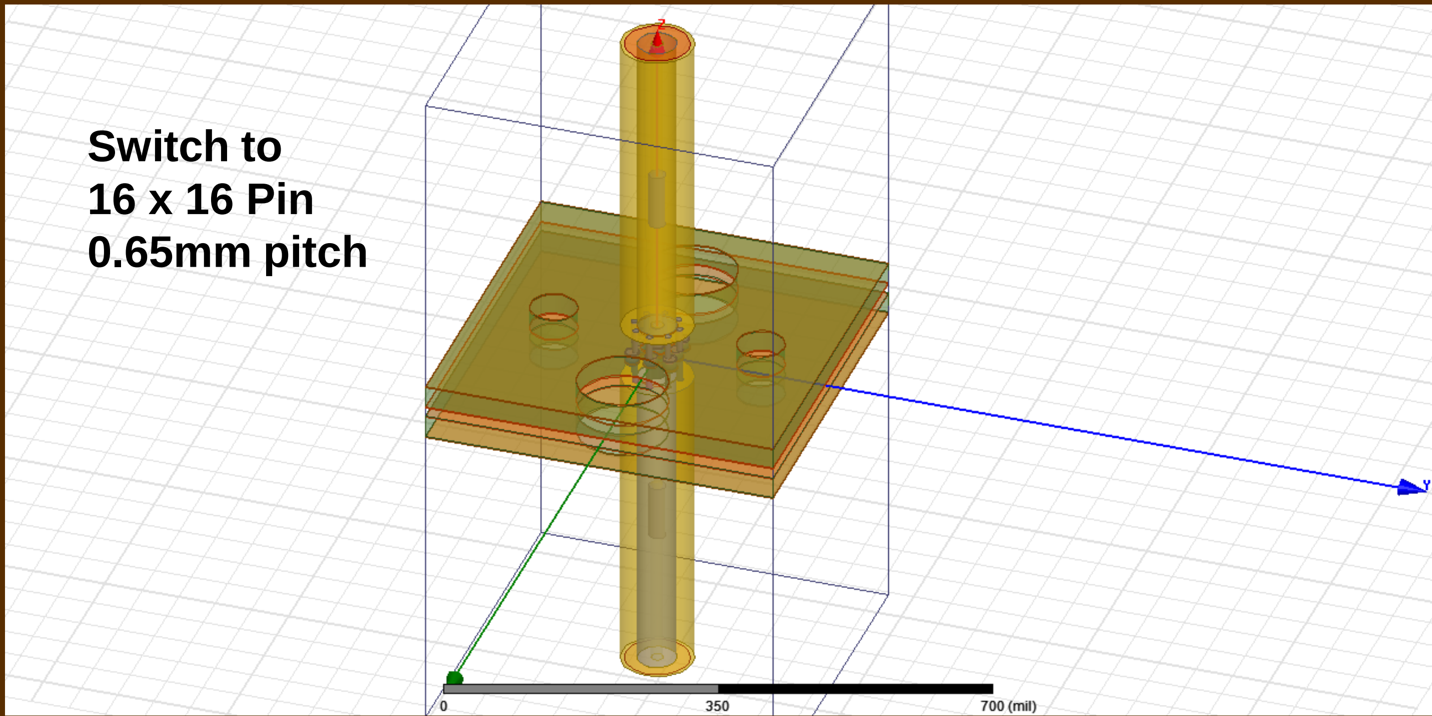


Determine the 3D model

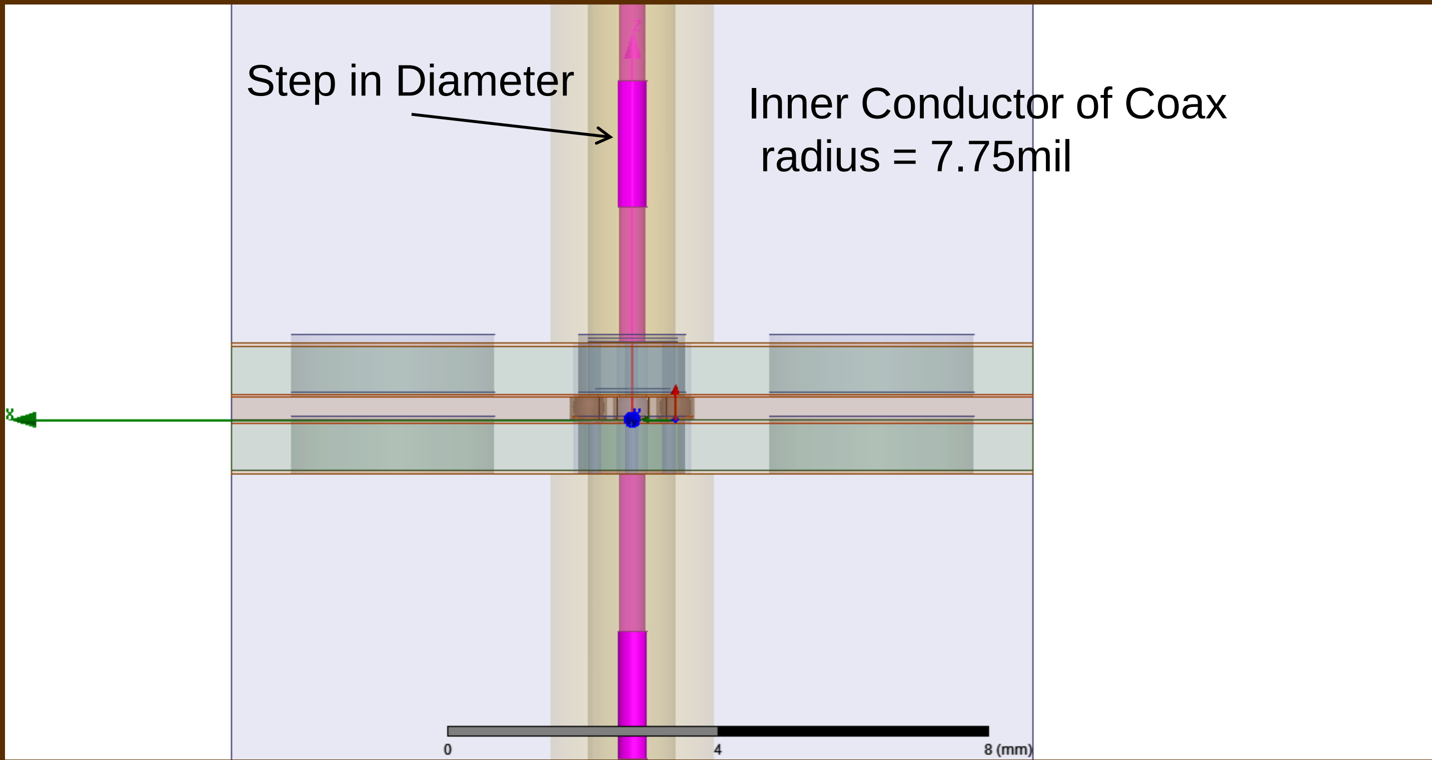
- In order to have confidence in the High Speed Interconnect 3D model it is best to take more than one approach when comparing with measured data.
- Build 2 HFSS Models and compare with two different measurements:
  1. Use measured data that contains the test fixture with the contacts that we want to model.
  2. Use the VNA De-embedded measurement data (Contacts Only)

Complete Measurement- Connectors, two PCB's with Invisipin soldered to one PCB with Hardstop between.

Switch to 16 x 16 Pin 0.65mm pitch

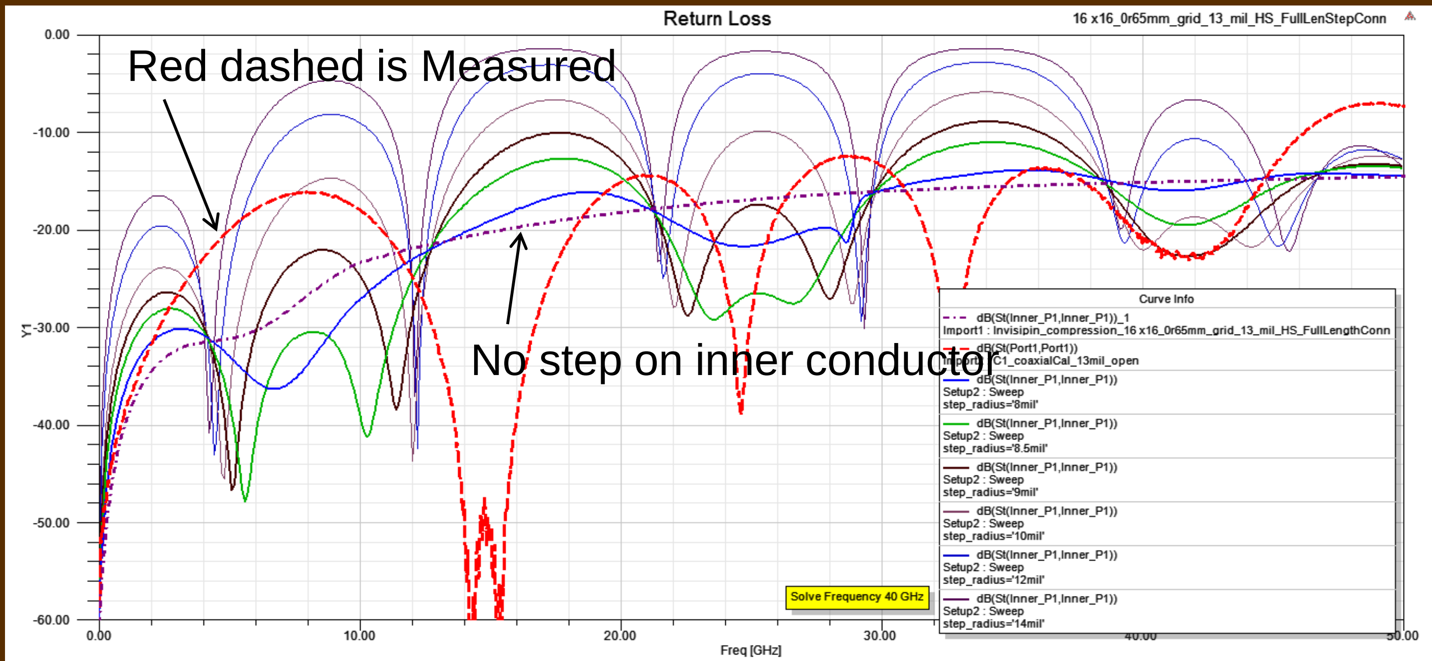


Step in inner conductor of the coax representing the connector construction



Return Loss - Vary radius of the step on inner conductor, from 8mil to 14mil

Inner Conductor of Coax, radius = 7.75mil



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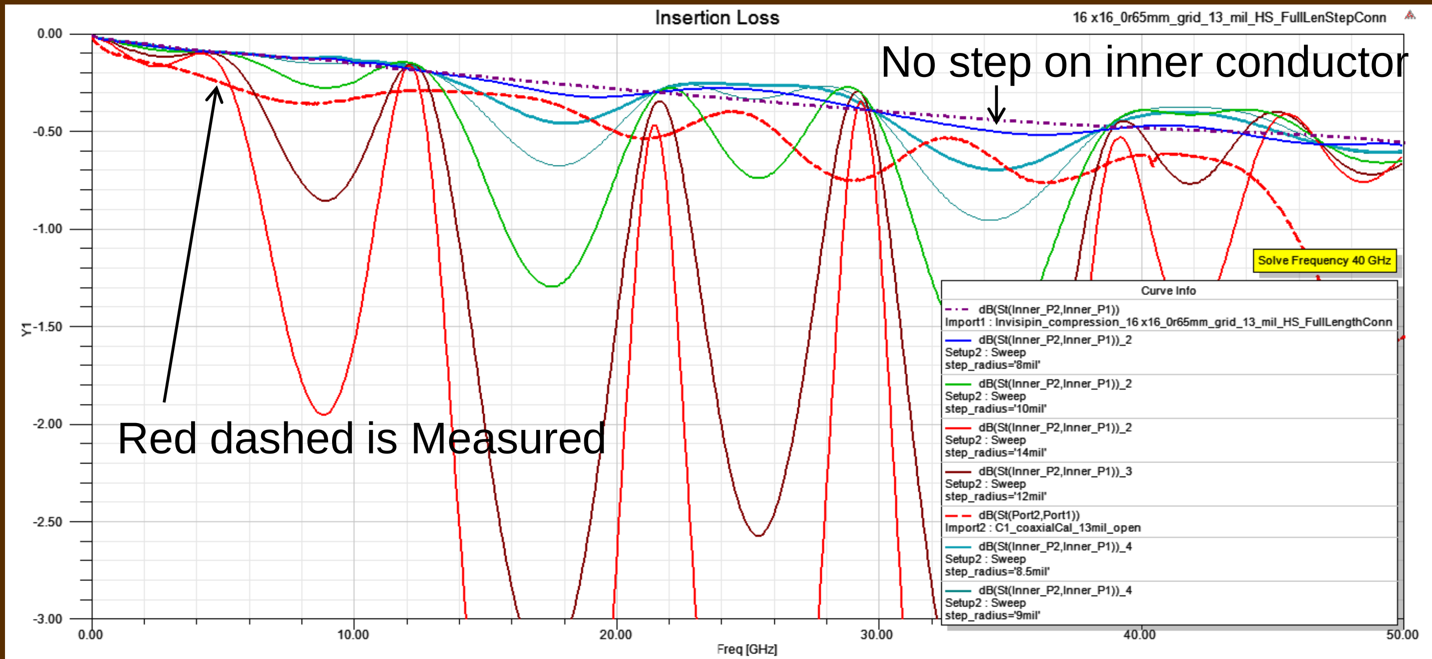
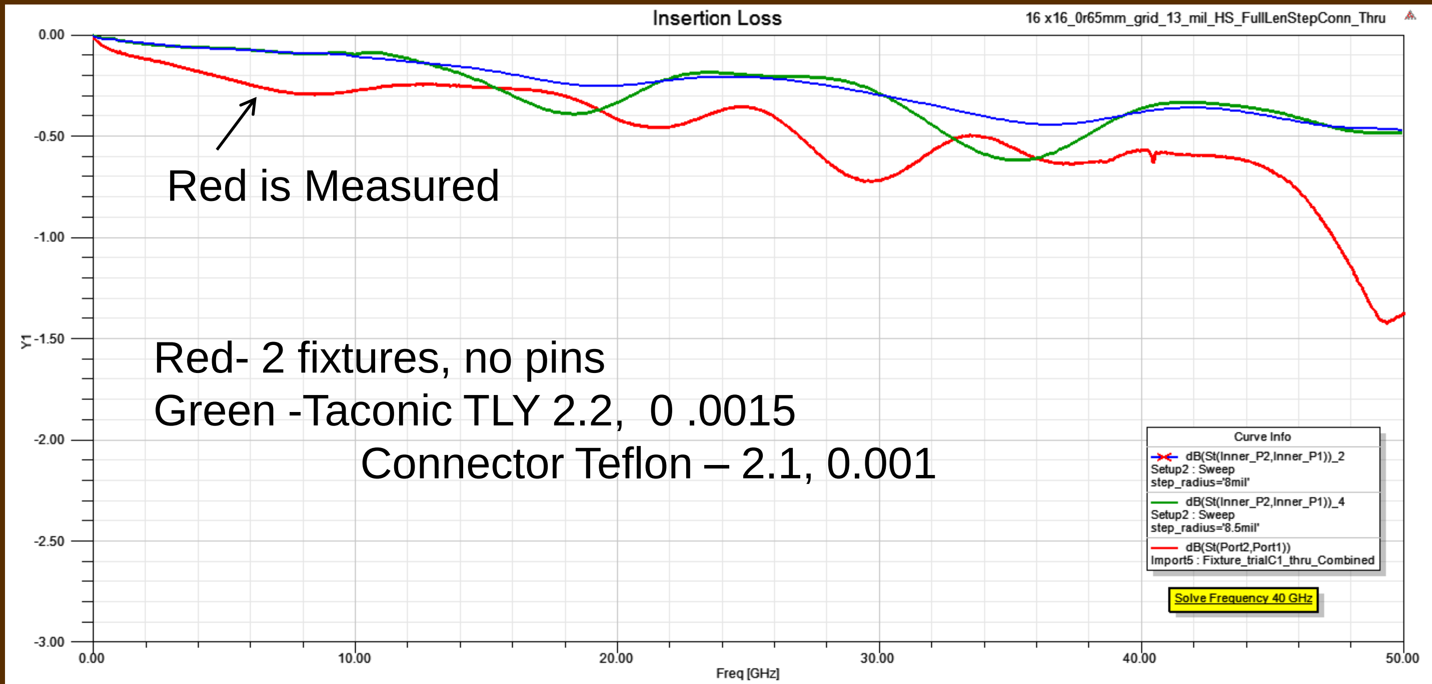
Insertion Loss - Vary radius of the step on inner conductor, from 8mil to 14mil

Inner Conductor of Coax, radius = 7.75mil



No Invisipin mounted, 0.65mm Two fixtures back to back Thru

Tweak the electrical properties of the connector insulator



No Invisipin mounted, 0.65mm Two fixtures back to back Thru

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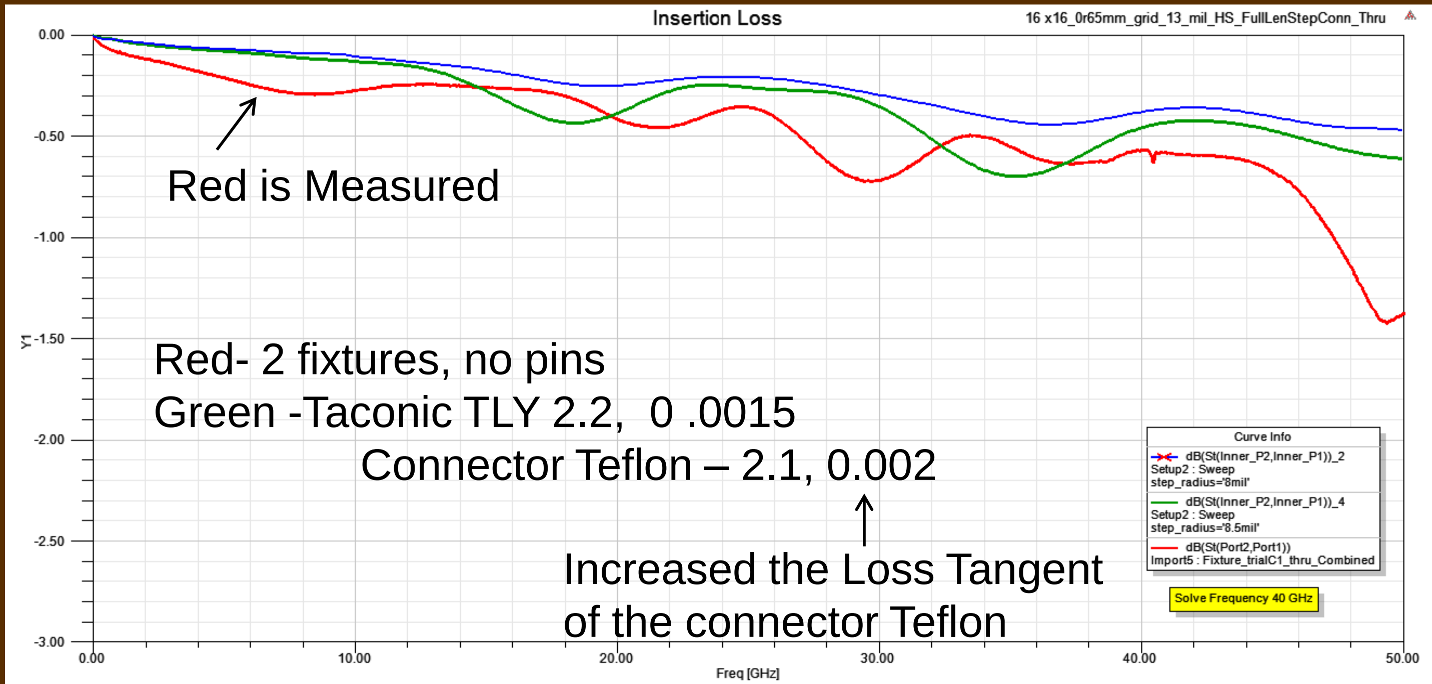
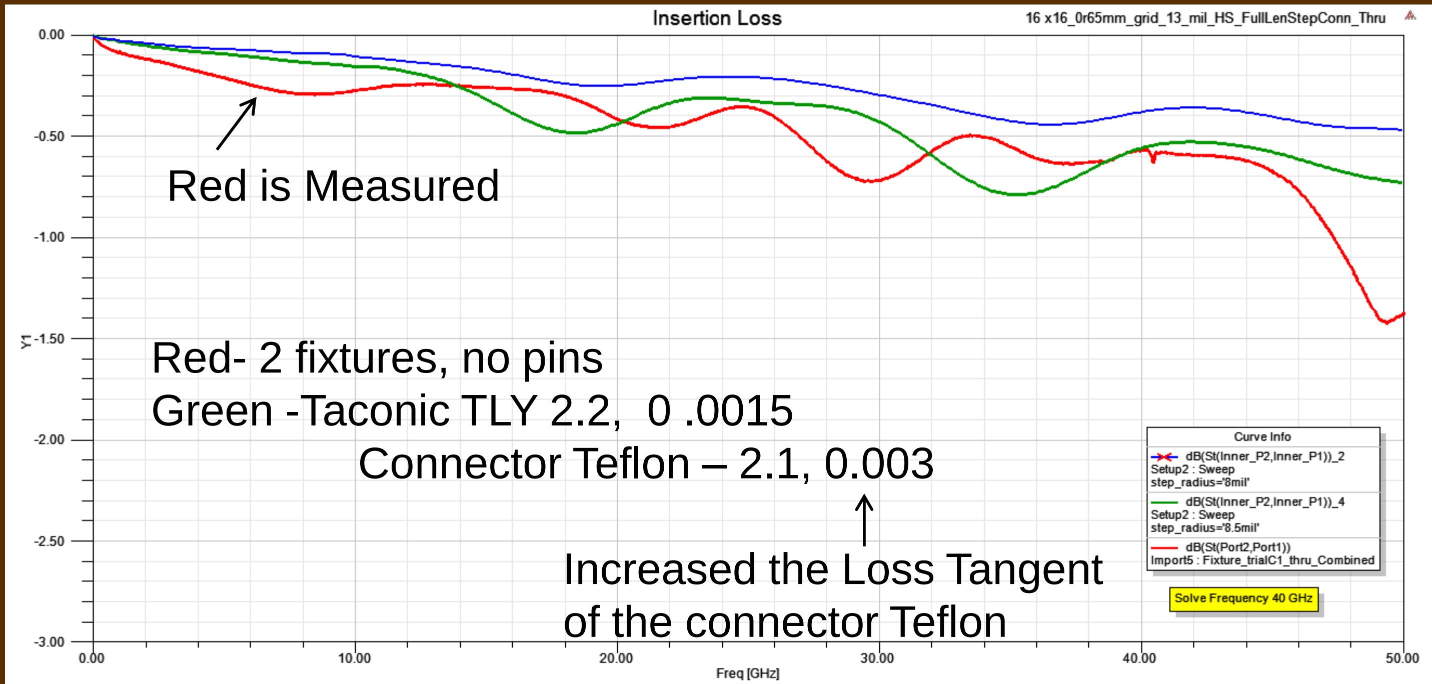
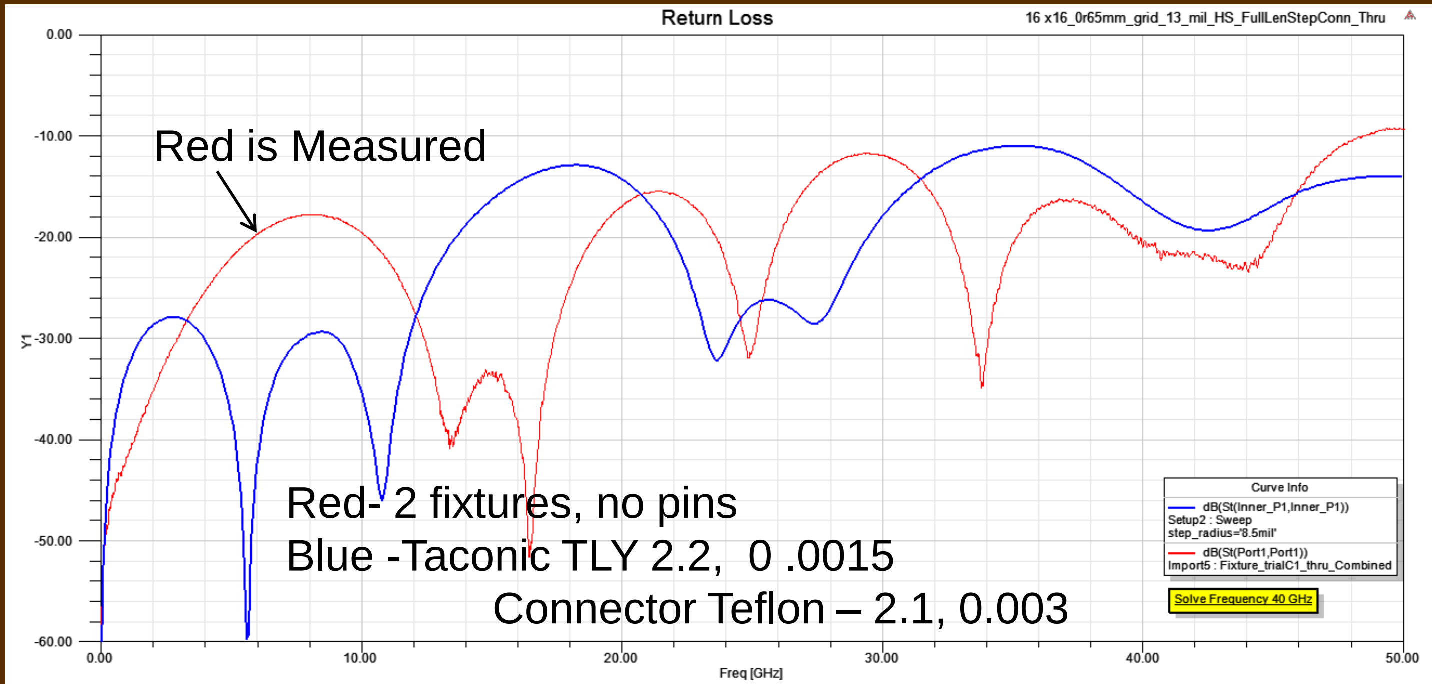


Change Loss Tangent of the Teflon in Connector

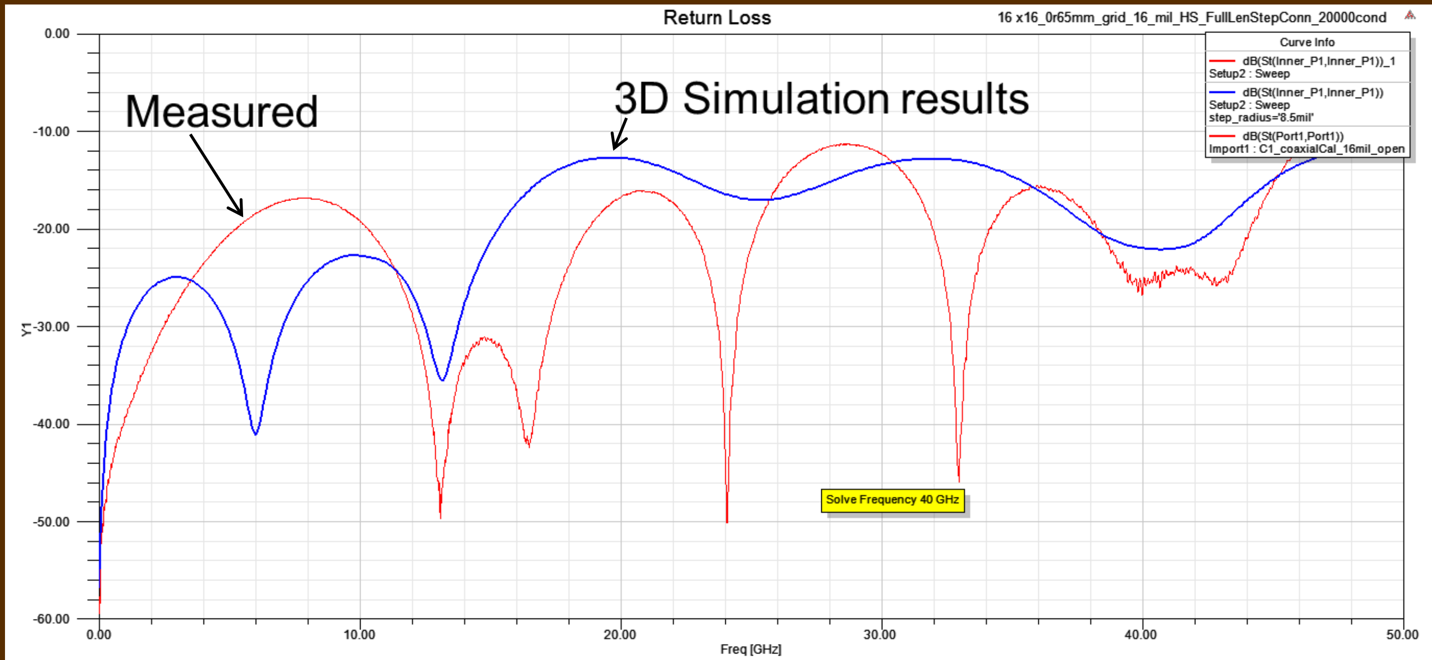


No Invisipin mounted, 0.65mm Two fixtures back to back Thru
Final electrical property values



Measured vs. Final 3D model of Complete Test Fixture with Pins

16 x 16, 0.65mm pitch - 16 mil Hardstop height



Characterize Only the High Speed Interconnect Performance

Measured vs. Final 3D model of <u>Complete</u> Test Fixture with Pins

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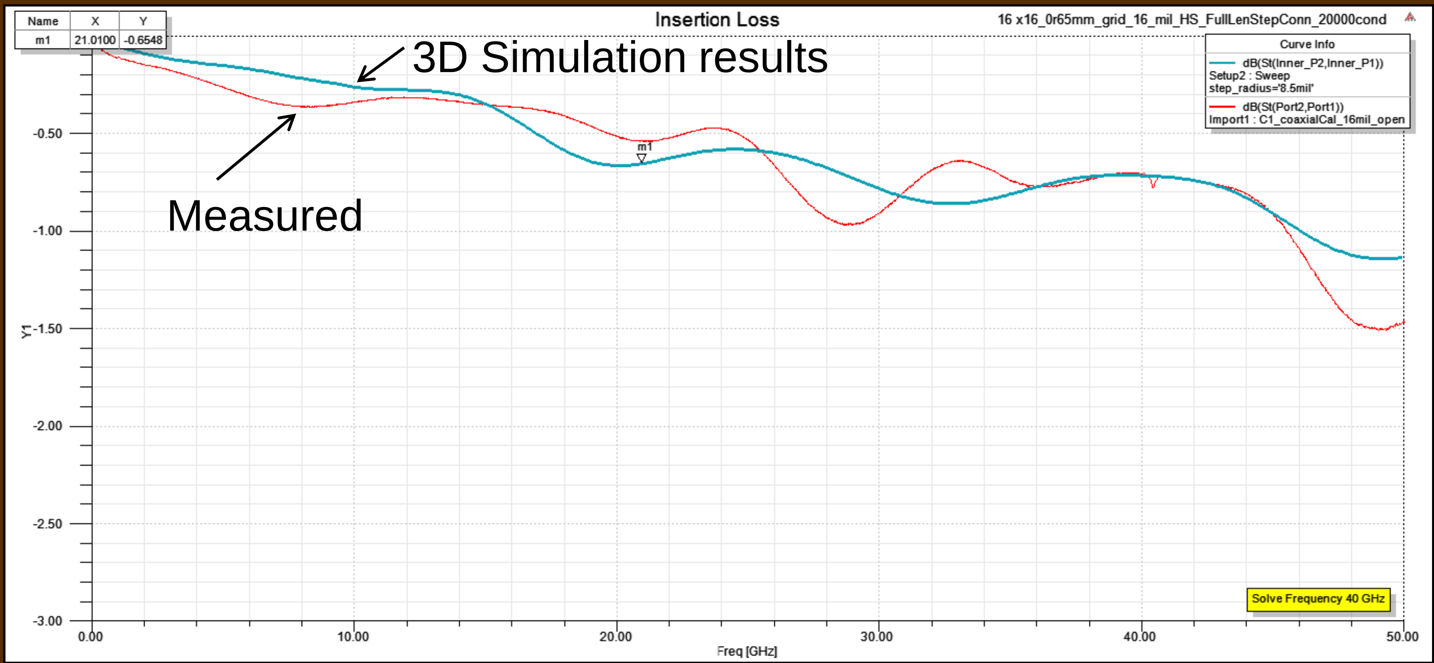
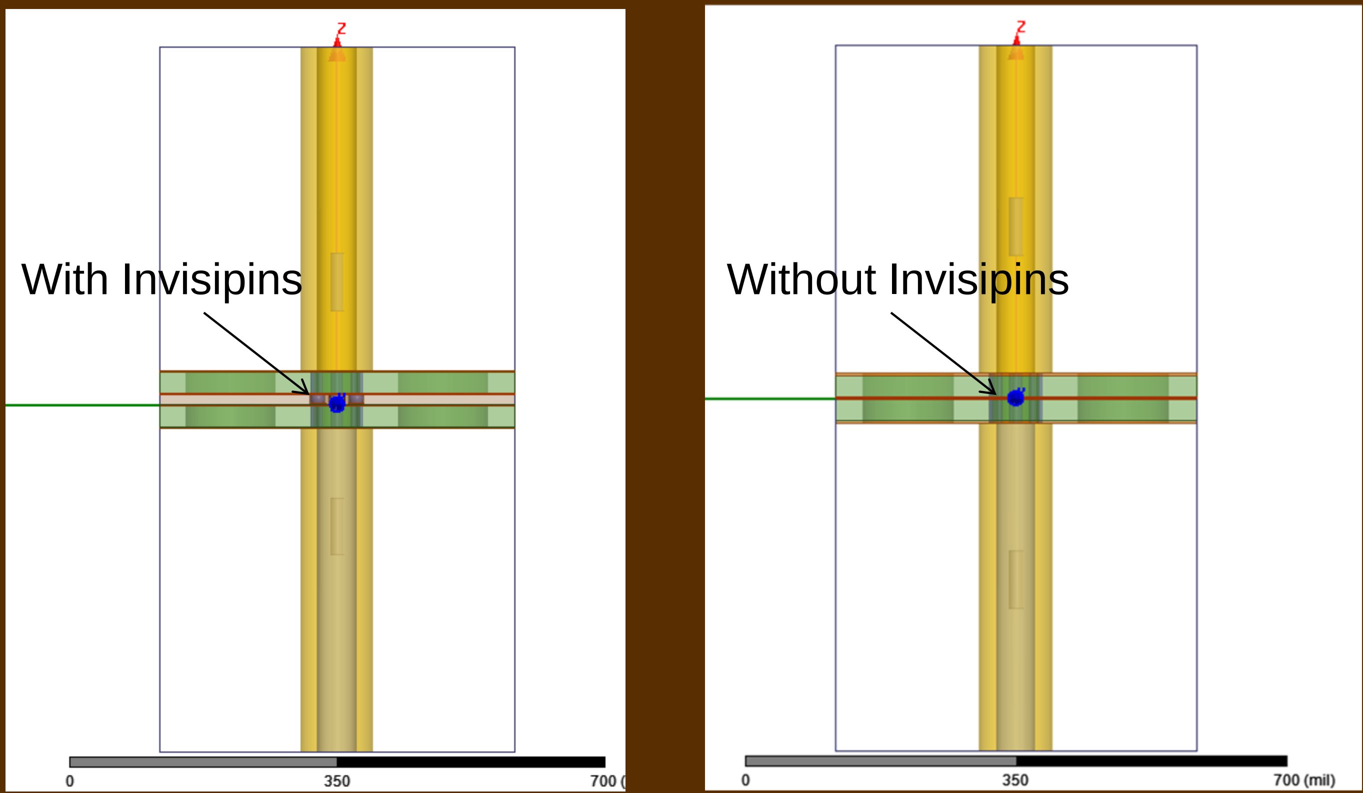
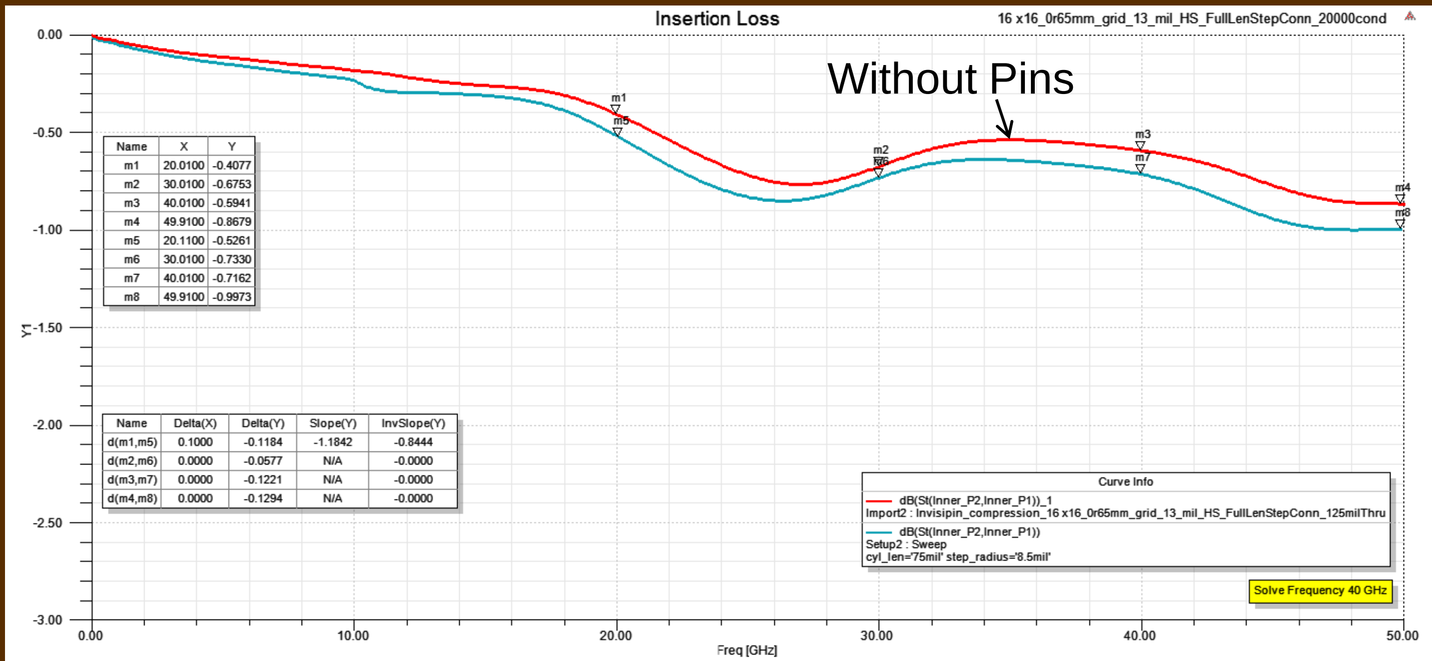


3D Model with and Without Pins



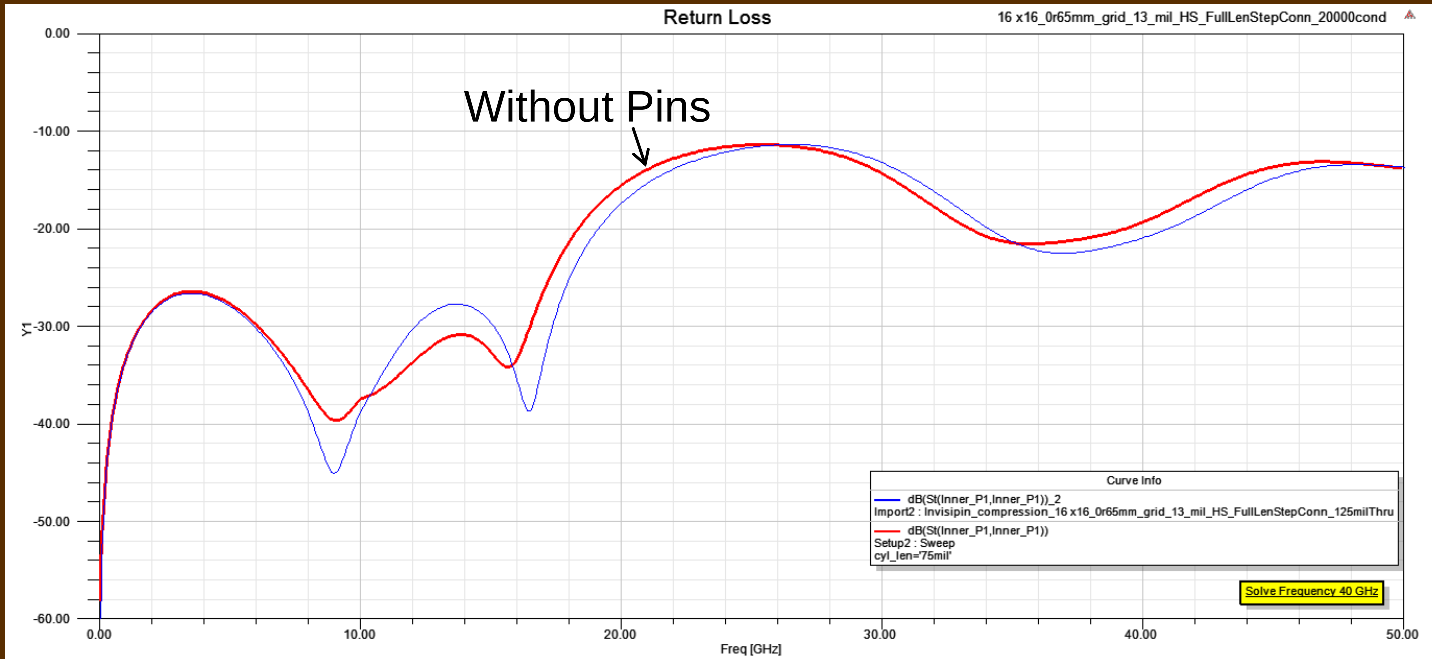
Characterize Only the High Speed Interconnect Performance

Comparing the two 3D Models- with the Pins / without the Pins

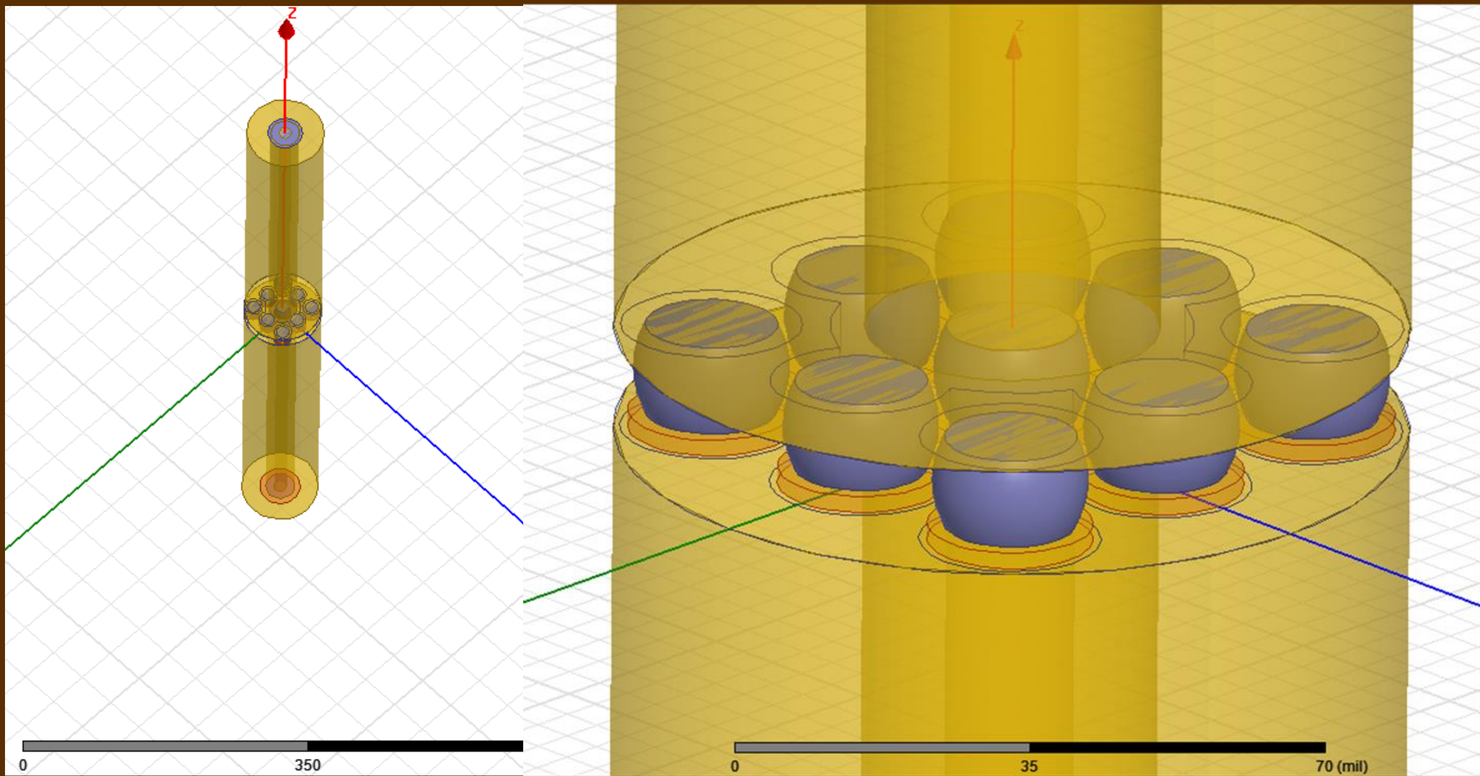


Characterize Only the High Speed Interconnect Performance

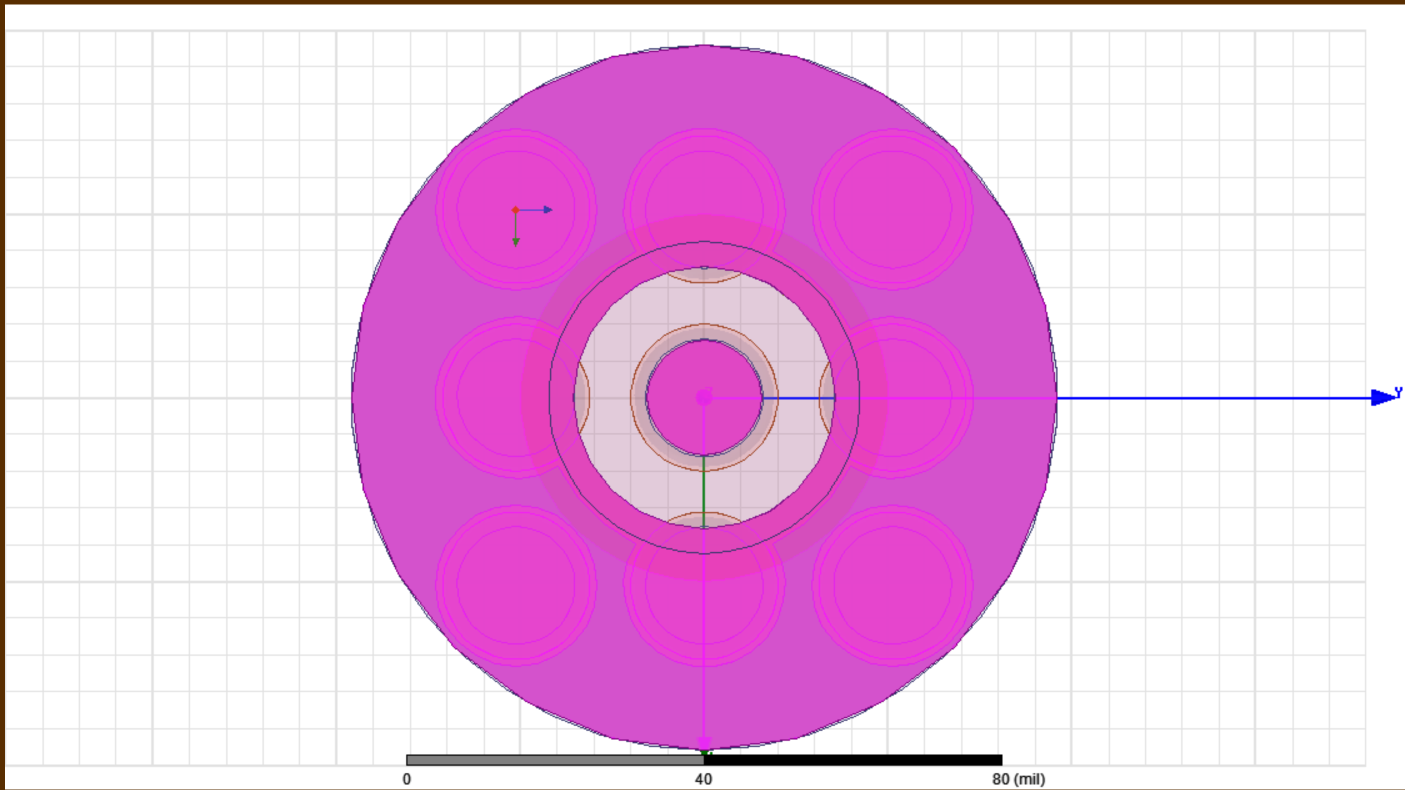
Comparing the two 3D Models- with the Pins / without the Pins



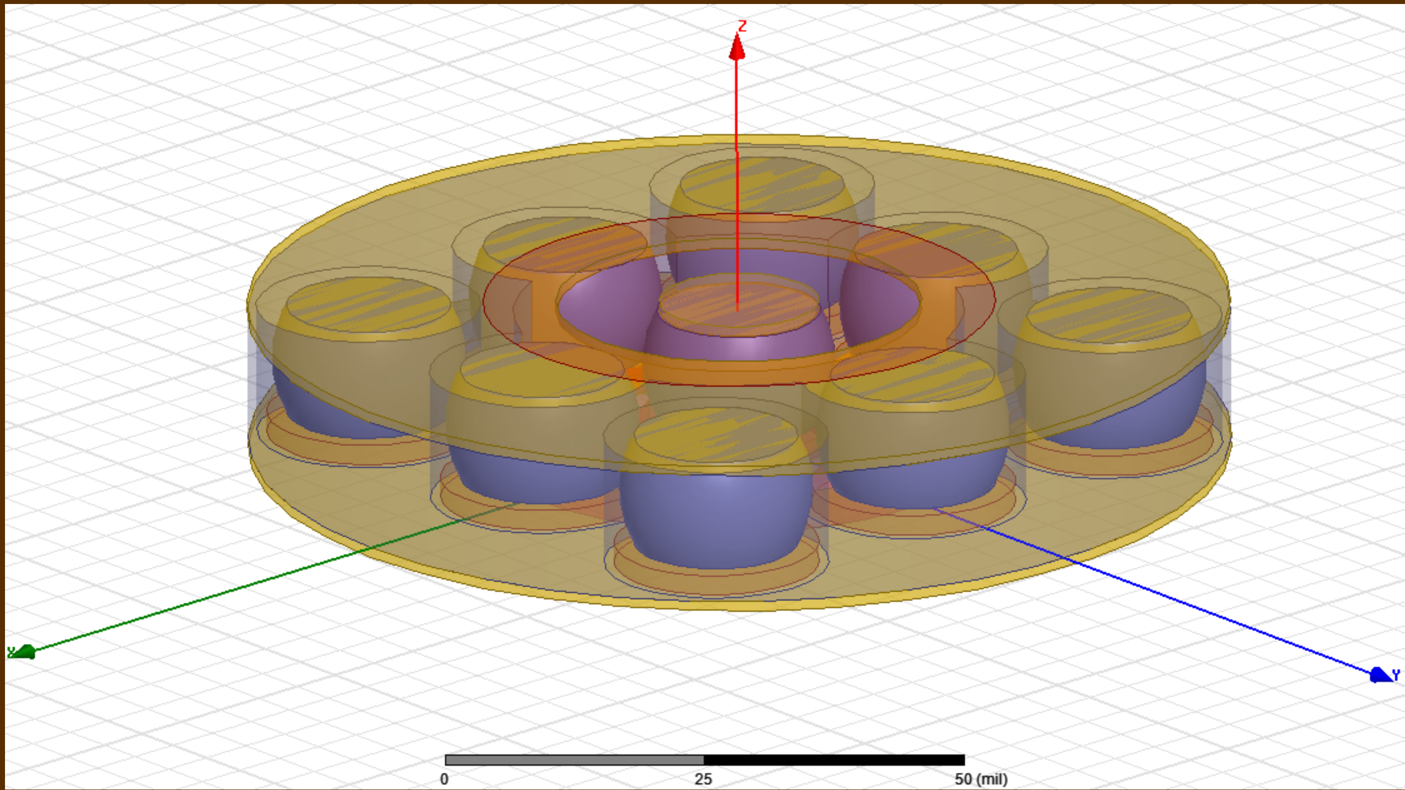
3D Model of Just the Pins, same Electrical properties- with Waveport coaxial launch



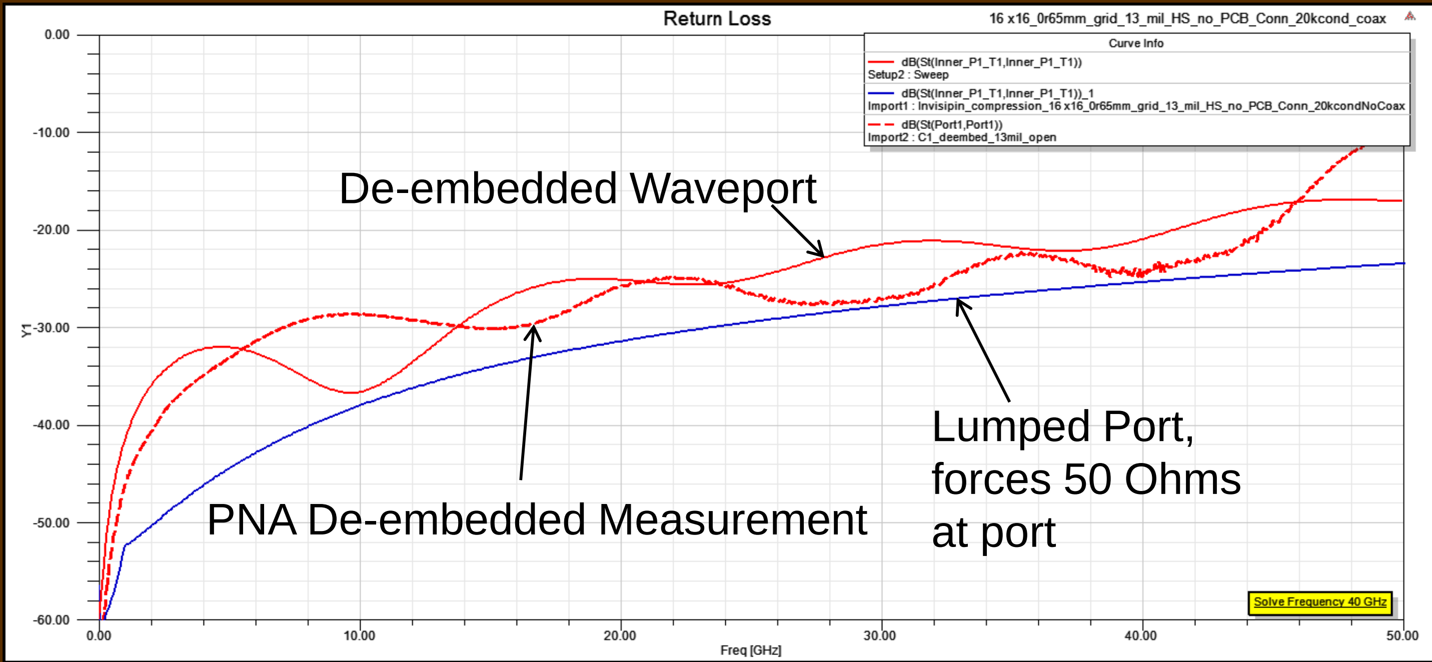
Outer and Inner Conductor of Air Core coax



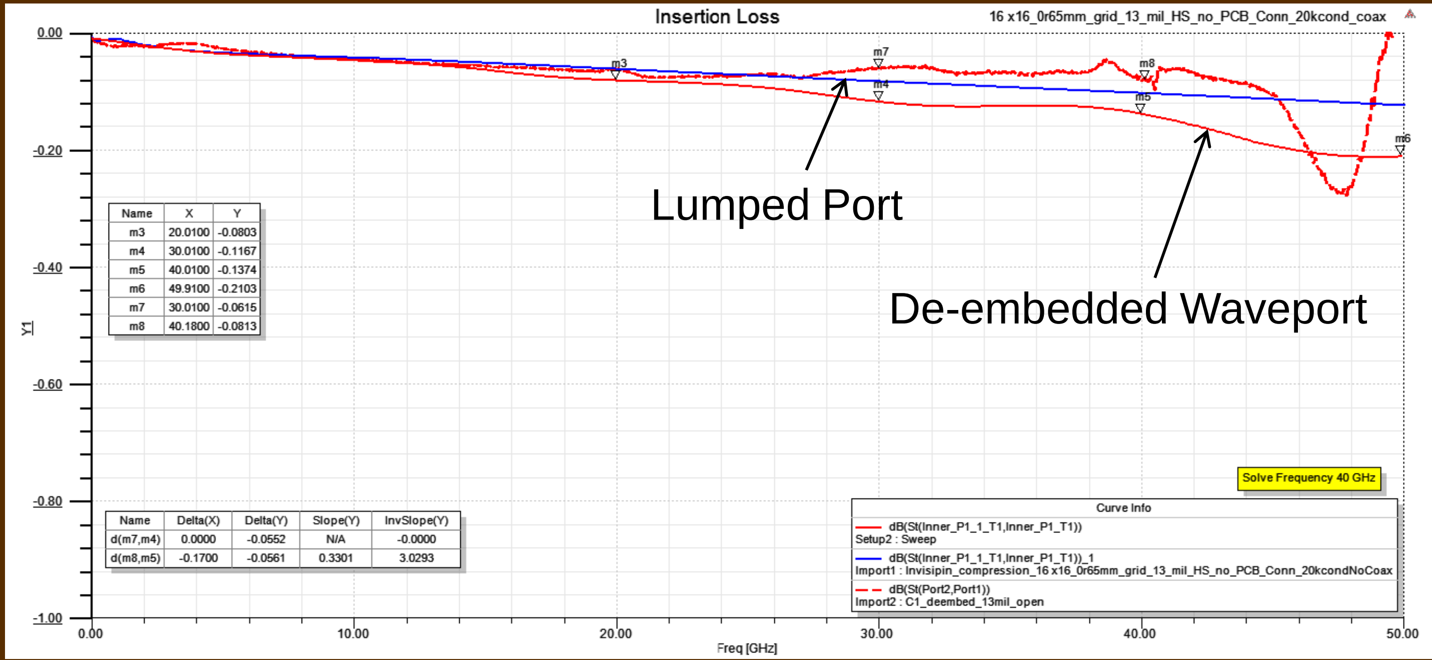
Same diameters on 1 mil thick PEC for the Coaxial Lumped Port



Just the Invisipins HFSS models vs. PNA De-embedded



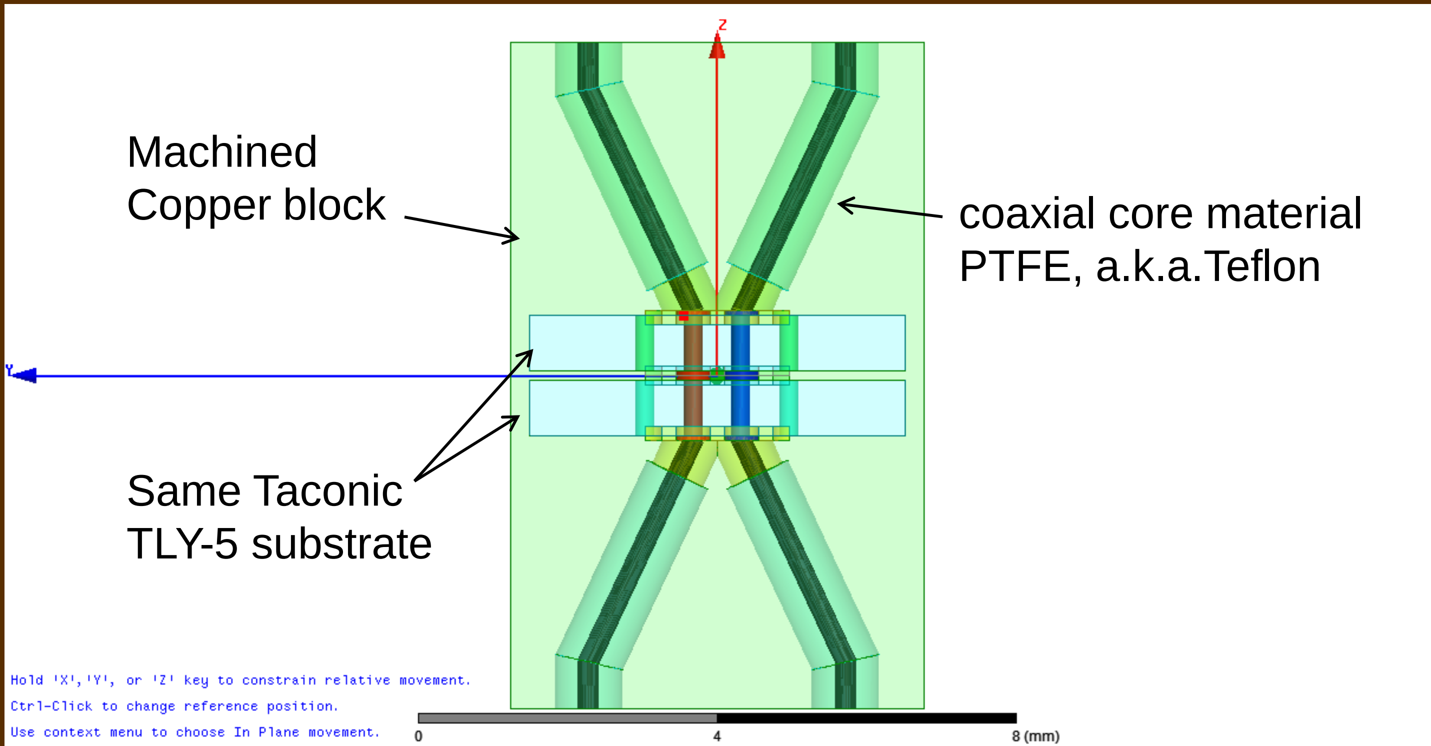
Just the Invisipins
HFSS models vs. PNA De-embedded



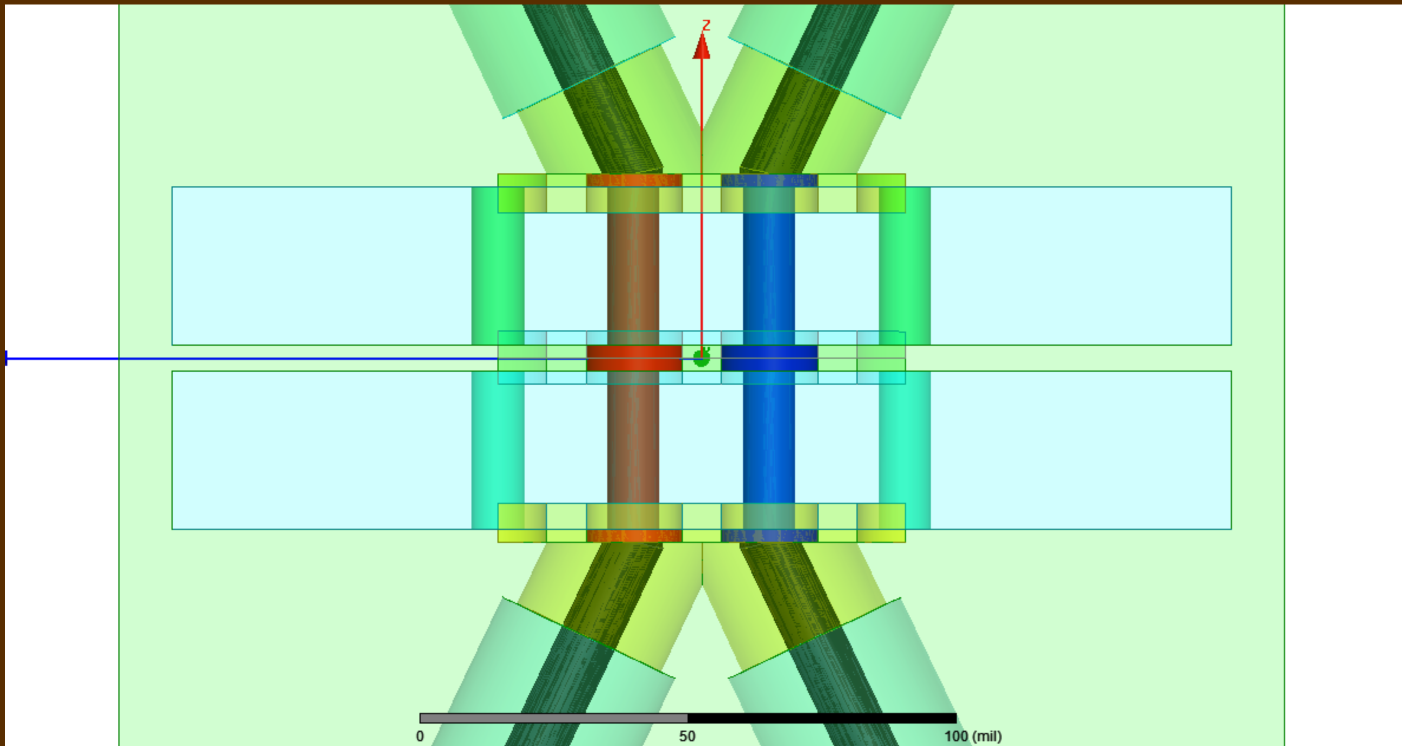
Determine the 3D model for a Differential Interconnect

- Why is Differential Signaling beneficial?
  - Lower voltage swings
  - Immunity from power supply noise
  - Reduce dependency on difficult high frequency RF grounding
  - Improved EMI performance
- Model will vary depending on the exact ***differential signal pin/Ground pin pattern*** being used for your application.

Differential 0.65mm Pitch- No Pins Materials match real construction



Differential 0.65mm Pitch- No Pins
Materials match real construction



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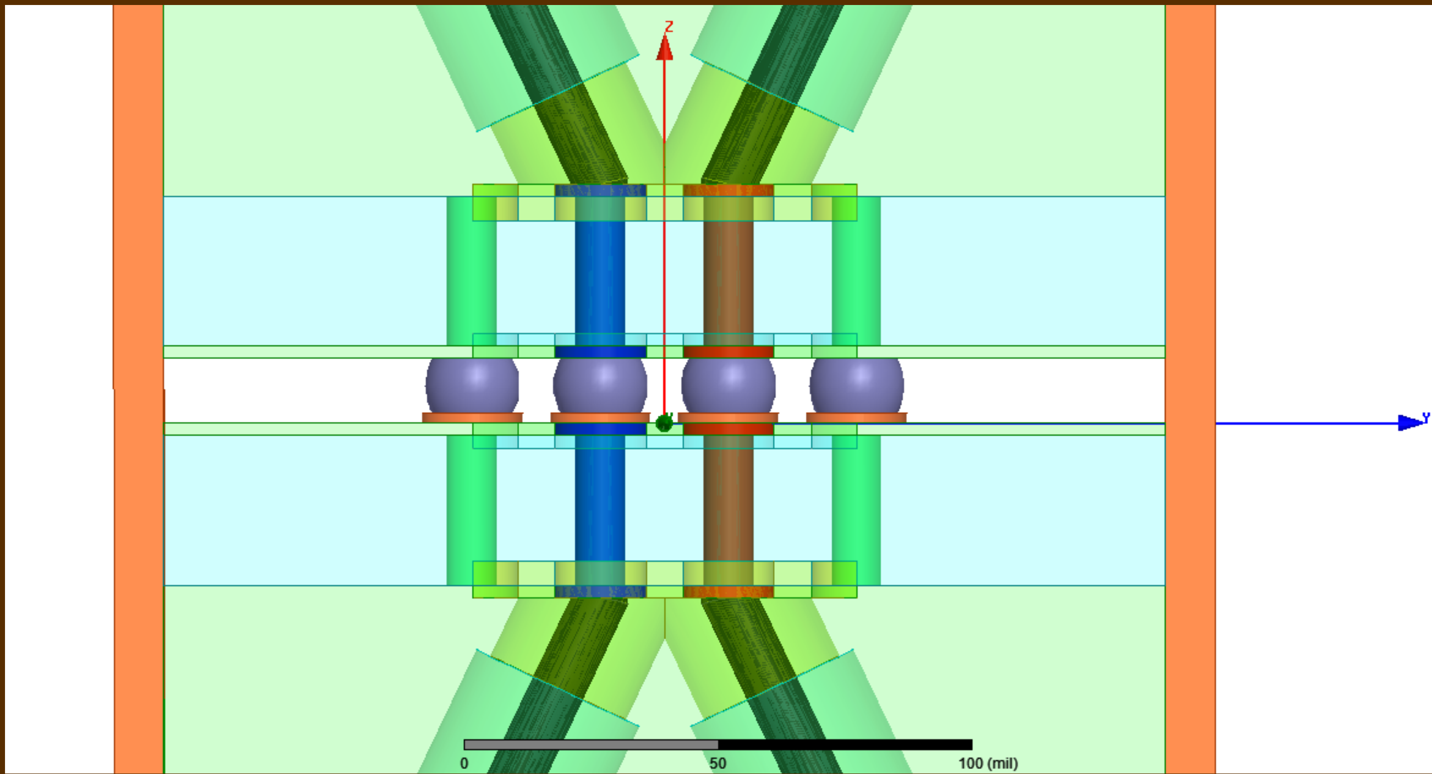
Differential 0.65mm Pitch Pins – Same Electrical Properties



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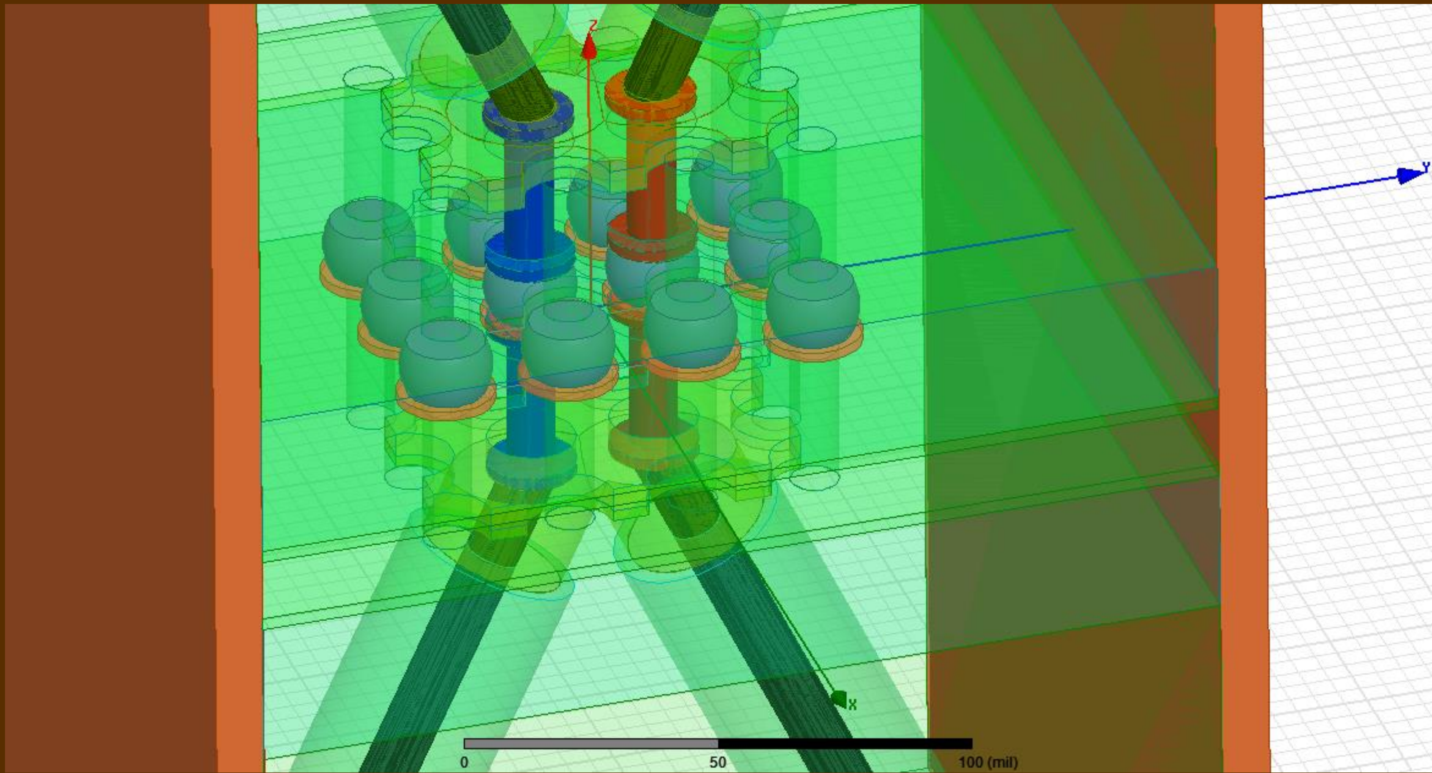
Differential 0.65mm Pitch- Pins
Ground Pins Surrounding Signal pair



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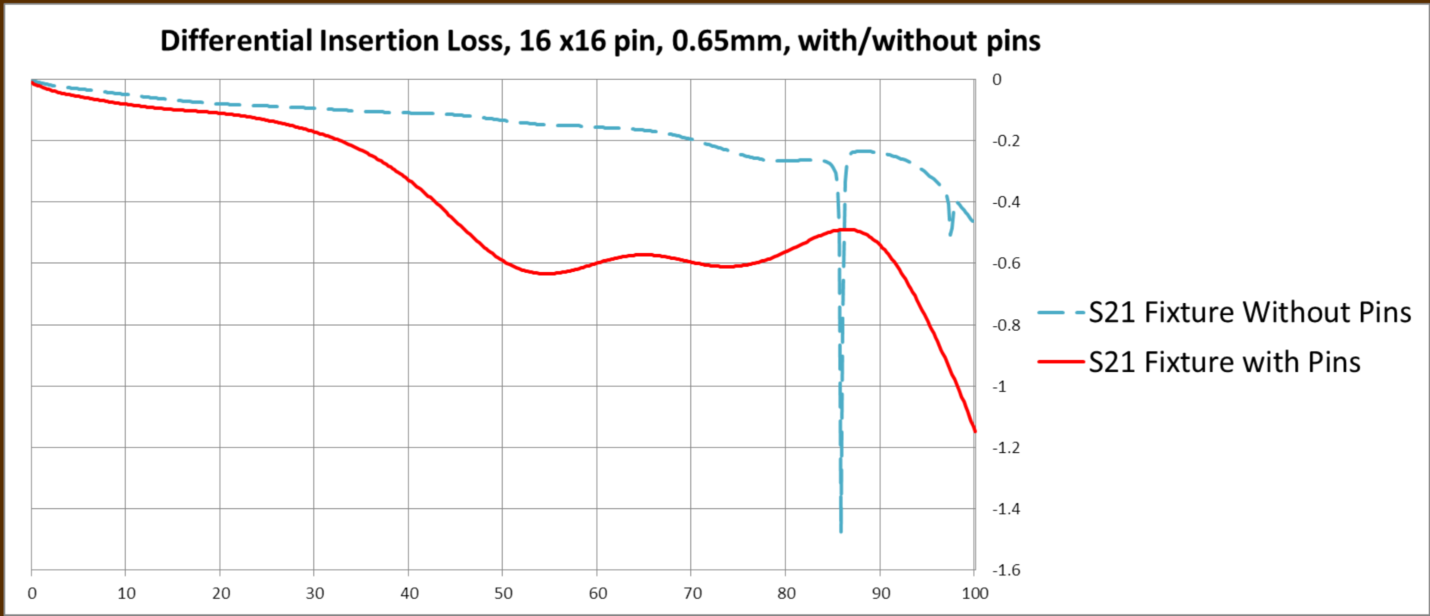
Differential Insertion Loss 0.65mm Pitch- with/without Pins

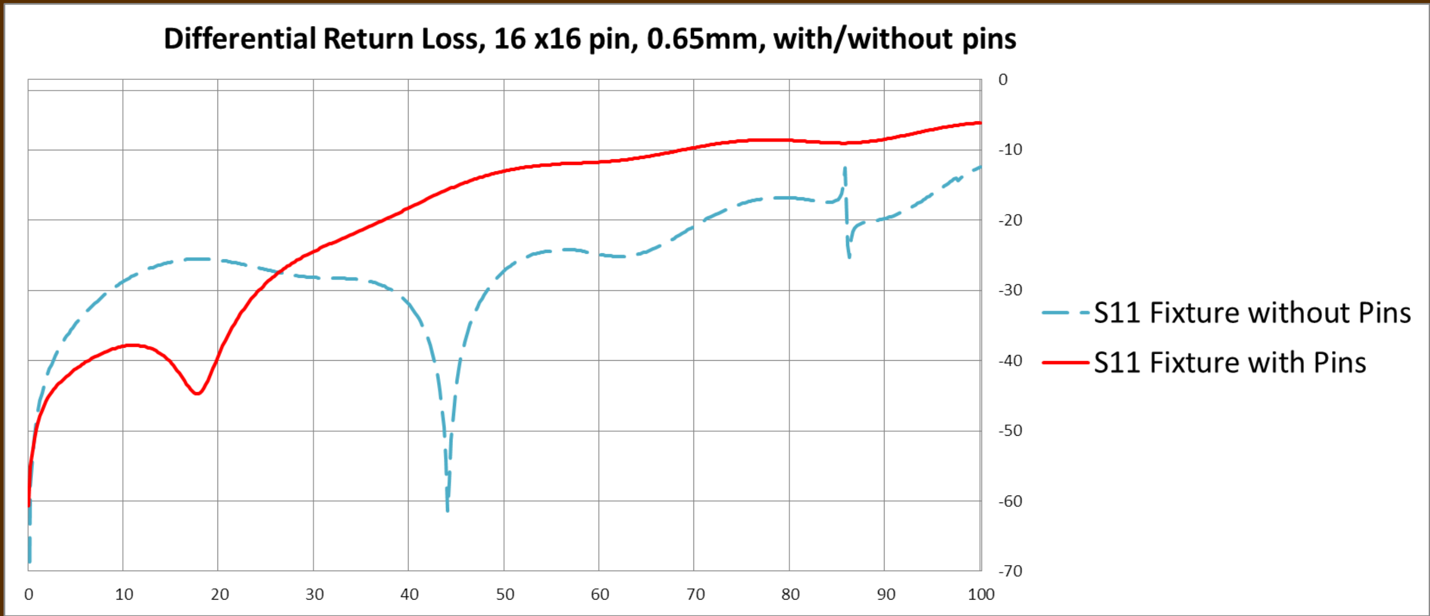
Notice the Frequency Sweep has Doubled



Characterize Only the High Speed Interconnect Performance

Differential Return Loss 0.65mm Pitch- with/without Pins

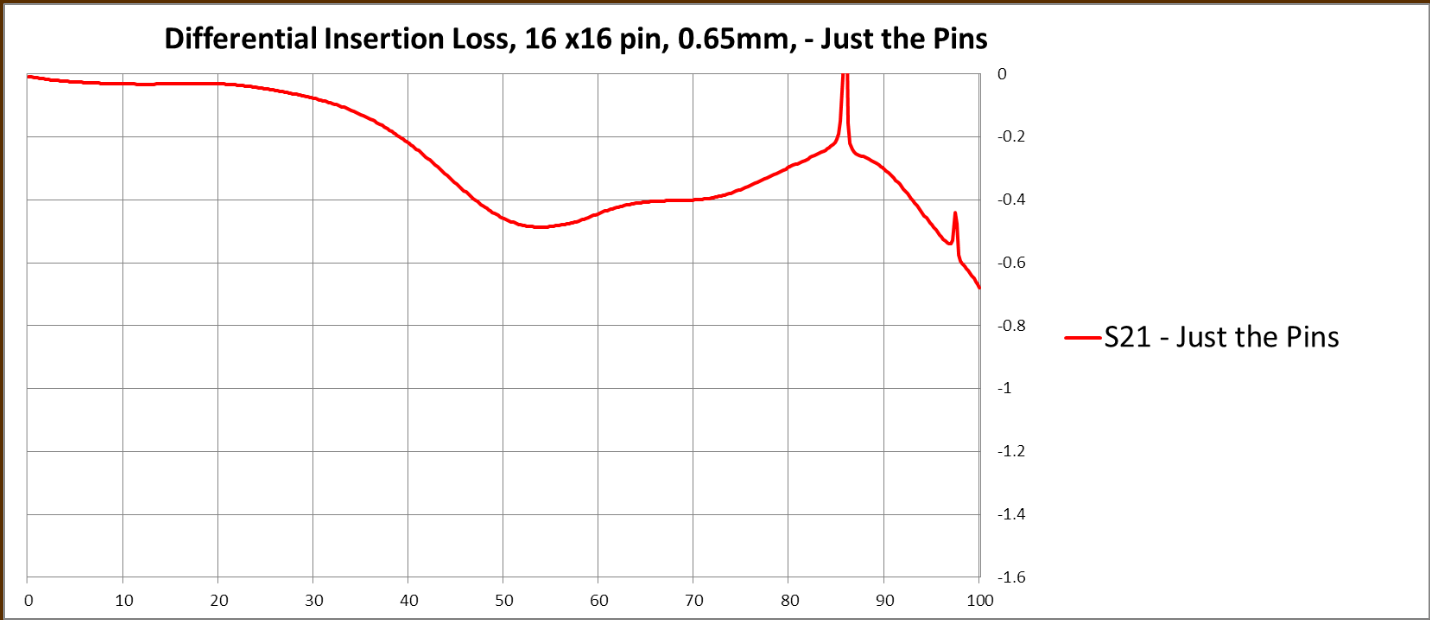
Notice the Frequency Sweep has Doubled



Characterize Only the High Speed Interconnect Performance

Differential Insertion Loss 0.65mm Pitch- Just the Pins

Notice the Frequency Sweep has Doubled



Acknowledgements

- Diagram of S-parameter block, slide 4, http://practicalfmri.blogspot.com/2011/06/physics-for-understanding-fmri_23.html
- **S-parameters Without Tears-** Understand this critical frequency-domain measurement and its interpretations,
  By Colin Warwick and Fangyi Rao, Agilent Technologies
- **Agilent Time Domain Analysis, Using a Network Analyzer,** Application Note 1287-12, Document 5989-5723EN

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- **Keysight Technologies, Physical Layer Test System (PLTS) 2015**, Document 5989-6841EN
- Thomas P. Warwick, HFSS 3D model of Differential Test Fixture