
SEVENTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 6 - 9, 2016
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive- Session 3
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BiTS 2016 Burn-in & Test Strategies Workshop

Session 3
Morten Jensen
Session Chair

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 4:30 pm

Stimulating Simulating

"Optimizing the PCB-to-socket-to-DUT interface"

Gert Hohenwarter - GateWave Northern, Inc.

"Characterize Only the High Speed Interconnect Performance"

Carol McCuen - R&D Altanova

"Modelling, Materials, and Madness"

Mike Gedeon - Materion

BiTS 2016 Burn-in & Test Strategies Workshop

Optimizing the PCB-to-socket Interface

Gert Hohenwarter
GateWave Northern, Inc.

2016 BiTS Workshop
March 6 - 9, 2016

Objective

- Highlight impact of via field design on socket and signal path performance
- Examine methods on how to improve that performance
- Identify some of the unique challenges of designing for automotive radar systems

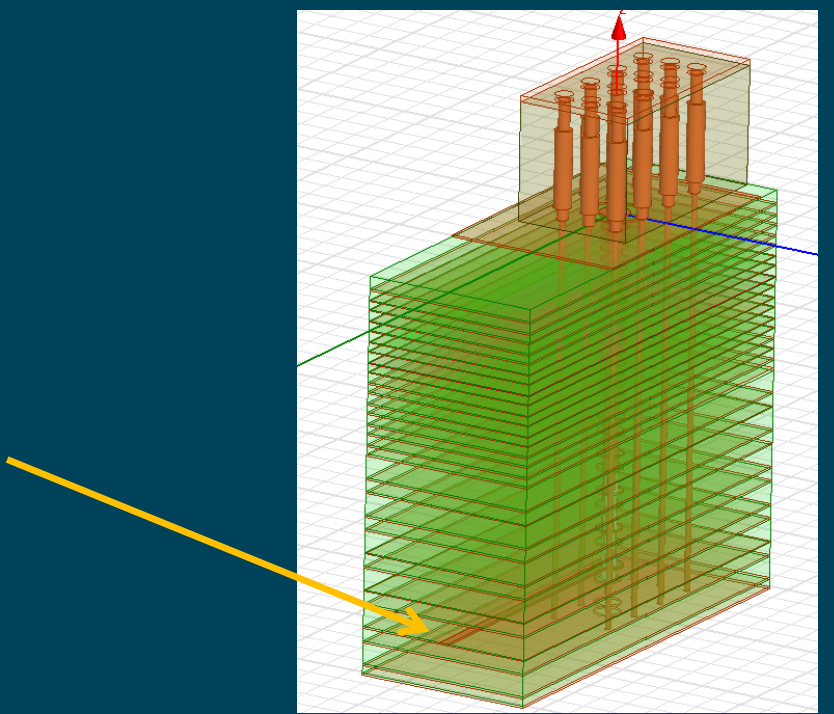
Approach

- Set up simulations that highlight impact of changes in via field on insertion and return loss
- Examine impact of these changes on overall system performance
- Develop criteria regarding interface construction and optimization

Tools

- 40 GHz VNA
- ANSYS HFSS
- Mentor HyperLynx
- SPICE simulator

Socket on via field



Socket driven by signal from deep within PCB

Parameters to consider

- Pad diameters
- Via diameters
- Anti-pad sizes
- Dielectric constants, i.e. PCB materials
- Stubs
- Line widths

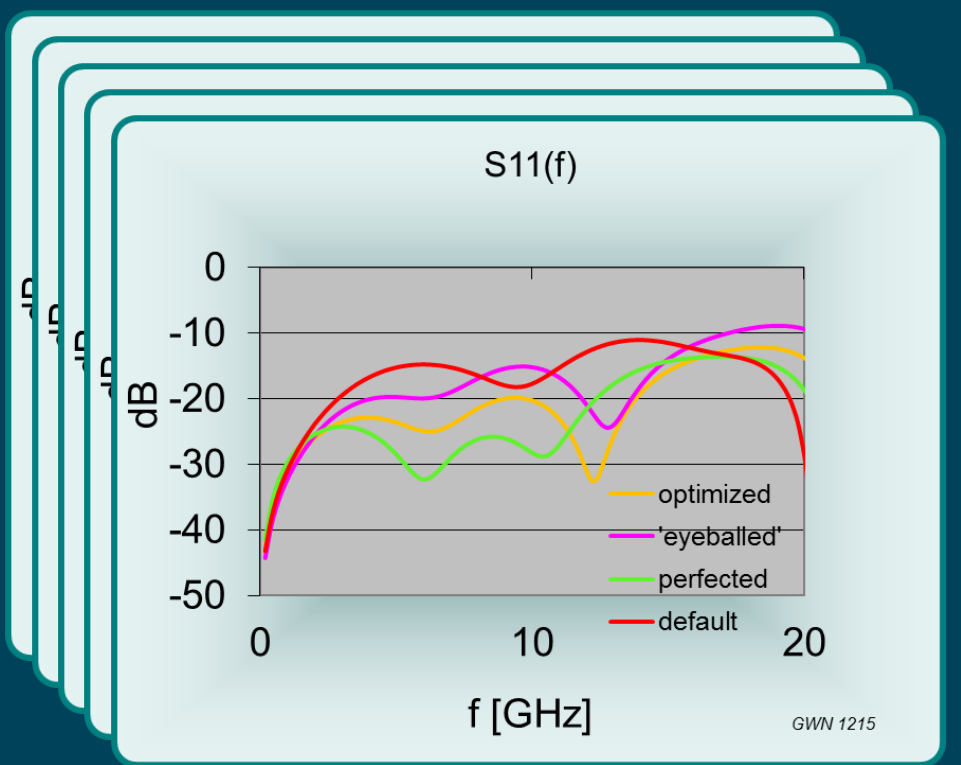
Under control of the PCB designer

Parameters to consider

- Ground locations
- Ball sizes
- IC parameters e.g. routing on IC
- Rise times

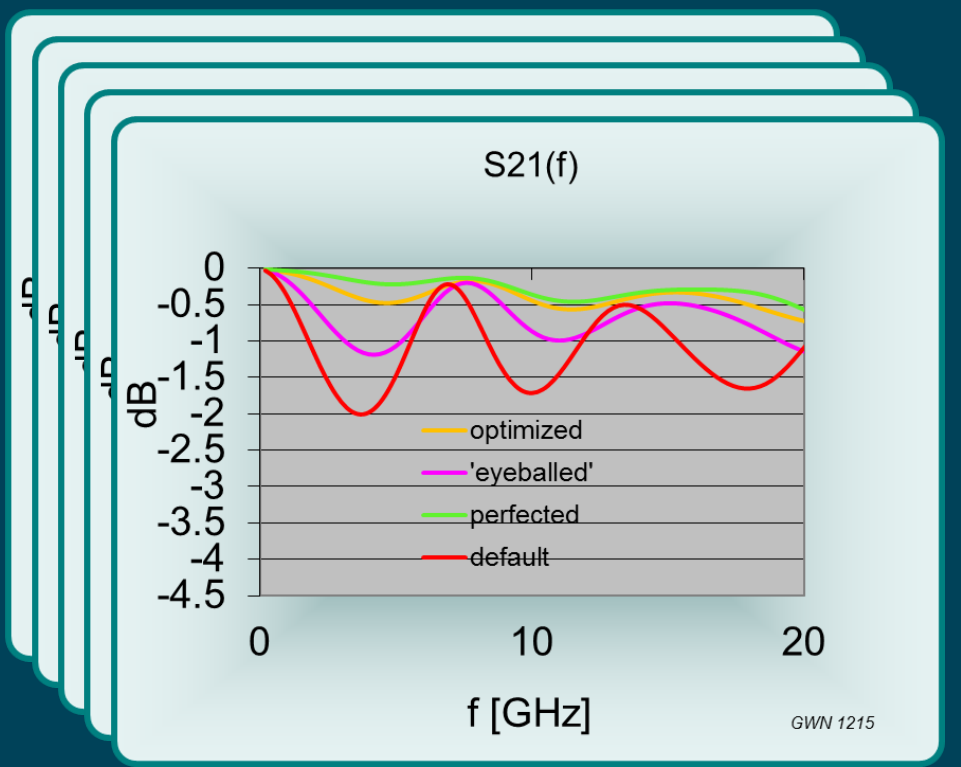
NOT under control of the PCB designer

Return loss S11



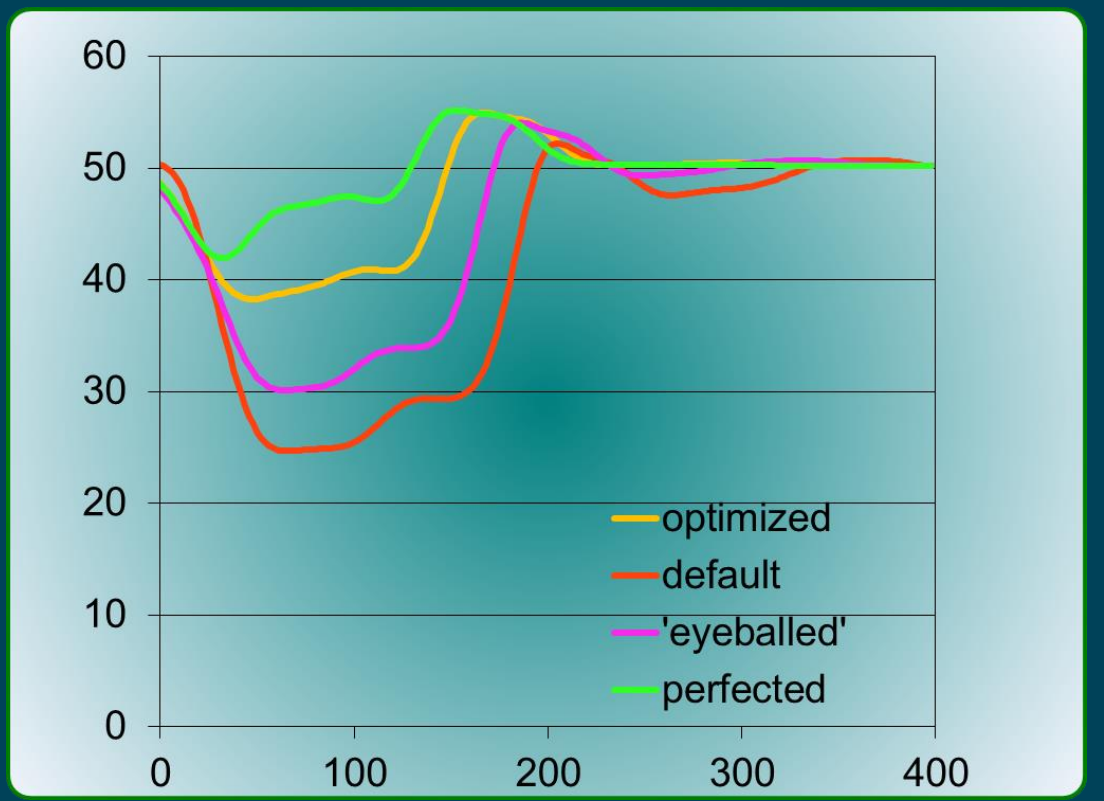
Socket plus via field

Insertion loss S21

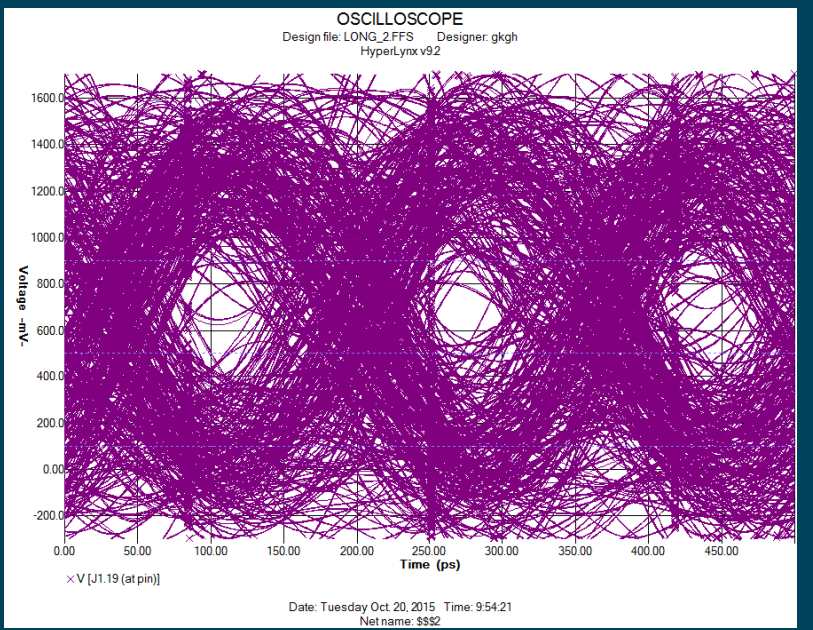


Socket plus via field

Impedance


Ohms
60
50
40
30
20
10
0
0
100
200
300
400
optimized
default
'eyeballed'
perfected
Socket plus via field
ps

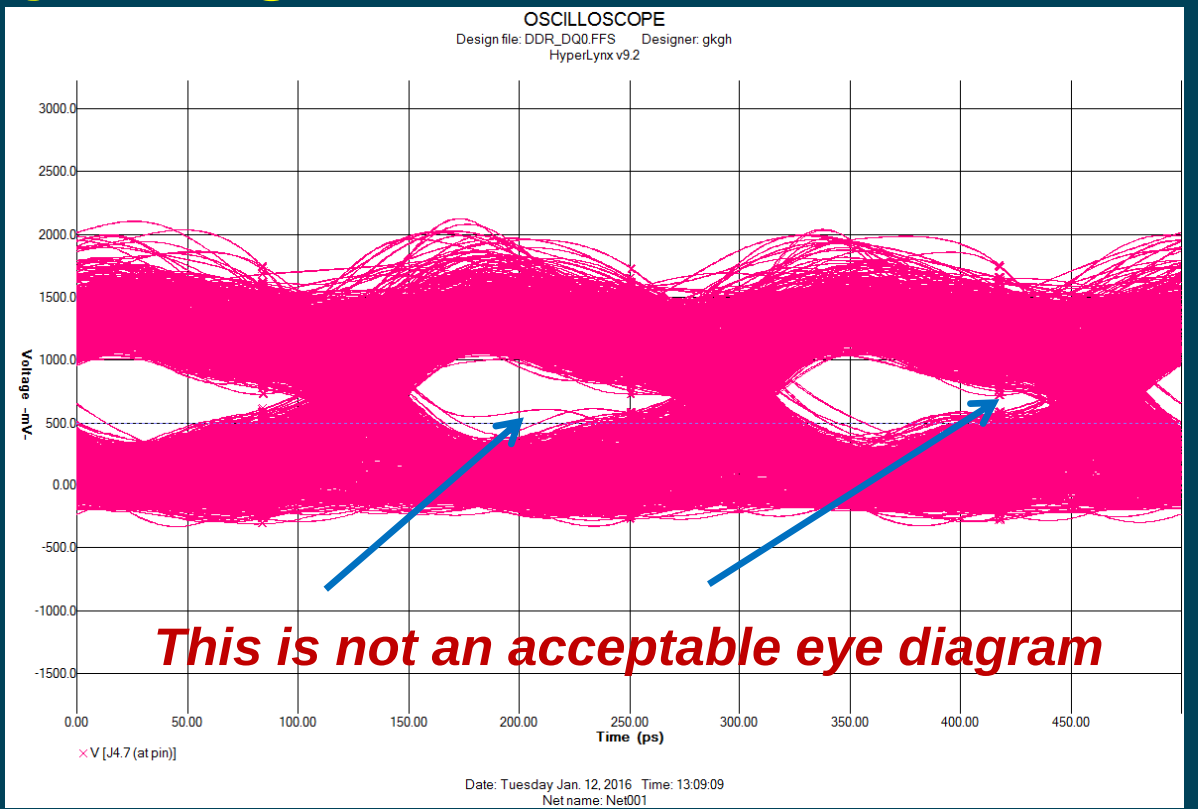
Eye diagram of PCB with socket



There is no point investigating the difference between optimized and unoptimized via fields in this case

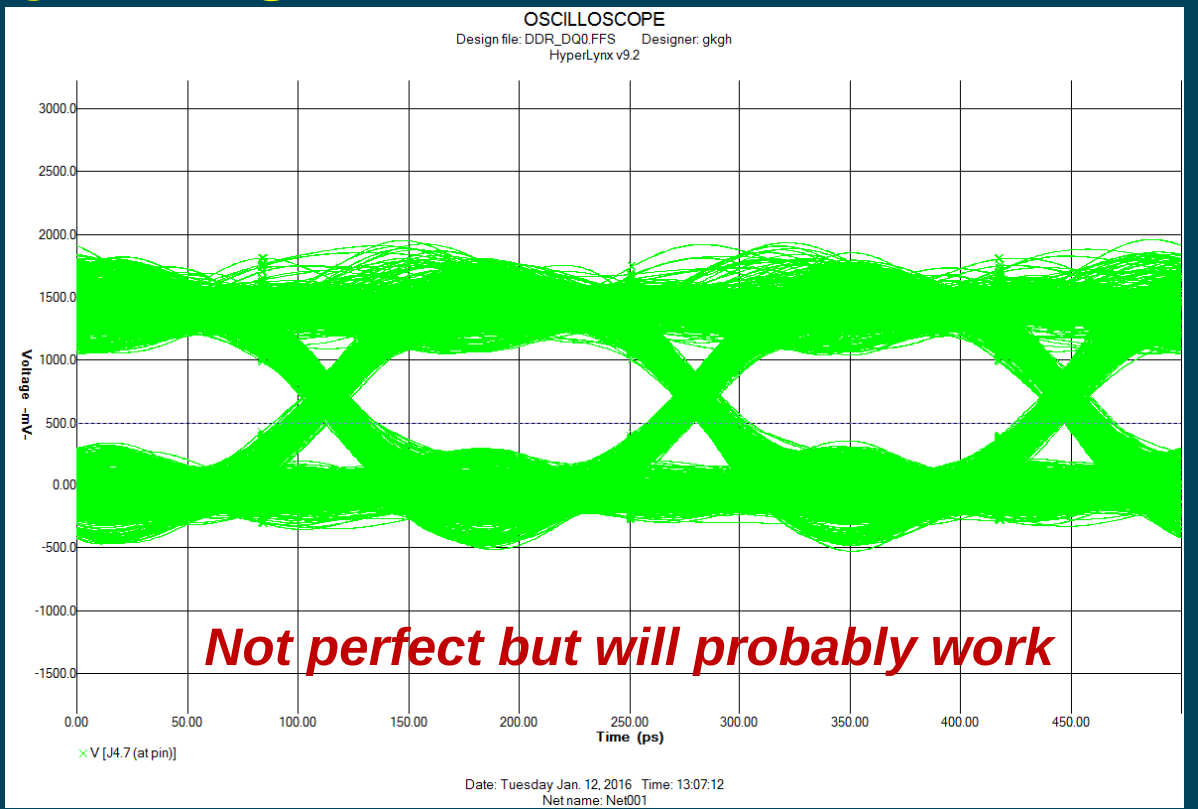
Long lines, 6 GB/s, optimized interface

Eye diagram of PCB with socket



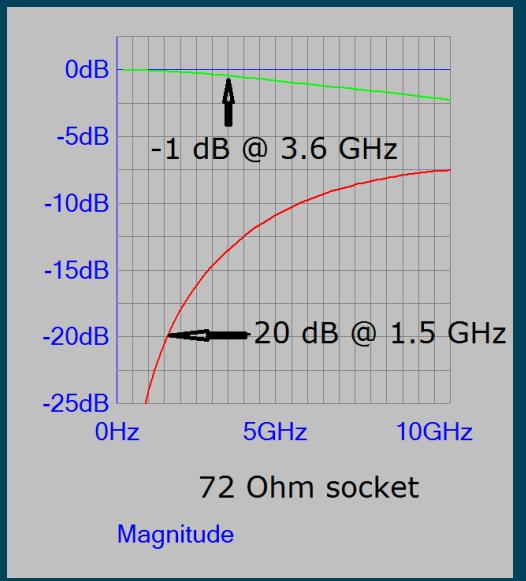
Short lines, 6 GB/s, default interface

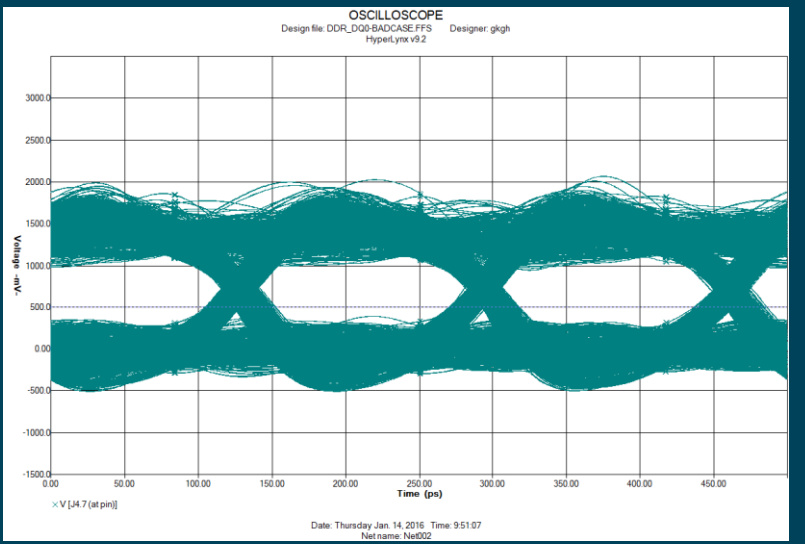
Eye diagram of PCB with socket



Short lines, 6 GB/s, optimized interface

Eye diagram of PCB with socket





This is also a form of optimization

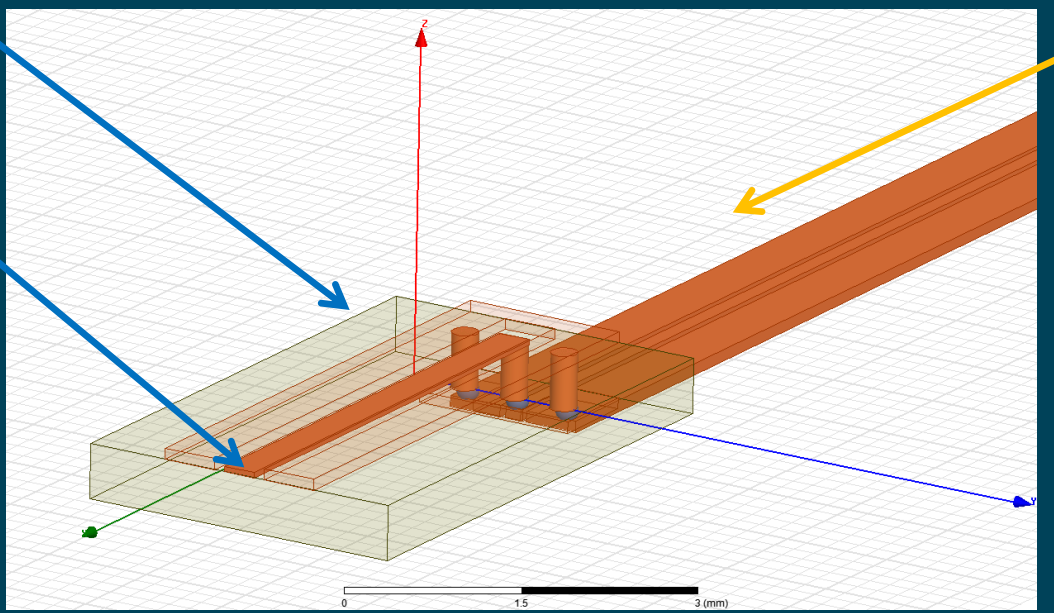
Short lines, 6 GB/s, 35 Ohm PCB – 72 Ohm socket

Automotive Radar Example

Die

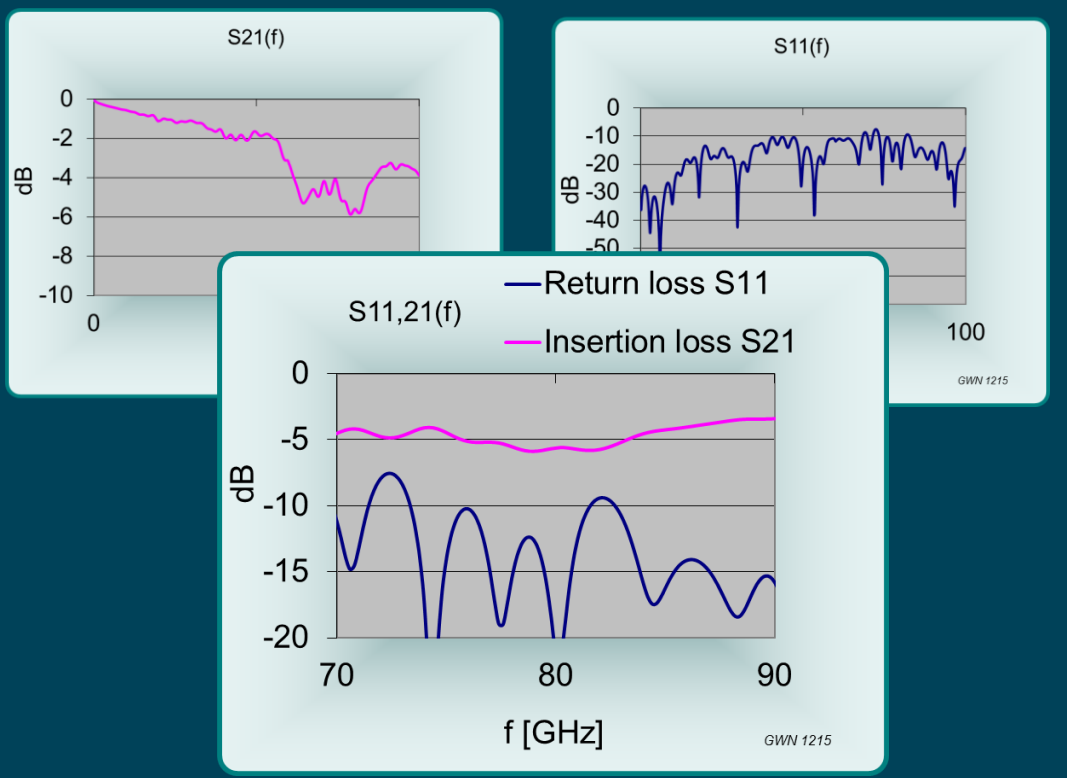
On-die RX / TX

Signal in



IC interfaced to high speed CPW

Performance with CPW

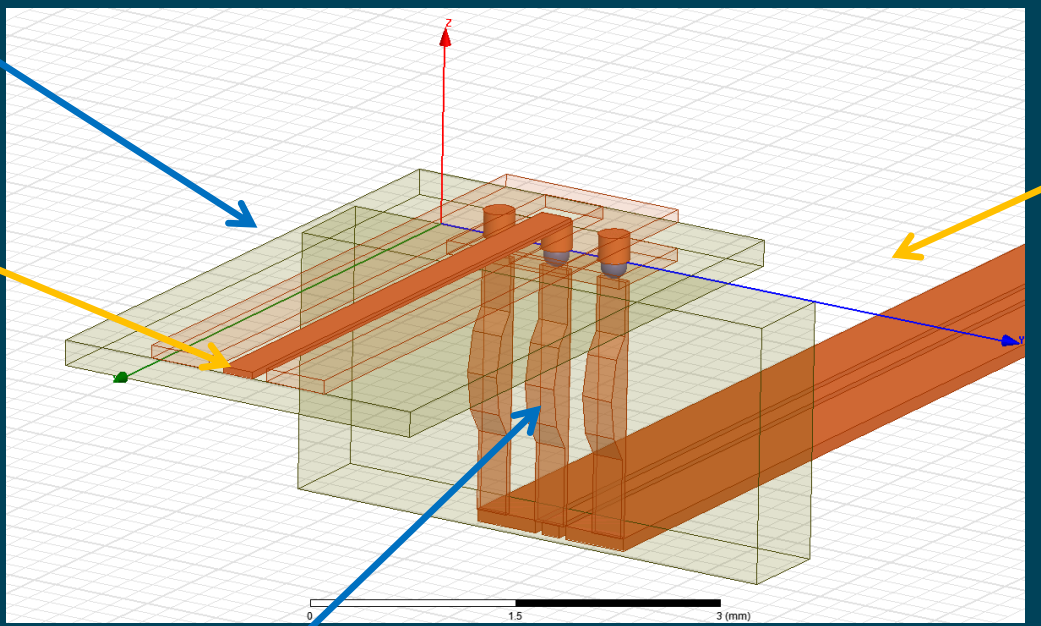


Smooth insertion loss response

Automotive Radar Socket

Die

On-die RX / TX

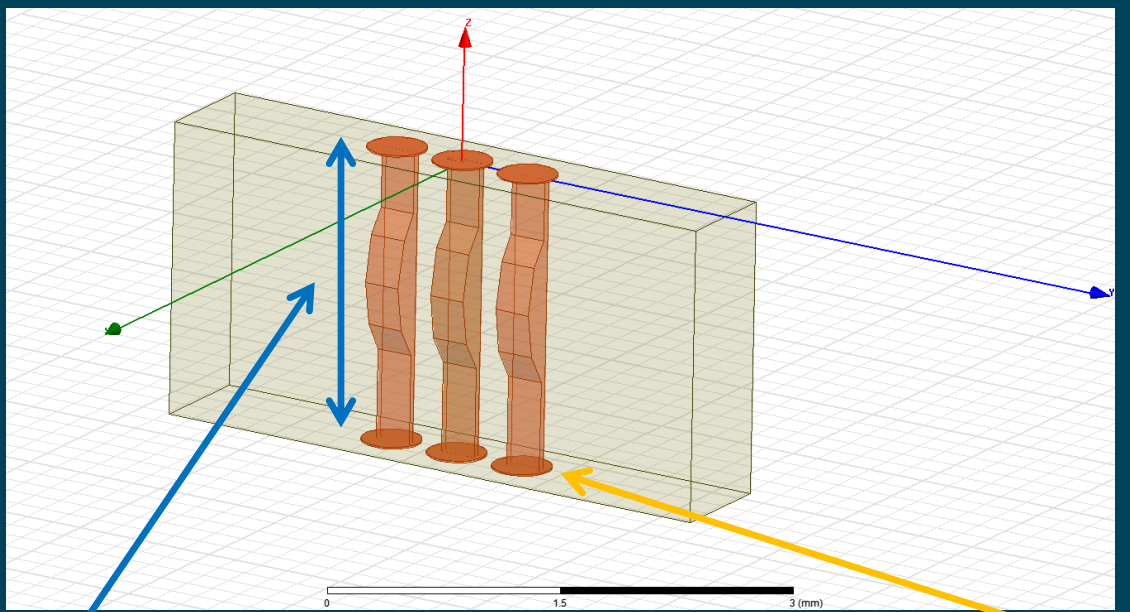


Signal in

Socket example

IC interfaced to high speed CPW via G-S-G socket

Examine Impact of Two Variables



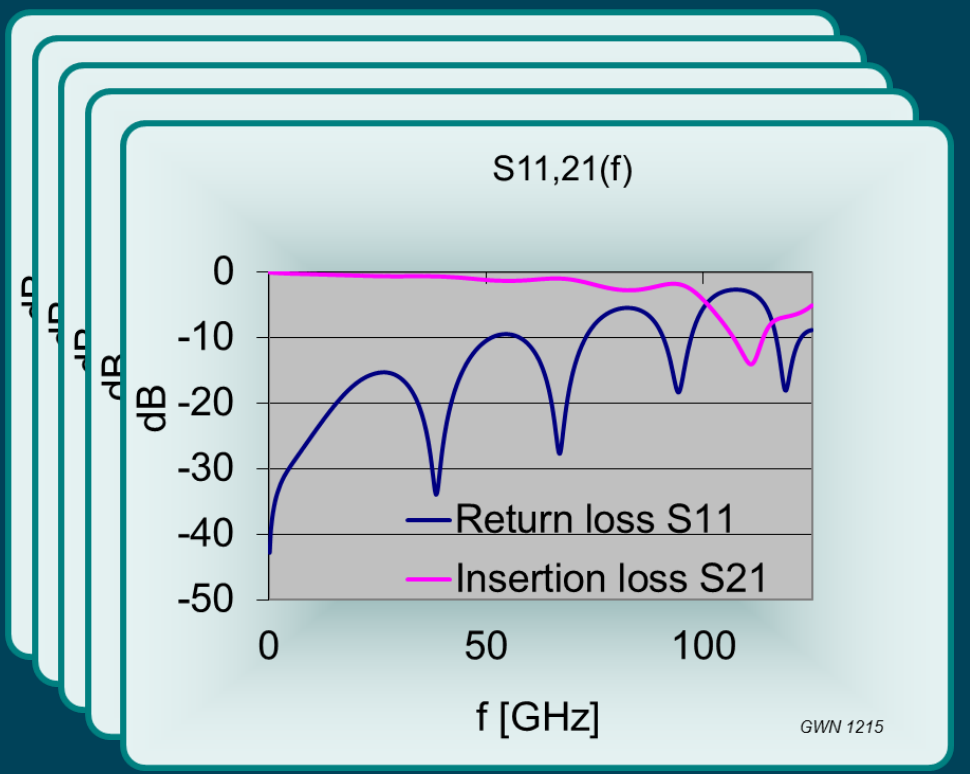
Pad spacing

Pad diameter

Pitch is generally not available for optimization

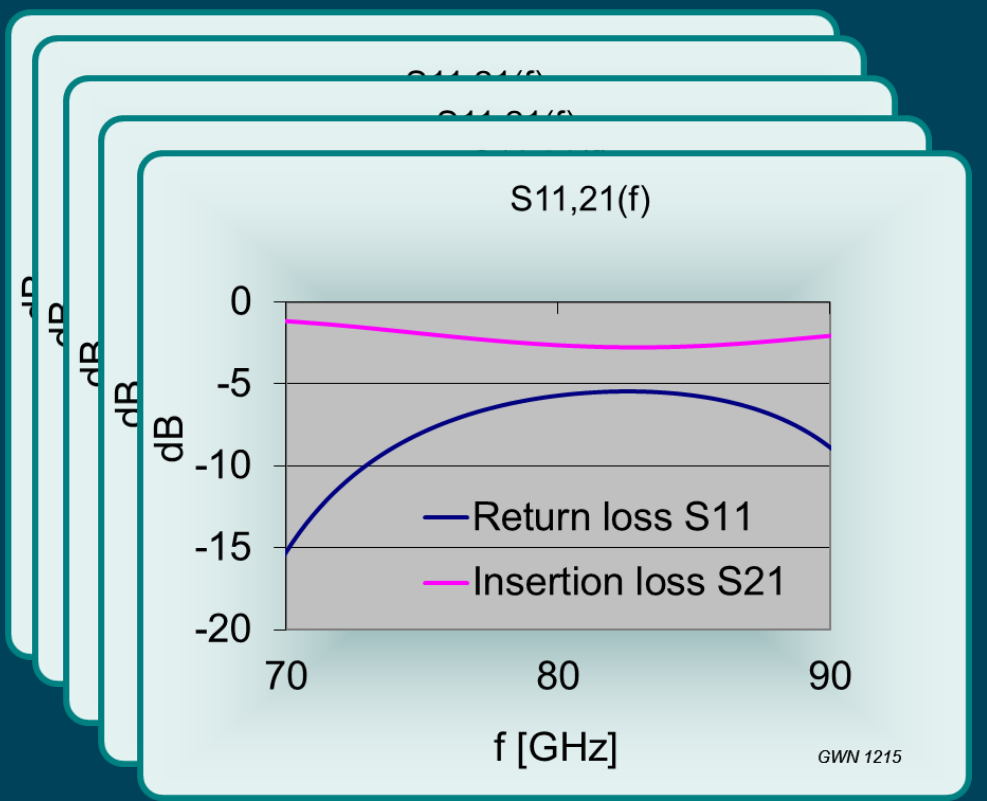
'Generic' contact interface

Return and insertion loss



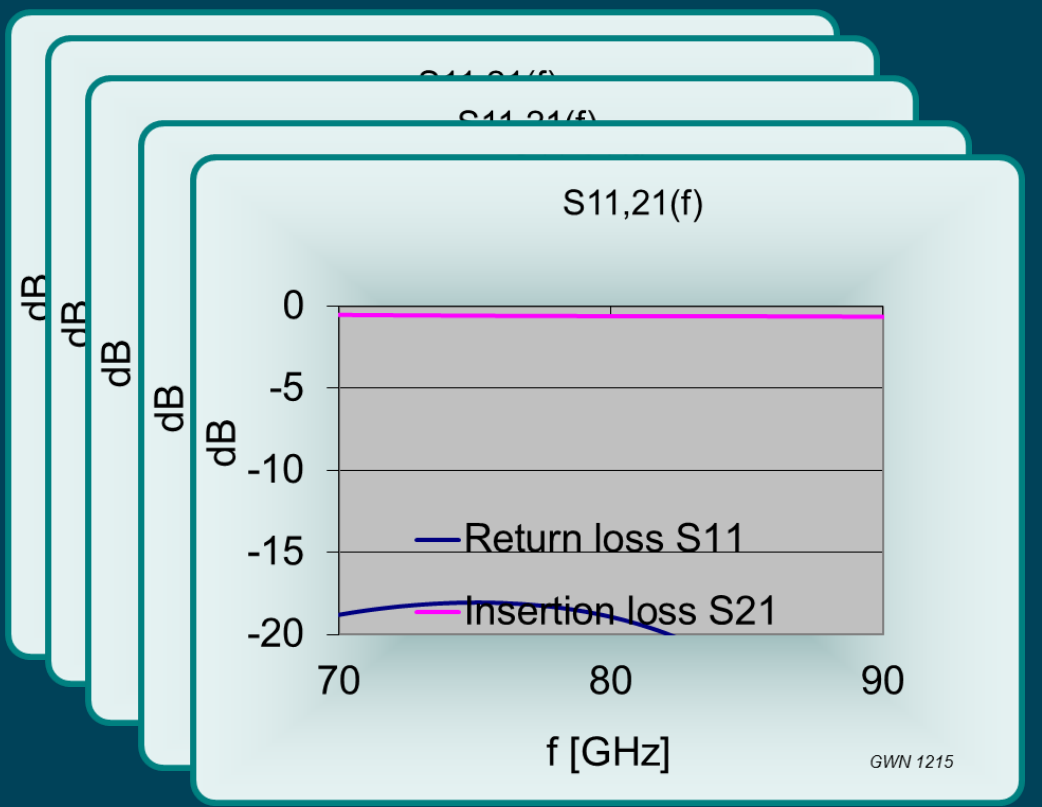
Pin length shifts frequency of S11 ‘resonances’

Return and insertion loss



Pin length has significant impact on return loss in frequency range of interest

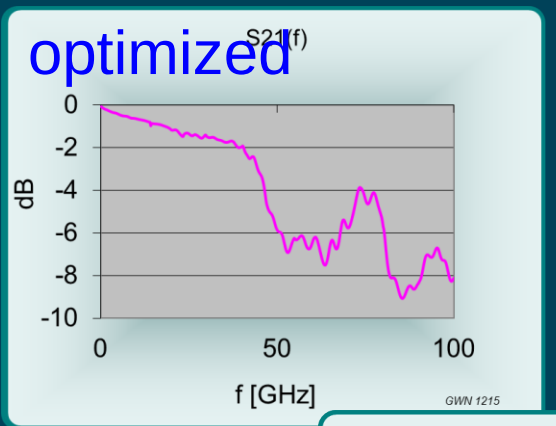
Return and insertion loss

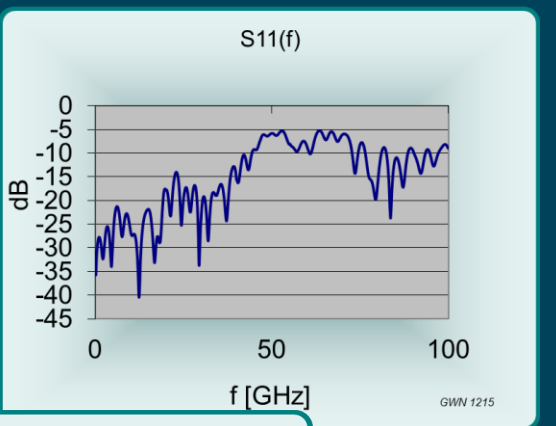


Pad diameter also severely impacts return loss S11

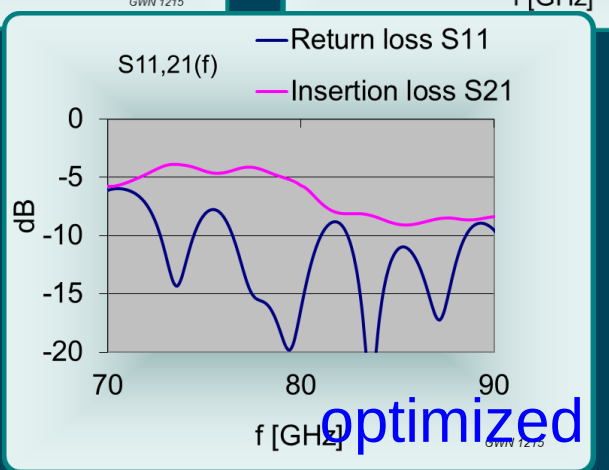
Performance with Socket

optimized





In the range of interest…



Conclusion

- Inattentive via field design will impact socket performance
- A ‘good’ socket may not work as well in such an application while a ‘bad’ one might
- Automotive radar interfaces demand careful attention to interface and signal path optimization