SEVENTEENTH ANNUAL

BiTS™

Burn-in & Test Strategies Workshop

March 6 - 9, 2016

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive- Session 2

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BiTS 2016 Burn-in & Test Strategies Workshop

Session 2
Ashok Kabadi
Session Chair

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 1:30 pm

Material Matters

"Long Life Probe Pin by Electroforming Process"
Makota Kondo & Hirotada Teranishi - Omron Corporation
Takahiro Sakai & Naoyuki Kimura - Omron Corporation

"Carbon Nanotube Polymer Composites as High Performance Thermal Interface Materials for Burn in and Test Applications"
Leonardo Prinzi - Georgia Institute of Technology
Craig Green & Baratunde Cola - Carbice Nanotechnologies, Inc.

"Requirements and Solutions for Test PCBs"
Markku Jamsa - Aspocomp Group Oyj

"PCB Test Fixture and Socket Challenges for mmWave Applications"
Don Thompson Jose - R&D Altanova
Jose Moreira - Advantest Europe GmbH
Giovanni Bianchi - Advantest

BiTS Burn-in & Test Strategies Workshop 2016

Requirements and Solutions for Test PCBs

Markku Jämsä
Aspocomp Group plc

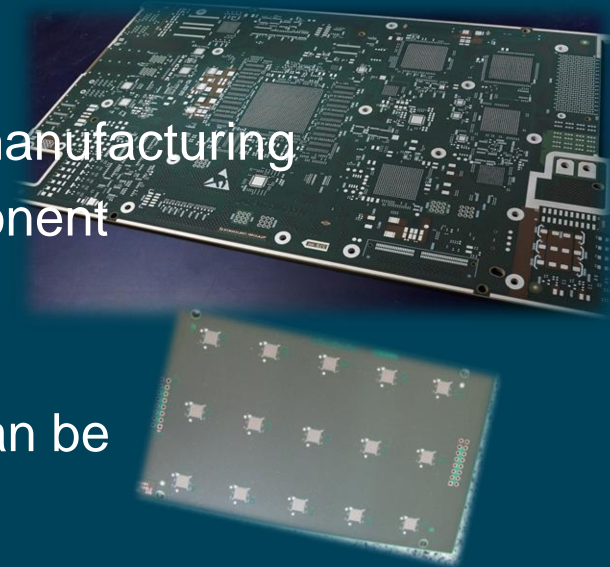
2016 BiTS Workshop
March 6 - 9, 2016

ASPOCOMP
PCB Technology Company

Test PCBs in the Test Systems

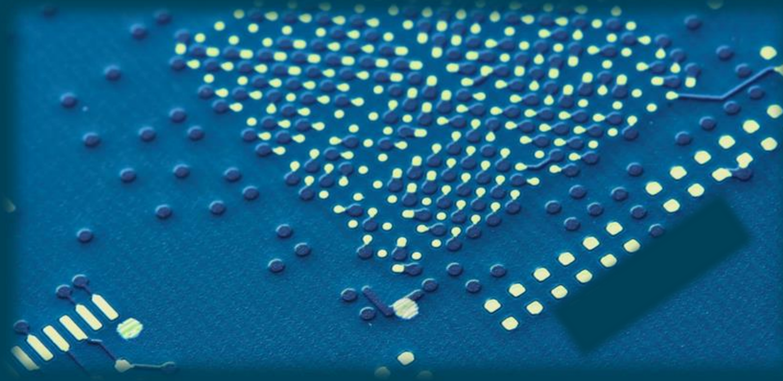
- PCB is a key component for several IC testing applications including:
  - IC ATE testing in component manufacturing
  - Reliability testing during component qualification

PCB manufacturing lead times can be bottleneck regarding the project schedules



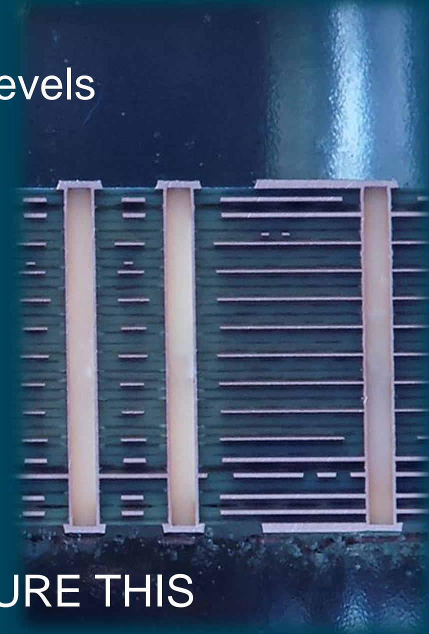
IC ATE PCBs, Typical Technical Requirements

- High packaging density combined to large PCB
- Impedance match, insertion loss minimize
- Other signal integrity items
- Flatness
- PCB assisted cooling
- And a few more



IC Test Board Example

- PCB size 250 x 450mm (9”x18”)
- 3,7mm (0,15 inch); 24 Layers, no HDI
- Epoxy filled / over plated vias, back-drill in 6 levels
- Via size 0,25mm (10mils), Aspect ratio 15
- PTH to Cu Clearance 180u /7 mils
- Low loss material EM828
- 12 impedance control configurations
- Dielectric thickness 75-150u (3-6 mils)
- Line width 75/90u (3/3,5mils)



- NEW STACK-UP, 1ST TIME TO MANUFACTURE THIS STACK-UP

Test Board in Quick Turn Around (QTA) Manufacturing

5 day manufacturing requires at least following:

- All laminate raw materials must be in hand
- All technology features tested and agreed in advance
- Dimensional parameters are known in advance
- Impedance and other signal integrity matters pre-set

Target is to make the example PCB in 5 working days, how to make it happen?

Key Issues to Prepare for This QTA Batch

– Dimensional (shrinkage) control of the new stack-up
– Impedance details and tolerances
– Insertion loss and material choices
– Cooling details and design guidelines for it
– Prepare with the laminates if any missing

– Agree in advance as much commercial matter as possible

Dimensional Control Challenge

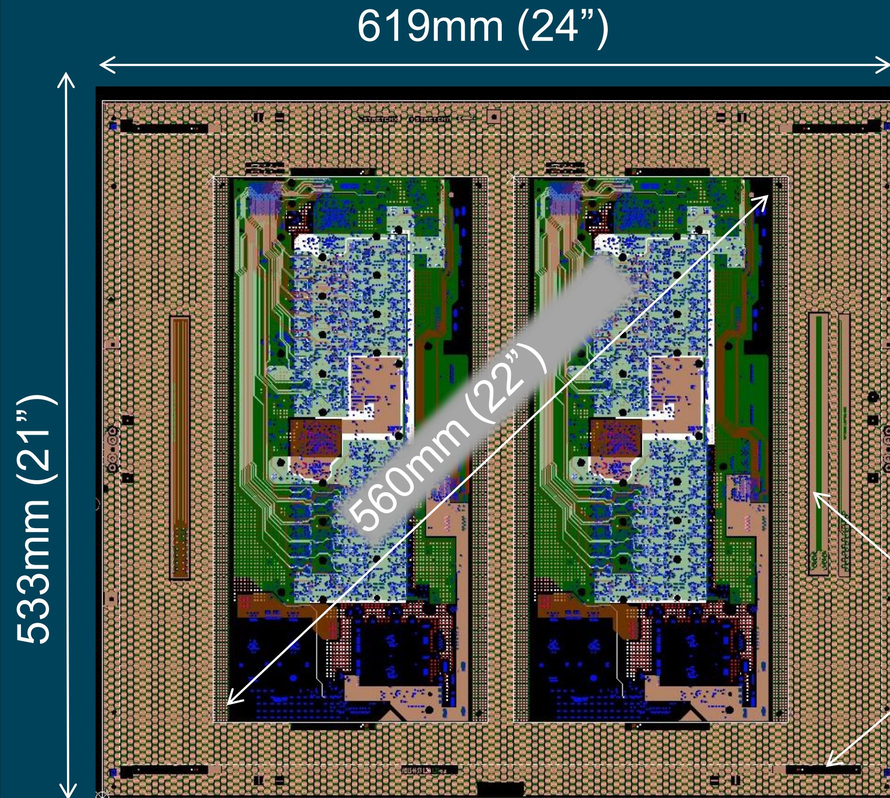
PCB is based on organic substrate, x-y dimensions change (shrink) during the manufacturing

Each inner layer in this PCB will shrink in magnitude of 8-12 mils, each layer in individual manner*

Shrinkage is stack-up sensitive, but repeat-able

* Depending on the materials and number of sequential laminations, the values can be much higher in some cases

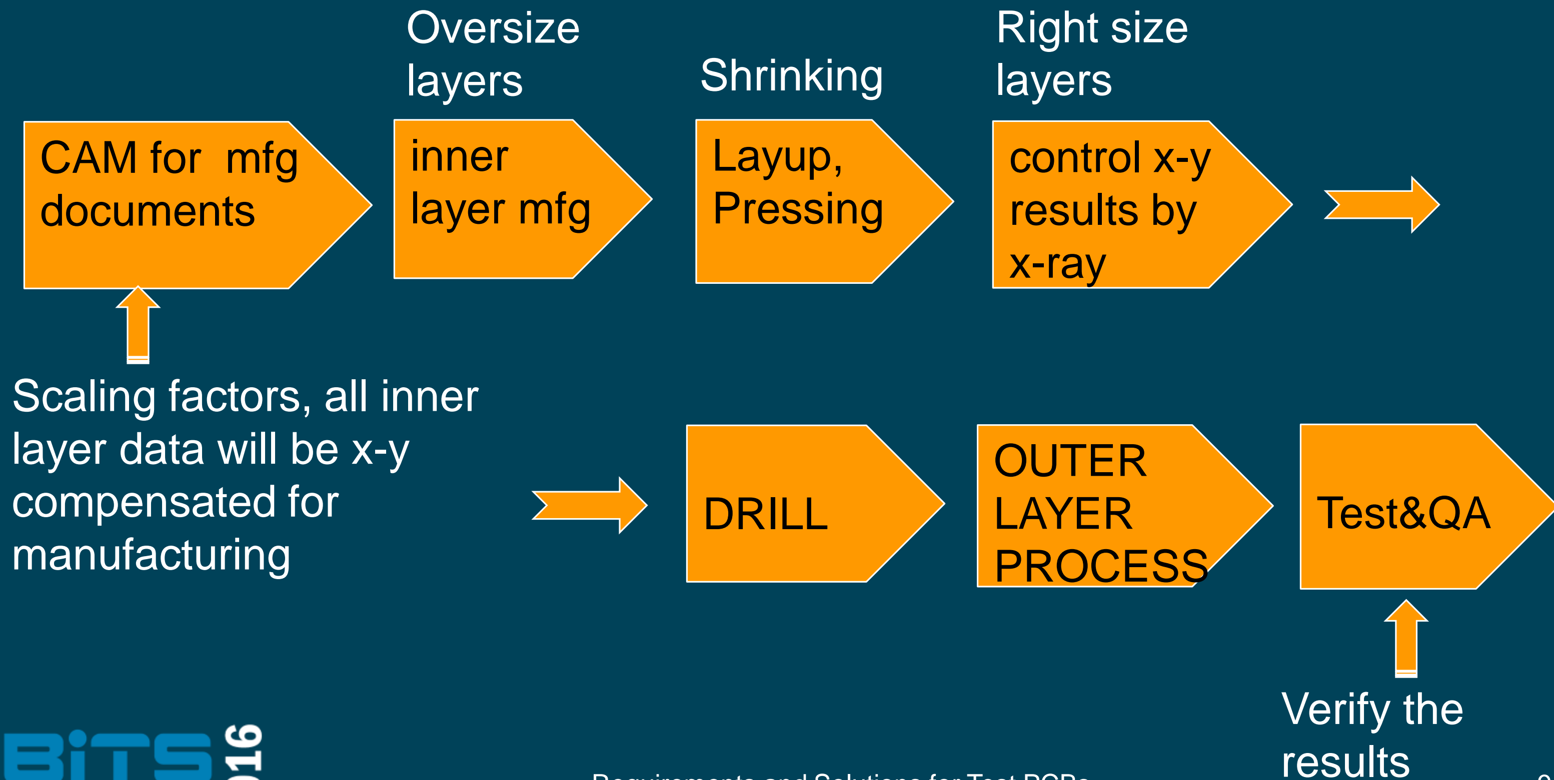
Inner Layer Production Panel



Dimensional control is a key regarding functionality, PCB yield and cost

Impedance coupons

Layer x-y position targets


Dimensional Control,
Simplified Multilayer Process
Oversize layers
Shrinking
Right size layers
CAM for mfg documents
inner layer mfg
Layup, Pressing
control x-y results by x-ray
Scaling factors, all inner layer data will be x-y compensated for manufacturing
DRILL
OUTER LAYER PROCESS
Test&QA
Verify the results
Requirements and Solutions for Test PCBs
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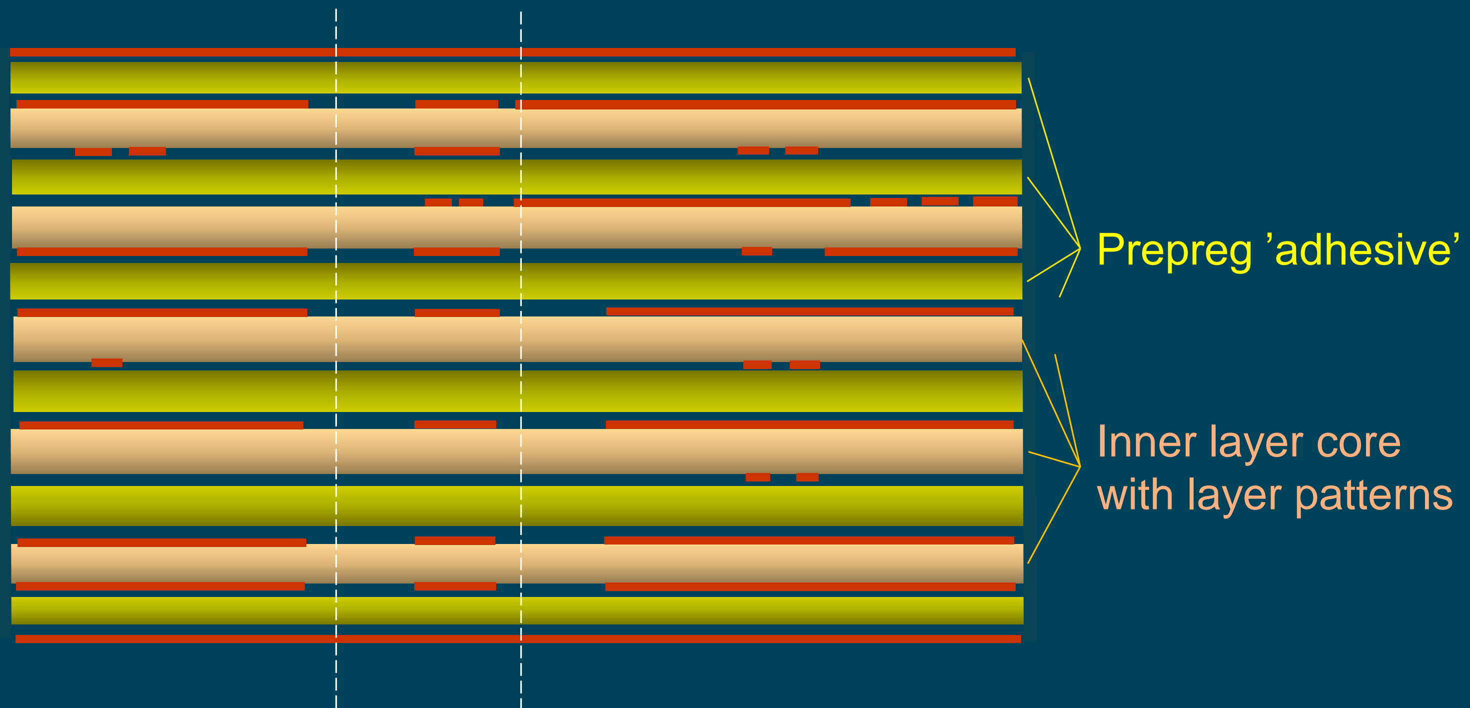
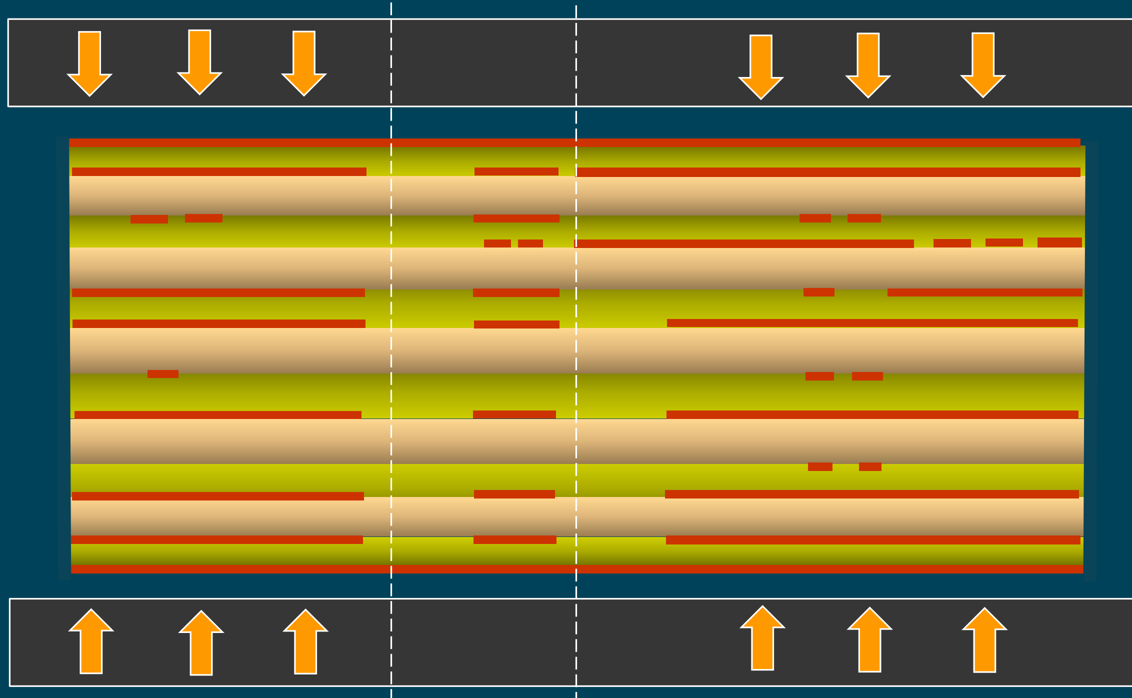
Multilayer Lay-up



Multilayer Press

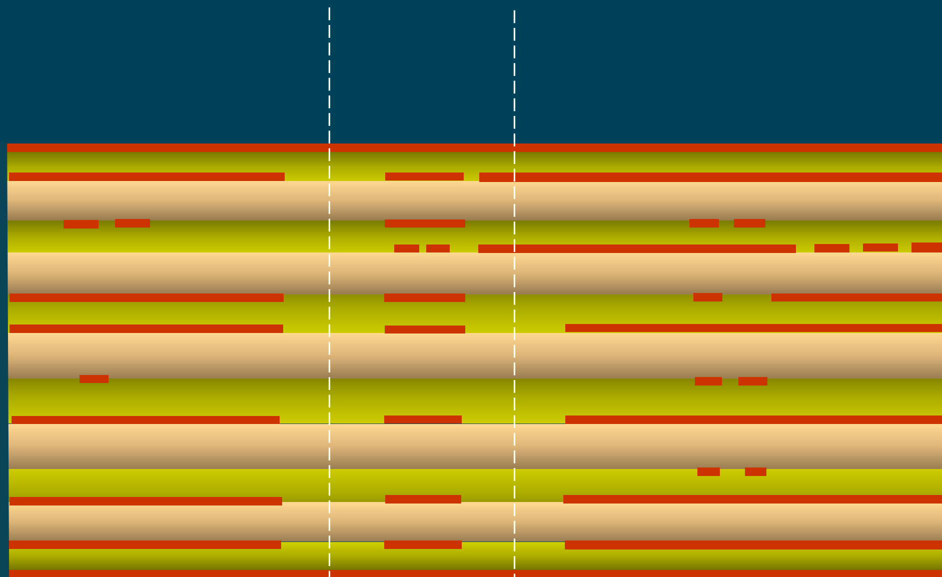


Epoxy in prepreg will polymerize under pressure and high temperature

At the same time the entire stackup will shrink horizontally

Planned drill hole centerlines

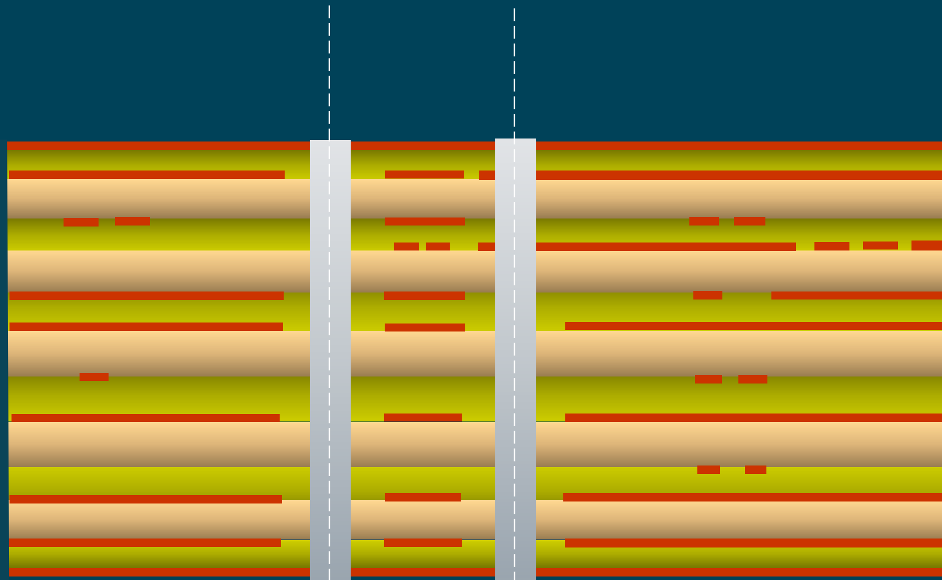
Drilling



Shrinkage correctly compensated, ready to drill

Planned drill hole centerlines

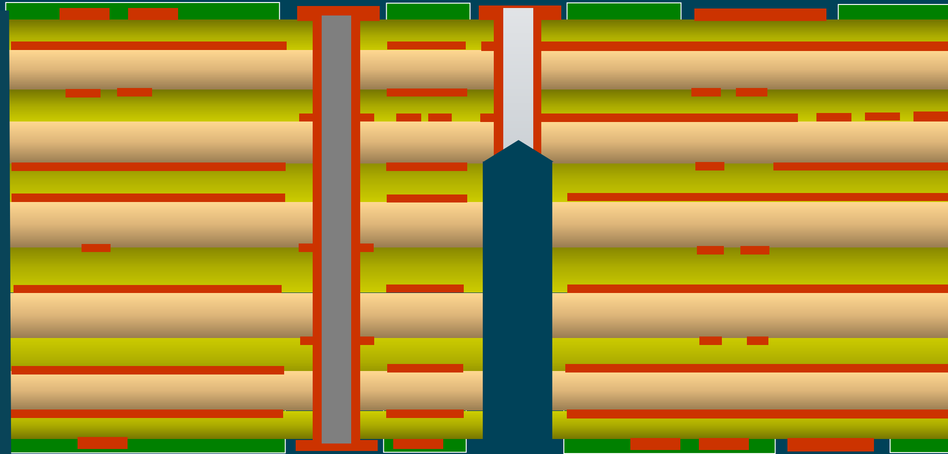
Drilling



Now we can drill safely, hitting the pad stack , maintaining PTH to Cu

Planned drill hole centerlines

PCB Ready

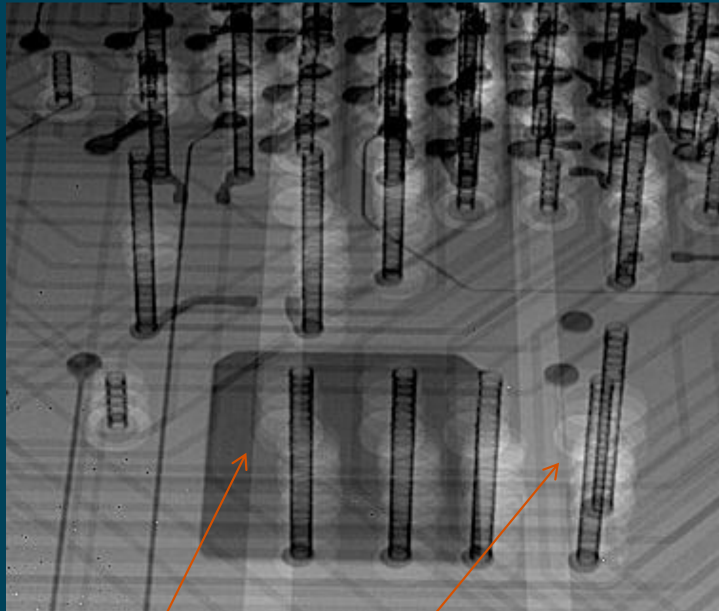


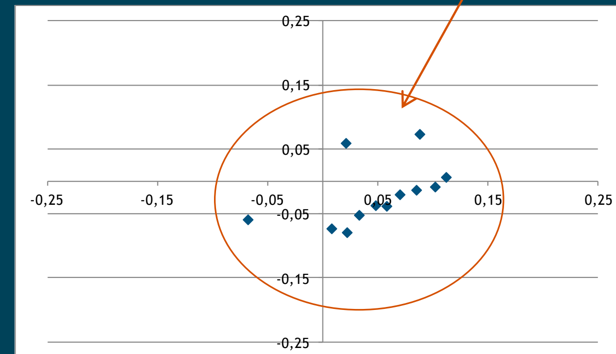
PCB can be finalized

Epoxy fill overplate via

Backdrilled via

View Before Optimizing



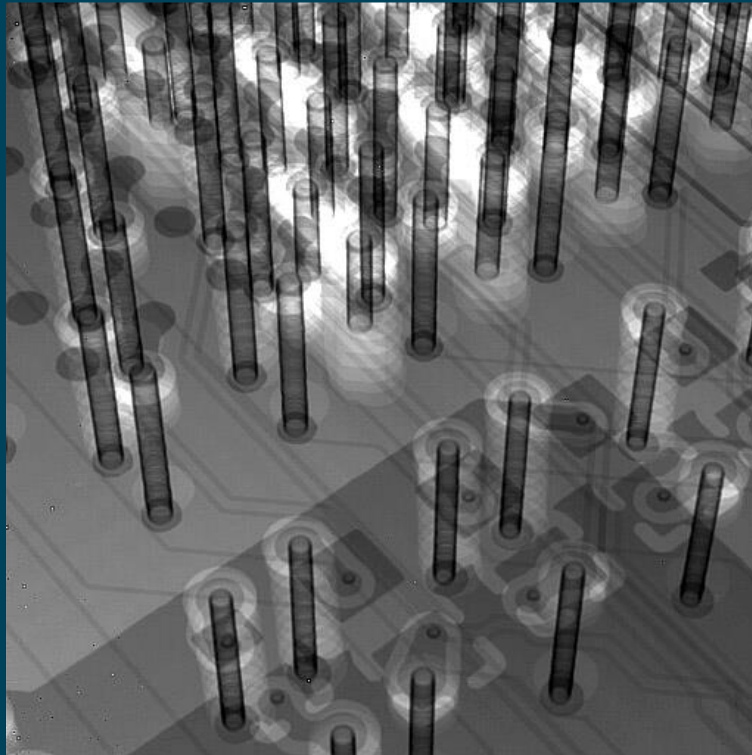


True layer average positions within +/- 120u (5mils)

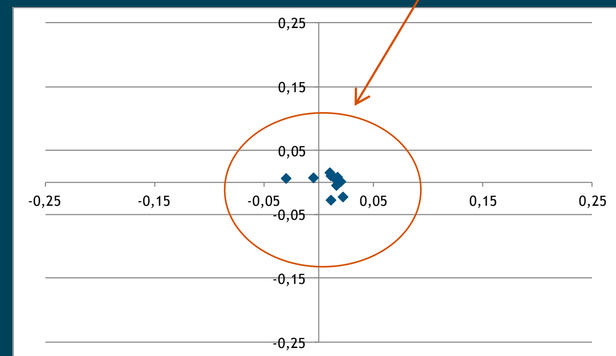
Short circuit risk due to layer misalignment

Batch will fail without optimizing

View After Optimizing



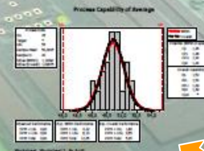
All true layer average positions within +/-40u (1,5mils)



Batch will be ok

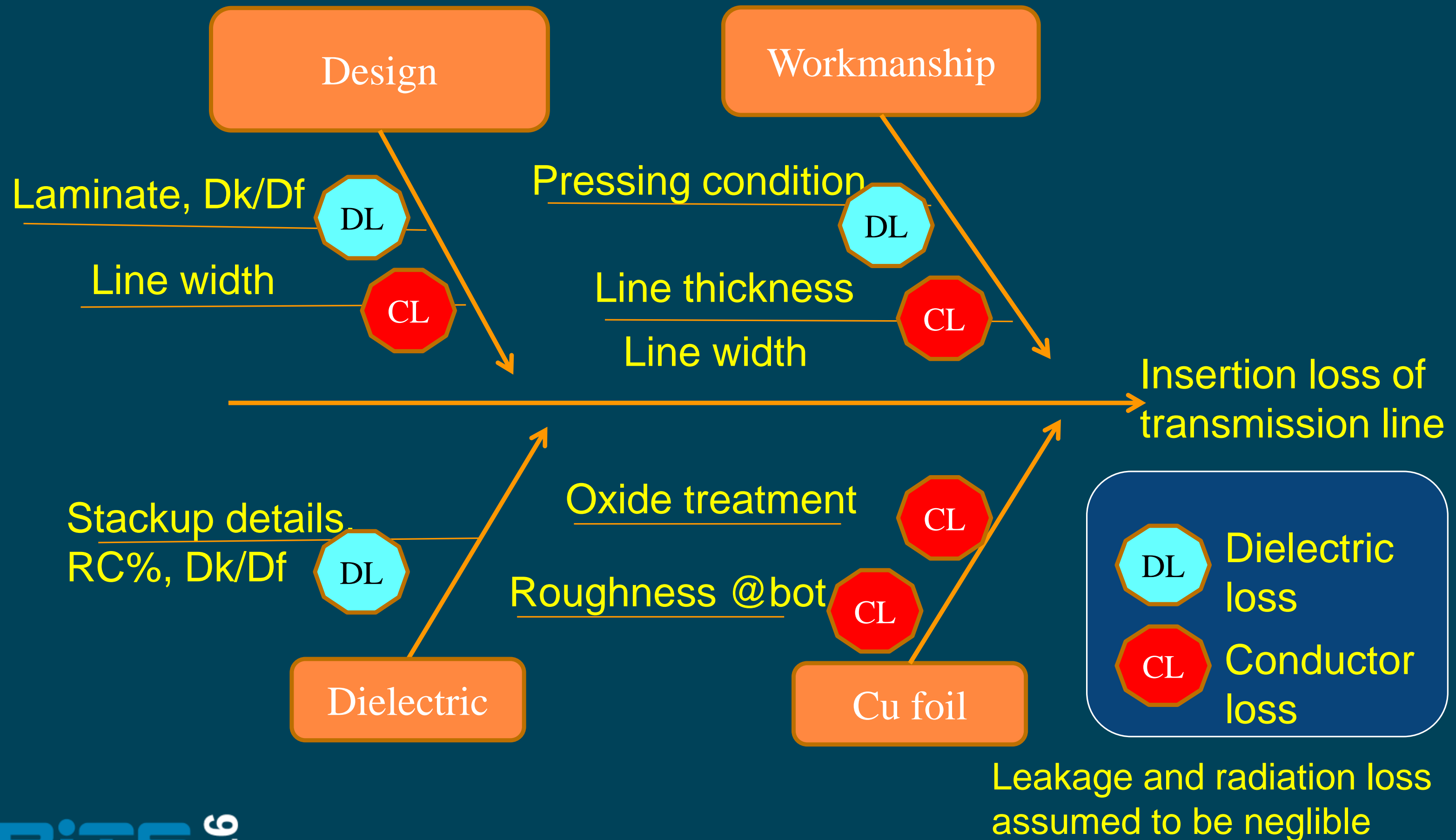
Impedance Control Preparation

Line type	Transmission line width	Typical Tolerance
SINGLE MICROSTRIP 50 ohm	90µm 150µm 300µm	+/-10% +/-8% +/-5%
SINGLE STRIPLINE 50 ohm	75µm * 90µm 150µm 300µm	+/-12% +/-10% +/-8% +/-5%
EMBEDDED DIFFERENTIAL 90-100 ohm	75µm * 90µm 100µm 150µm	+/-12% +/-10% +/-10% +/-7%



* Below 75µm trace for impedance control is not generally recommended, please contact Aspocomp
Normally tolerances are case sensitive, tighter tolerances may be achieved depending on case, ple
contact Aspocomp

Designer takes care of robust dimensions and PCB company takes care of the best possible tolerances


Simplified Insertion Loss Fishbone
Design
Workmanship
Laminate, Dk/Df
DL
Line width
CL
Pressing condition
DL
Line thickness
CL
Line width
Insertion loss of transmission line
Stackup details, RC%, Dk/Df
DL
Dielectric
Oxide treatment
CL
Roughness @bot
CL
Cu foil
DL
Dielectric loss
CL
Conductor loss
Leakage and radiation loss assumed to be neglible
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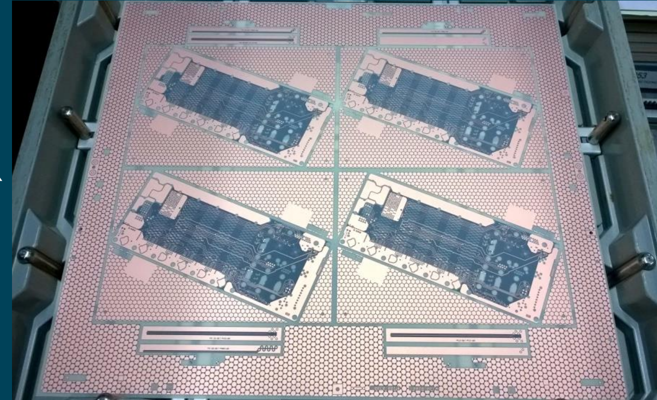
2016

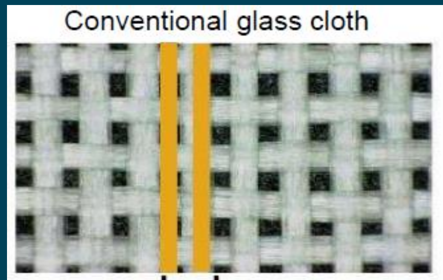
Insertion Loss Consideration

- Designer's task
  - Laminate material choice
  - Applicable track width
  - Copper foil type selection together with PCB supplier
  - Insertion loss simulation
- PCB manufacturer's task
  - Support the material choice and copper foil selection
  - Detailed stack-up support, impedance/trace dimensions
  - Possibly insertion loss simulation
  - Good workmanship
- Project management need to connect designer and the PCB shop

Additional Signal Integrity Matters

- Stub elimination → Back-drill
- Glass weave effect elimination
  - Tilted PCB in panel, can be bad MUR
  - Flat Glass





Optimized cost

No quality impacts

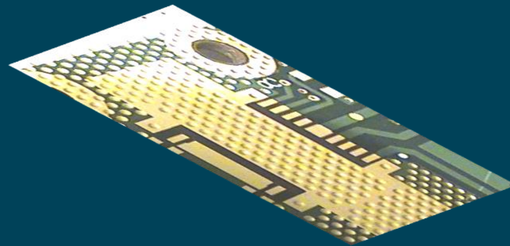
Higher cost

Improved RF performance

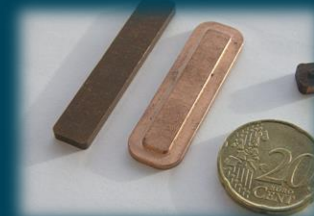
PCB Level Cooling

- Heat management is important when designing IC test equipment electronics
- Higher operating temperature may influence the electrical properties of the PCB
- Possibilities for PCB cooling:

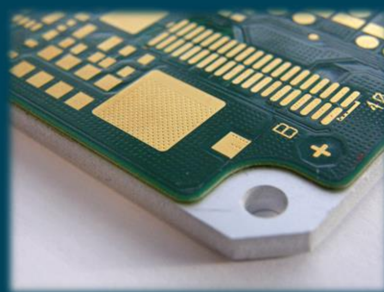
Thermal Viafarm



Embedded Cu Coin



Metalback PCB



Co-operation Approach

Stack-up , impedance, loss, design rules

PCB panel size MUR, ..

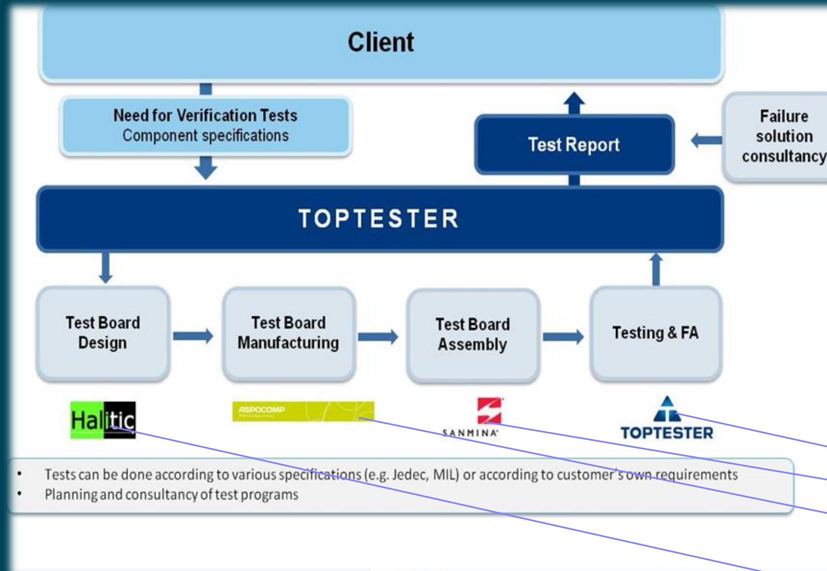
Customer feedback
DFM feedback

PCB Project Launch → PCB Layout → PCB Mfg → Assembly + testing → Follow-up

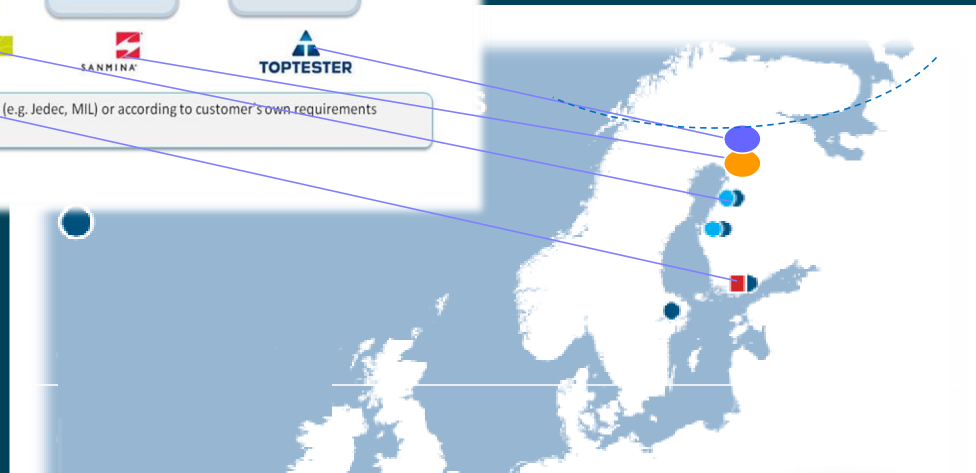
PCB technology test run if necessary

Raw-materials call-in
Key parameters
Impedance verification

Co-Operation Example @ Arctic Circle



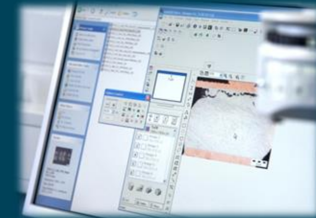
For reliability test boards



Reliability Test PCBs of JEDEC Style

- Examples of the key requirements for these PCBs:
  - High reliability, the purpose is to test components, not the PCB
  - Mechanical robustness
  - Connectivity → High local packaging density

10 000 g drop



With courtesy of

Conclusion

- Co-operate with your PCB partner in early stage
- Agree about commercial issues in advance
- Take care of the PCB details
- Follow-up with your PCB supplier