BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 8:30 am

Opening Remarks

Ira Feldman

General Chair,

BiTS Workshop

With Thanks to Our Sponsors!

Premier
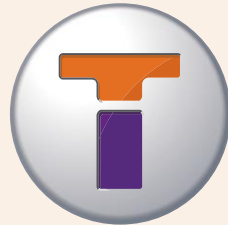
TwinSolution

Honored

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QUALITY INTERCONNECTION EXPERTS

From Sensata Technologies

Emeritus

tts

innovate . collaborate . deliver

TSE

Distinguished

R&D Altanova®

FELDMAN ENGINEERING

Networking

Innovative Circuits Engineering, INC

BiTS 2016
Burn-in & Test Strategies Workshop

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With Thanks to Our Sponsors!

Thumb drives & Lanyards

Notebooks

Keycards

Publication Sponsor

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… and Industry Partners

BiTS Workshop Committee

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Feldman Engineering Corp.

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Debbora Ahlgren, Chair
Feldman Engineering Corp.

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BiTS EXPO
Owen Prillaman, Chair
TechConnect Sales and Distribution Inc.

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BiTS Workshop Committee

Program

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Intel

Ila Pal, Co-Chair
Ironwood Electronics

Rafiq Hussain
Consultant

Mike Ramsey
Plastronics

Morten Jensen
Intel

Jeff Roehr
Texas Instruments

Marc Moessinger
Advantest

Fredrick Taber
General Chair Emeritus
Taber Consulting

Jason Mroczkowski
Xcerra Corp

Valts Treibergs
Multitest – Xcerra Corp.

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BiTS Overview

17th Annual

Welcome to the BiTS Workshop!

- **B**urn-**i**n and **T**est **S**trategies Workshop
  – A scope that incorporates next-generation solutions to test and burn-in challenges while also providing vital, current information on traditional technologies

What's NOW & NEXT in Test and Burn-in of Packaged ICs

- The World's Premier Forum For The Latest Information About Test & Burn-in of Packaged IC's

- Extensive & Diverse Technical Program

- The Latest Products & Services at BiTS EXPO

- Many Networking Opportunities

Feedback & Suggestions are Encouraged

Informal and Casual Throughout All Sessions & Activities

BiTS 2016
Burn-in & Test Strategies Workshop

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Core Values

What's *Now & Next* in Burn-in and Test

Premier Event ◆ Cutting Edge ◆ Staying Ahead

Learn...   Technical Program

...Explore...S   BiTS EXPO – 47 Exhibitors

...Share   Networking Opportunities

Learn …

Podium Sessions

- 8 Sessions Across 3 Days; 30 Practical & Useful Presentations

Poster Session

- 4 Posters

Renowned Speakers

- Keynote Address

- Distinguished Speaker

Market Reports

- Information about the Test & Socket Markets

BiTS Tutorial

- Learn From An Industry Expert & Build Your Leading Edge Skills

… Explore …

BiTS EXPO

- 47 Companies Are Exhibiting
- Exhibits Area is Open
  - Monday 6:00 – 9:00 pm
  - Tuesday 3:30 – 6:30 pm

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... Share

Meet and Chat With Someone You Don't Know!

- Many Opportunities to Network, Share & Discuss Ideas
    - 3 Breakfasts, 2 Lunches, 3 Receptions, 3 Dinners
- Morning and Afternoon Breaks
    - Poster Session During Monday Afternoon
- "The Sporty BiTS Bar & Grill" Social Event
    - Excellent food and drink
    - Enjoy the table games & fun

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Trip Report

Burn-in & Test Strategies Workshop   www.bitsworkshop.org   March 6-9, 2016

High Technology – MagLev Train

[267 MPH]

INAUGURAL

BiTS

Workshop 上海 Shanghai

™

October 21, 2015

© 2015 BiTS Workshop – Image: Zhu Difeng/Dollar Photo Club

BiTS Shanghai 2015 Recap

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Ira Feldman
BiTS General Chair

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Keynote Address by Ed Pausa (PwC)
"China's Impact on the Semiconductor Industry

– 2015 Update"

Jose Moreira
Advantest

Valts Treibergs
Xcerra

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John West
VLSI Research

Session 1

Yuanjun Shi
Session Chair

BiTS Shanghai

The Best of BiTS 2015

"PCB Test Fixture and DUT Socket Challenges for 32 Gbps/GBaud ATE Applications "

Jose Moreira - Advantest

-15 minute break-
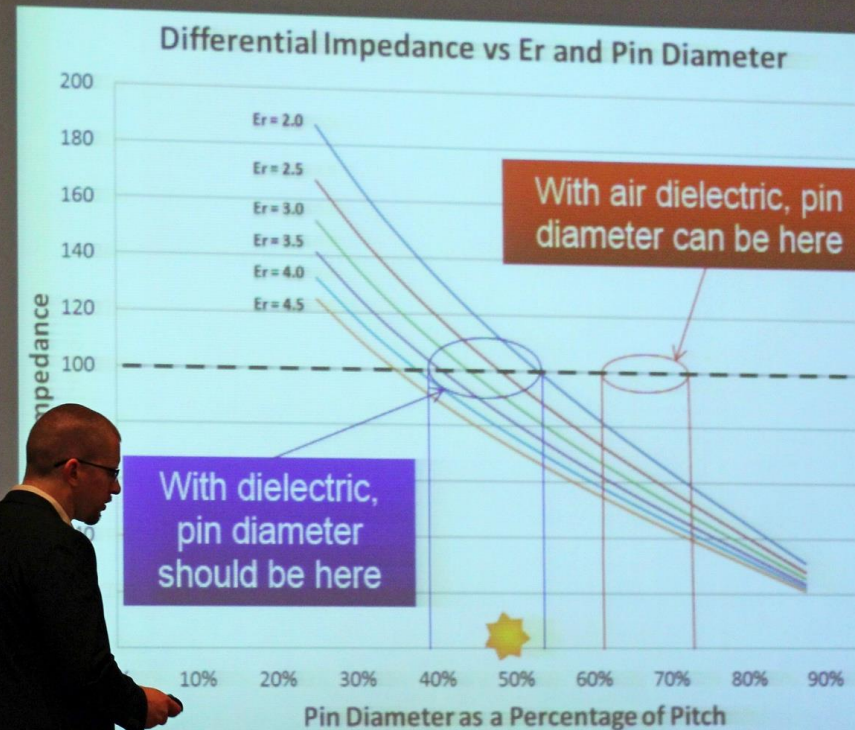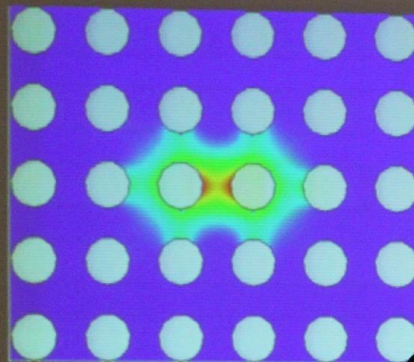
"Designing Sockets for Ludicrous Speed (80 GHz)"

Don Thompson - R&D Altanova

"Comparison of Different Methods in Determining Current Carrying Capacity of Semiconductor Test Contacts"

Valts Treibergs - Xcerra Corporation

**"The Economics of Semiconductor Test – Challenges and Opportunities for 2016"**

John West - VLSI Research Europe

Clark Liu
PowerTech Technology

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Colin Koh
Test Tooling Solutions Group

13

Jiachun (Frank) Zhou
Smiths Connectors

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Yuanjun Shi
TwinSolution Technology

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Session 2

Frank Zhou
Session Chair

BiTS Shanghai

East Meets West

"WLP Probing Technology Opportunity and Challenge"

Clark Liu - PowerTech Technology Inc.

"Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket"

Colin Koh - Test Tooling Solutions Group

"Signal Integrity & Inpacts by Connector Structures"

Jiachun (Frank) Zhou - Smiths Connectors

"LPDDR4 Signal & Power Performance Optimization By Hardware"

Yuanjun Shi - TwinSolution Technology

Best Presentation

BiTS Shanghai EXPO

Tomson Ballroom

Registration

Elevators

Escalators
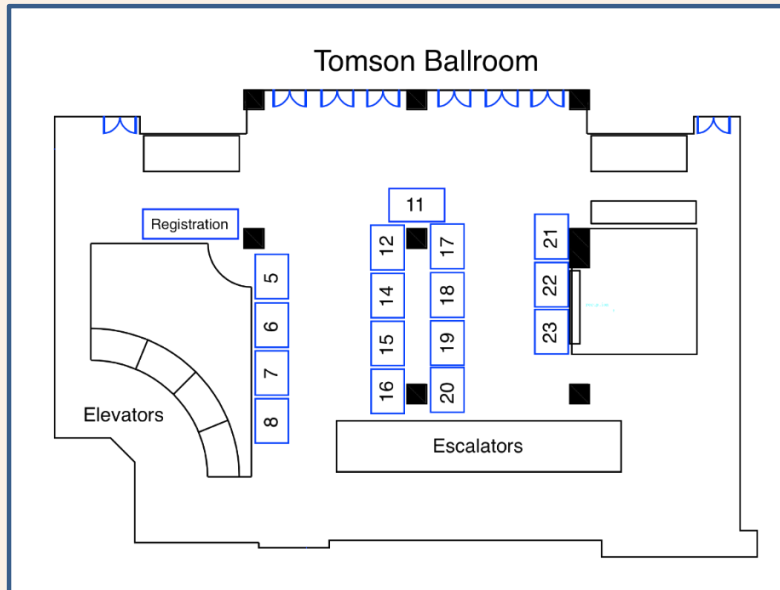
Exhibitor	Booth
Aehr Test Systems	23
Chip Shine Electronics	18
Giga Force Electronics	6
ISC Co.	14
IWIN Co.	8
JDT Technology	21
Leeno Industrial	17
MIS Technologies	7
Nitaku Electronics	16
Rika Denshi	12
Sensata Technologies	15
Test Tooling Solutions Group	11
TSE Co.	19
Twin Solution	5
WinWay Technology	22

Burn-in & Test Strategies Workshop   www.bitsworkshop.org   October 21, 2015
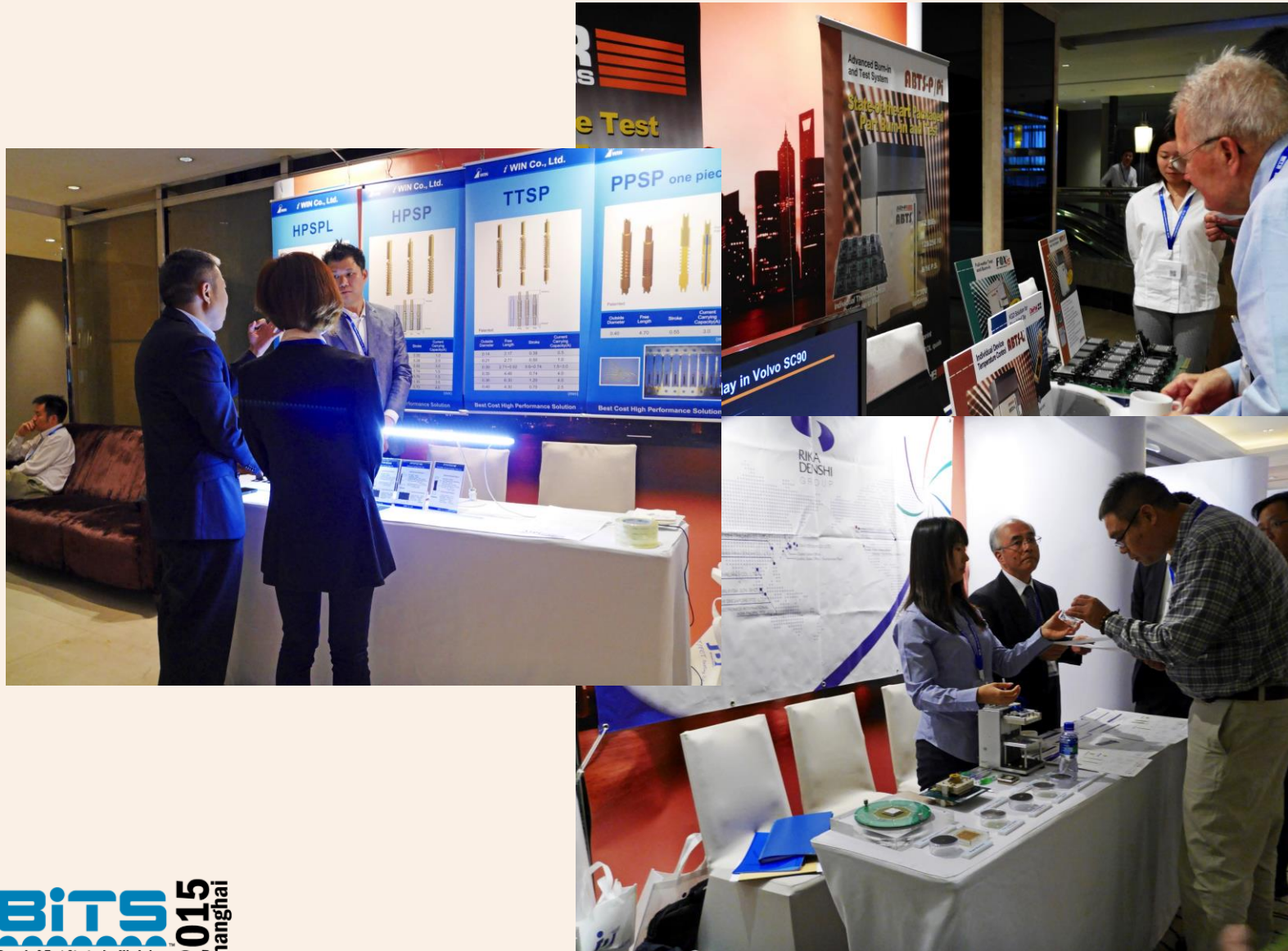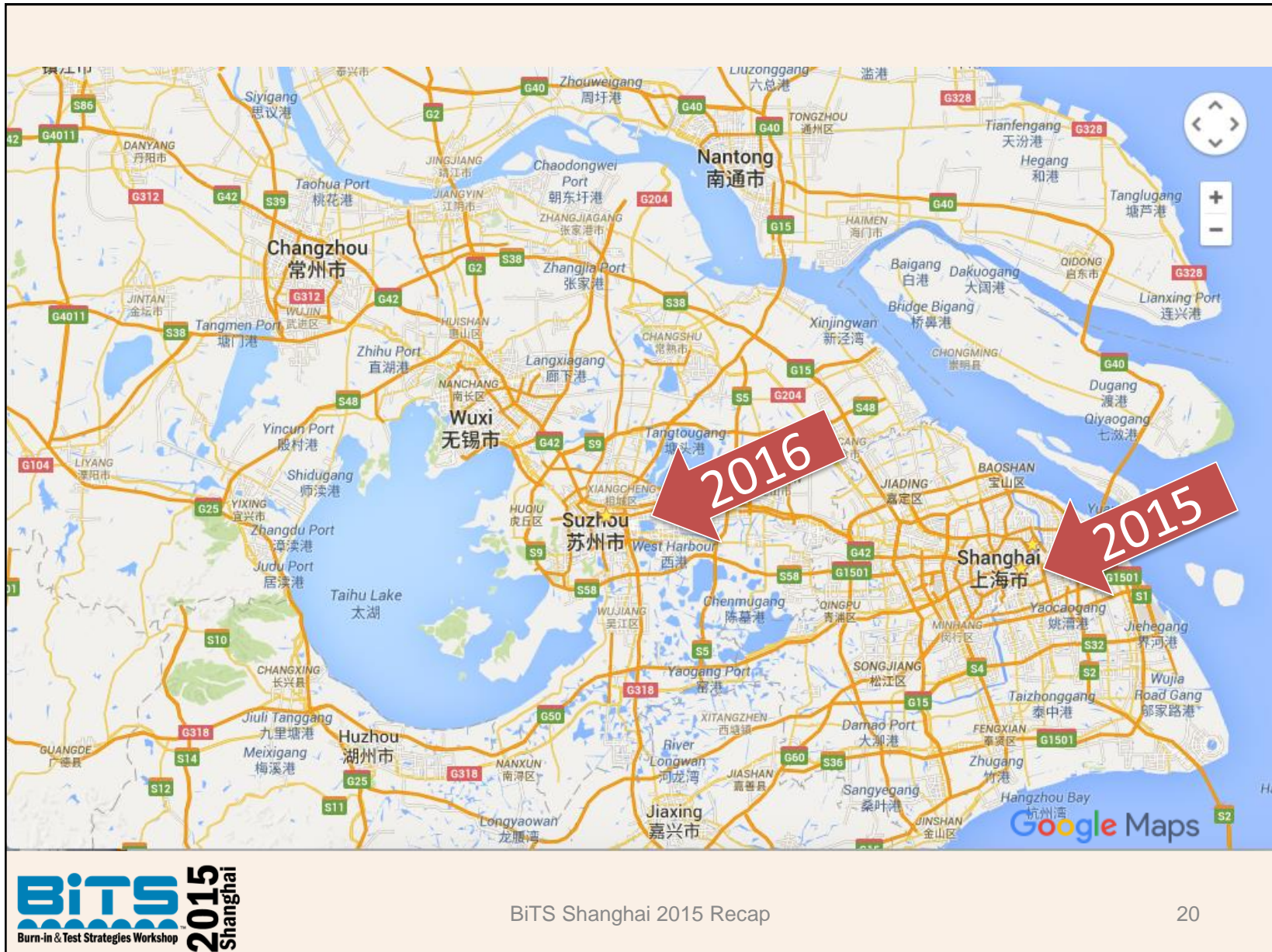
BiTS China
September 13, 2016
Suzhou China

Burn-in & Test Strategies Workshop   www.bitsworkshop.org   October 21, 2015

BiTS Workshop 2016 Schedule

Tutorial Day

Sunday March 6, 2016

Noon	Tutorial – **Adaptive Test, Outlier Analysis, and Burn-In reduction/elimination tutorial** *Jeffrey Roehr -Texas Instruments*	Pueblo Ballroom
6:30 pm	Welcome Reception	Kiva Foyer & Patio
7:30 pm	**Dinner**	Kiva Ballroom
8:30 pm	Distinguished Speaker – **Recovery from the Downturn; Technologies That Will Drive Semiconductor Business for the Coming Years** *Risto Puhakka - VLSIresearch*	Kiva Ballroom
9:30 pm	Adjourn	

Tutorial – Abstract

Jeffrey Roehr

This tutorial is designed to give attendees useful and practical information on the theory and statistics that support the application and use of Adaptive Test (AT) and Outlier Analysis (OA) in the production of modern semiconductor devices. In addition to providing information on the technical background behind these methods, the tutorial will include discussion of papers and case studies of real world applications of these techniques, emphasizing Burn-In elimination or reduction in production testing.

The goal of the tutorial is to provide attendees with the information and knowledge that they need to understand how (and when) AT & OA strategies are effective, the risk/reward relation implicit in these methods, the basic constraints and limitations of their use, and to walk away with the ability to implement fundamental techniques on their own. Sources of the material for this tutorial include personal experience, as well as extracts and references to papers and reports published by Universities and companies such as IBM, INTEL, Analog Devices, LSI Logic, AMD, NXP, and Texas Instruments. Resource links to a variety of technical papers, authors, and 3rd party software vendors will also be provided as part of the tutorial materials.

The tutorial will be led by Jeffrey Roehr who is a Senior Member of the Technical Staff at Texas Instruments, a 35 year veteran of product and test engineering, and a Senior Member of the IEEE.

Distinguished Speaker – Abstract

Risto Puhakka

The semiconductor markets have been going through downturn in recent quarters. At the time of this speech, the recovery is around the corner if not already underway. Is semiconductor industry ready to exploit new technologies to drive the next cycle? What will be China's role this time? What is required from test? We will have numerous opportunities, technologies and devices that will drive the business for years to come. The presentation will explore and define these opportunities.

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7, 2016

8:30 am	Opening Remarks – *Ira Feldman – BiTS Workshop General Chair*	Kiva Ballroom
9:00 am	Keynote Address – **Chip Overtest - Are Ics Tested Too Much?** Dale Ohmart -Texas Instruments	Kiva Ballroom
10:00 am	Break & Networking	Kiva Foyer & Patio
10:30 am	Session 1 – **Marketplace Report & Thing One, Thing Two, and Test Them We Do** *Internet of Things*	Kiva Ballroom
12:30 pm	Lunch	Kiva Foyer & Patio

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7, 2016

1:30 pm	Session 2 – **Material Matters** *Advanced Materials & Manufacturing*	Kiva Ballroom
3:30 pm	Poster Session	Kiva Ballroom
4:30 pm	Session 3 – **Stimulating Simulating** *Simulation*	Kiva Ballroom
6:00 pm	**BiTS EXPO & Reception**	Atrium
9:00 pm	Adjourn	

BiTS Awards

- Best Presentation

- Best Poster

- Best Data Presented

- Most Inspirational Presentation

- Best Presentation, Tutorial in Nature

- Attendee Choice

  … and …

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BiTS "Special" Award

For the Least Concealed Sales Pitch

(Almost)

Brilliant

Disguise

"Semi-retired" but always available…

BiTS EXPO

to Kiva Ballroom and BiTS Registration
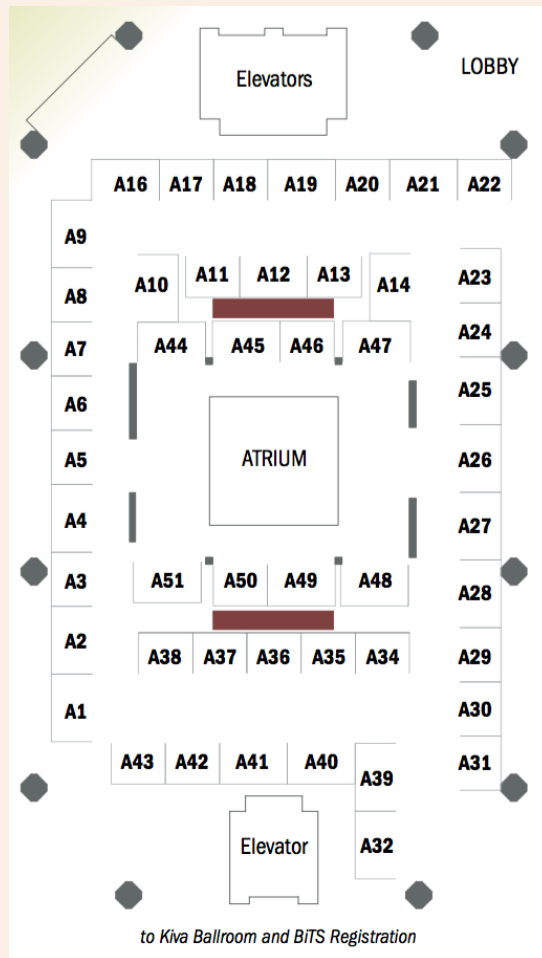
Company	Booth
Aehr Test Systems	A28
Aries Electronics, Inc.	A25
Astronics Test Systems	A19
CCT Plastics	A24
Chip Shine, Inc.	A38
CMR Summit	A9
Cohu	A3
DuPont Vespel	A36
E-TEC Interconnect AG	A6
E. Jordan Brookes	A30
ELES Semiconductor	A7
Enplas Tech Solutions, Inc.	A44
Ensinger Inc.	A50
EXATRON	A13
HSIO Technologies	A14
Incal Technology, Inc.	A26
INNO Global	A16
Integrated Test Corp	A37
intest Corporation	A32
ISC Co., Ltd.	A43
IWIN Co., Ltd.	A11
J2M Test Solutions	A4
Johnstech International	A10
Kita USA, Inc.	A18
LEENO	A21
Materion Performance	A49
MCS	A8
Micro Control Company	A5
MJC Electronics Corp.	A39
Modus Test, LLC	A41, A42
Phoenix Test Arrays	A46
Plastronics	A48
Qualmax, Inc.	A51
R&D Altanova	A1
Rika Denshi America, Inc.	A23
Semiconductor Test	A22
Sensata Technologies	A34, A35
Smiths Connectors	A40
Sun Electric Heater	A2
SV TCL-An SV Probe	A20
Test Spectrum	A29
Test Tooling Solutions	A45
TSE	A12
Twin Solution Technologies	A27
WinWay Technology	A17
Xcerra	A31
Yamaichi Electronics USA, Inc.	A47

BiTS Social Event

"The Sporty BiTS Bar & Grill"

Tuesday 6:30 – 9:30 pm
Kiva Foyer and Patio

Canstock/sCukrov

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Schedule At A Glance

THE COMPLETE BiTS SCHEDULE AT-A-GLANCE

SUNDAY March 6	MONDAY March 7	TIME	TUESDAY March 8	WEDNESDAY March 9
	Continental Breakfast / Registration Desk Open	7 00	Continental Breakfast / Registration Desk Open	Continental Breakfast / Registration Desk Open
		7 30		
		8 00		
	Opening Remarks	8 30	SESSION 4 High Frequency	SESSION 7 Contact Technology
	KEYNOTE ADDRESS Dale Ohmart	9 00		
		9 30		
	Break & Networking	10 00	Break & Networking	Break & Networking
	SESSION 1 Marketplace & Internet of Things	10 30	SESSION 5 Advanced Technology/ New Approaches	SESSION 8 Test Cell Part 2
Registration Desk Open		11 00		
		11 30		
		12 00		Awards & Closing Remarks
	Lunch	12 30	Lunch	Adjourn Workshop
		1 00		
	SESSION 2 Advanced Materials & Manufacturing	1 30	SESSION 6 Test Cell Part1	VISIT the BiTS WEBSITE for PROGRAM DETAILS and DESCRIPTIONS.
TUTORIAL Adaptive Test, Outlier Analysis, and Burn-In Reduction/ Elimination Mr. Jeffrey Roehr		2 00		
		2 30		
		3 00		
	POSTER SESSION Break & Networking	3 30		
		4 00	EXPO2016	
	SESSION 3 Simulation	4 30		
		5 00		
		5 30		
		6 00		
	EXPO2016	6 30		
Welcome Reception		7 00	SOCIAL EVENT The Sporty BiTS Bar & Grill Food, Beverages, Games	
		7 30		
Dinner		8 00		
		8 30		
DISTINGUISHED SPEAKER Mr. Risto Puhakka		9 00		
Adjourn for the day	Adjourn for the day	9 30	Adjourn for the day	

BiTS 2016   Burn-in & Test Strategies Workshop

bitsworkshop.org

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bitsworkshop.org

Your Complete Source For Information About BiTS

Current Workshop

- Call For Papers
- EXPO & Sponsorships
- Advance/Final Program
- Registration Information & Forms; Register On-line
- Author Information
- Hotel Information/Travel

Features

- Committee Members
- Contact BiTS - Add to Mailing List & Inquiries
- Links to Other Websites
- 'Press' About BiTS
- Archive of past BiTS
- Search BiTS Feature

Plus Premium Archive...

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BiTS Premium Archive

- Multimedia
  - Audio with synchronized slides & pointer
  - BiTS 2014 & BiTS 2015 & BiTS Shanghai 2015
  - BiTS 2016 posted shortly after BiTS

- Additional content
  - Tutorials

- Subscription Model
  - BiTS 2016 Professional Attendees – Subscription for One Year
  - Subscriber – Nominal Fee
    - Applied to BiTS 2017 Registration

bitsworkshop.org/premium

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BiTS 2017

March 5 – 8 , 2017

Hilton Phoenix / Mesa Hotel

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Keynote
Address

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 9:00 am

Chip Overtest

Are ICs Tested too Much?

Dale Ohmart

Texas Instruments

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7, 2016

Time	Session	Location
8:30 am	Opening Remarks – *Ira Feldman – BiTS Workshop General Chair*	Kiva Ballroom
9:00 am	Keynote Address – **Chip Overtest - Are Ics Tested Too Much?** Dale Ohmart -Texas Instruments	Kiva Ballroom
10:00 am	Break & Networking	Kiva Foyer & Patio
10:30 am	Session 1 – **Marketplace Report & Thing One, Thing Two, and Test Them We Do** *Internet of Things*	Kiva Ballroom
12:30 pm	Lunch	Kiva Foyer & Patio

Session 1

Ila Pal
Session Chair

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 10:30 am

Marketplace Report & Thing One, Thing Two, and Test Them We Do

"Marketplace Report"

Ira Feldman & Debbora Ahlgren - Feldman Engineering Corp.

"How Internet Of Things Will Change Back End Processing"

Mike Frazier & Laurie Wright - Xcerra Corporation

"Serialized Programming Solutions for IoT Secure Elements"

Robert Howell - Exatron

"Internet of Things Testing Challenges"

Anthony Lum - Advantest

BiTS 2016
Burn-in & Test Strategies Workshop

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7, 2016

1:30 pm	Session 2 – **Material Matters** *Advanced Materials & Manufacturing*	Kiva Ballroom
3:30 pm	Poster Session	Kiva Ballroom
4:30 pm	Session 3 – **Stimulating Simulating** *Simulation*	Kiva Ballroom
6:00 pm	**BiTS EXPO & Reception**	Atrium
9:00 pm	Adjourn	

Session 2

Ashok Kabadi
Session Chair

Frontiers Day

Monday March 7 - 1:30 pm

Material Matters

"Long Life Probe Pin by Electroforming Process"
Makota Kondo & Hirotada Teranishi - Omron Corporation
Takahiro Sakai & Naoyuki Kimura - Omron Corporation

"Carbon Nanotube Polymer Composites as High Performance Thermal Interface Materials for Burn in and Test Applications"
Leonardo Prinzi - Georgia Institute of Technology
Craig Green & Baratunde Cola - Carbice Nanotechnologies, Inc.

"Requirements and Solutions for Test PCBs"
Markku   Jamsa - Aspocomp Group Oyj

"PCB Test Fixture and Socket Challenges for mmWave Applications"
Don Thompson Jose - R&D Altanova
Jose Moreira - Advantest Europe GmbH
Giovanni Bianchi - Advantest

Poster **S**ession

Frontiers Day

Monday March 7 - 3:30 pm

Poster Session

"WiGig Test"

Bert Brost – Xcerra

"Re-balling BGA with Gold Plated Copper Spheres, the Need and the SMT Challenges"

Emad Al-Momani, Srikanth Mothukuri, Jack Mumbo - Intel Corporation

"Thermal Test Methodology for Validating Automotive Semiconductor Packages"

Ying Feng Pang, Amy Xia – Intel Corporation

"Insitu 256 Node Resistive Leakage Tester"

Gordon Cowan, Rich Zavala - HighRel, Inc.

BiTS 2016
Burn-in & Test Strategies Workshop

Session 3

Morten Jensen
Session Chair

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 4:30 pm

Stimulating Simulating

"Optimizing the PCB-to-socket-to-DUT interface"

Gert Hohenwarter - GateWave Northern, Inc.

"Characterize Only the High Speed Interconnect Performance"

Carol McCuen - R&D Altanova

"Modelling, Materials, and Madness"

Mike Gedeon - Materion

Session 4

Marc Mössinger
Session Chair

BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 8 - 8:00 am

Frequently High

"High Speed BGA Sockets from a System Perspective"

Don Thompson - R&D Altanova

"A Solution of Test, Inspection and Evaluation for Blind Signal Waveform on a Board"

Tatsumi Watabe, Makoto Kawamura, Hiroyuki Yamakoshi - S.E.R. Corporation

"Device Packaging and How It Affects RF Performance"

Noureen Sajid, Jeff Sherry - Johnstech International

"Automotive Radar Test"

Jason Mroczkowski - Xcerra Corporation

Session 5

Ashok Kabadi
Session Chair

BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 8 - 10:30 am

West Meets East & Cutting Edge

"LPDDR4 Signal & Power Performance Optimization By Hardware"
"通过测试硬件的优化来提升LPDDR4信号和电源的性能"
Yuanjun Shi - Twinsolution Technology
Xiao Yao - HiSilicon Technologies Co

"Reliability Characterization of Unpackaged (bare) die for Silicon Photonics module"
Sujata Paul, Andrew Fong, Samir Alqadhy, Huy Nguyen, Zoe Conroy - Cisco
Tom Elliot, Jag Jassal - Evans Analytical Group

"Advanced High Energy CO2 Spray Cleaning Technology for Burn-In Test Substrate Cleaning Applications"
Nelson Sorbo - Cool Clean Technologies

"Texas Instruments Final Test Contactor Qualification Process and Low Profile Contactor Solution"
James Tong, Hisashi Ata - Texas Instruments

Session 6

Jason Mroczkowski
Session Chair

Performance Day

Tuesday March 8 - 1:30 pm

Cell-ebrating Test

"Vision Assist Method for Common Change Kit"

Brad Emberger, Zain Abadin – Advantest

"Test Cell Thermal Solution"

Gianluca Lombardi - Advantest

"Testing Magnetic Sensors"

Paul Ruo - Aries Electronics, Inc.

Larre Nelson - Kita USA

"Magnetically shielded test-cell for an integrated fluxgate sensor"

Gert Haensel - Texas Instruments

Loren Hillukka - Johnstech International Ltd.

Session **7**

Mike Ramsey
Session Chair

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 9 - 8:00 am

Very Touching

"Implementation of MEMS Particles Dramatically Improves Conventional Rubber Sockets"

Dave OH, Justin Yun, Kanghee Kim - TSE Co., Ltd.

"Contacting DC - 40GHz and beyond"

Tony Tiengtum - Xcerra Corporation

"Small Form Factor Sockets and Circuits for Silicon and Platform Validation"

James Rathburn - HSIO Technologies, LLC

"Prediction of Contact Mark for QFN package"

Yuanjun Shi - Twin Solution

BiTS
Burn-in & Test Strategies Workshop
2016

Session **8**

Jason Mroczkowski
Session Chair

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 9 - 10:30 am

Cell-ebrating Test Too

"Modeling Socket Thermal Performance Inside a Burn-In Chamber"
Jason Cullen – Plastronics
Rob Caldwell - Delta V Instruments

"Established the first WLCSP Testing at Tri-temp for RF and Non-RF Products"
Edwin Valderama & Jin Sheng Tan -Intel Technologies

"A Silicon Photonics Wafer Probing Test Cell"
Roberto Aranzulla, Daniele Sala, Roberto Barbon - ST Microelectronics
Giuseppe Astone, Maurizio Rigamonti, Massimo Galli - ST Microelectronics
Jean Luc Jeanneau, Dario Adorni, Paul Mooney - Tokyo Electron
Hubert Werkmann, Fabio Pizza - Advantest Europe GmbH
Jose Moreira, Zhan Zhang - Advantest

Awards &
Closing

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 18 Noon

Awards & Closing Remarks

Ira Feldman

General Chair,

BiTS Workshop

Call for BiTS 2017

March 5-8, 2017 ◆ Mesa, Arizona

Presentations ◆ Posters ◆ Tutorial	BiTS EXPO 2017 & Sponsors

Share your latest work and advancements as an **AUTHOR**! Your presentation or poster will be part of a stimulating and comprehensive program. Explore a demanding topic as a **TUTORIAL INSTRUCTOR**. Share your expertise with participants eager to build their leading edge skills. Presentation, Poster & Tutorial proposals addressing a broad range of burn-in and test subjects are welcome, including, but not limited to:

- Socketing/Contacting of Contemporary and Advanced Packaging Technologies
- PCBs, Materials, Handlers, Contact
- Technologies, Burn-in Tooling
- Modeling, Characterization & Analysis
- Process & Operational Challenges
- WLCSP Test for KGD or Final Test
- MEMS and Non-Electrical Stimuli Test

The EVENT for exhibiting your company's products & services. Showcase and promote what is *Now & Next!*

Don't miss out! See the registration desk to sign up now at the early-bird discount rate. **BiTS EXPO** is sure to sell out!

For more information about BiTS 2017 please contact the BITS Office
bitsinfo@bitsworkshop.org

Have the **LAST WORD!**
Tell us what you liked and what you disliked:

bitsworkshop.org/feedback

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BiTS Workshop 2016 Schedule

Performance Day

Tuesday March 17, 2015

8:00 am	Session 4 – **Frequently High** *High Frequency*	Kiva Ballroom
10:00 am	Break & Networking	Kiva Foyer & Patio
10:30 am	Session 5 – **West Meets East & Cutting Edge** *Advanced Technology / New Approaches*	Kiva Ballroom
12:30 pm	Lunch	Kiva Foyer & Patio
1:30 pm	Session 6 – **Cell-ebrating Test** *Test Cell - 1 of 2*	Kiva Ballroom
3:30 pm	**BiTS EXPO**	Atrium
6:30 pm	"The Sporty BiTS Bar & Grill" Social Event	Kiva Foyer & Patio
9:30 pm	Adjourn	

BiTS Workshop 2016 Schedule

Solutions Day

Wednesday March 9, 2015

8:00 am	Session 7 – **Very Touching** *Contact Technology*	Kiva Ballroom
10:00 am	Break & Networking	Kiva Foyer & Patio
10:30 am	Session 8 – **Cell-ebrating Test Too** *Test Cell - 2 of 2*	Kiva Ballroom
12:00 pm	**Awards & Closing Remarks**	Kiva Ballroom
12:30 pm	Adjourn	

BiTS 2016
Burn-in & Test Strategies Workshop

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Technical Program

Title
Tutorial **Adaptive Test, Outlier Analysis, and Burn-In reduction/elimination tutorial** Jeffrey Roehr - Texas Instruments
Distinguished Speaker **Recovery from the Downturn; Technologies That Will Drive Semiconductor Business for the Coming Years** Risto Puhakka - VLSIresearch
Opening Remarks Ira Feldman, General Chair
Keynote Address **Chip Overtest Are ICs Tested Too Much?** Dale Ohmart - Texas Instruments
Closing & Awards Ira Feldman, General Chair

Session	Title
1	**Marketplace Report & Thing One, Thing Two, and Test Them We Do** *Internet of Things*
2	**Material Matters** *Advanced Materials & Manufacturing*
3	**Stimulating Simulating** *Simulation*
4	**Frequently High** *High Frequency*
5	**West Meets East & Cutting Edge** *Advanced Technology /New Approaches*
6	**Cell-ebrating Test** *Test Cell - 1 of 2*
7	**Very Touching** *Contact Technology*
8	**Cell-ebrating Test Too** *Test Cell - 2 of 2*
Poster	**Poster Session**

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BiTS Workshop 2016 Schedule

Tutorial

Tutorial Day

Sunday March 6 - Noon

Adaptive Test, Outlier Analysis, and Burn-In reduction/elimination tutorial

This tutorial is designed to give attendees useful and practical information on the theory and statistics that support the application and use of Adaptive Test (AT) and Outlier Analysis (OA) in the production of modern semiconductor devices.

Jeffrey Roehr

Senior Member of Technical Staff

Texas Instruments

BiTS 2016
Burn-in & Test Strategies Workshop

Tutorial – Biography

Jeffrey Roehr

Jeffrey Roehr has over 35 years of experience in Product and Test Engineering and Management for RCA, GTE, Analog Devices, Mediatek, and is now working for Texas Instruments in Houston.

For the past 15 years his focus has been on developing algorithms for adaptive testing, outlier elimination, and statistical testing on very high volume production products.

Mr. Roehr has presented many papers, tutorials, and invited talks at IEEE events. He is a Senior Member of the IEEE, a member of the IEEE DATA Workshop Steering Committee, a member of the ITRS Adaptive Test working group, and is the founder and chairman of the Texas Instruments Data Analysis Workshop (DAW).

Distinguished **S**peaker

BiTS Workshop 2016 Schedule

Tutorial Day

Sunday March 6 - 8:30 pm

Recovery from the Downturn; Technologies That Will Drive Semiconductor Business for the Coming Years

Risto Puhakka

President

VLSIresearch

Distinguished Speaker – Biography

Risto Puhakka

Risto Puhakka is President of VLSIresearch, leading the company's commercial operations and market research activities. He is an expert in Semiconductor Capital Equipment markets as well as Semiconductor Manufacturing. Risto advises managers, boards, and investors about semiconductor market trends and strategic industry statistics. He is a regularly invited speaker at conferences about various topics in semiconductor manufacturing and equipment markets.

Risto is a graduate of Helsinki University of Technology (MSc) and UC Berkeley, Haas School of Business (MBA). When Risto is not working he cherishes time with his family, runs very long distances, and is occasionally spotted flying model airplanes.

Keynote Address – Abstract

Dale Ohmart

We need to define test differently. It is easy to fall into the trap of considering test to mean "prove every part shipped is good", and then one step further to "test must verify all the specs of the part to ensure it's a good part". But this thinking leads to ever increasing test complexities and spiraling test costs. A better way to look at test is that the semiconductor manufacturing process builds defects and test is a sorting process to eliminate those defects from the shipped population. Test cost and test capital trends in the semiconductor industry will be examined with a discussion on how much test is affordable. What are the real-world limitations to test throughput? Are there "optimal" target values for test time and multisite count? What are the impacts of test on device yield? And how does the test process itself impact its own intrinsic yield? In addition to exploring these questions, do new requirements, such as non-electrical test and 3D assembly, also change these "answers"? Many thought provoking questions will be covered in this keynote, which will change how you think about test!

Keynote Address – Biography

Dale Ohmart

Dale Ohmart is currently a Distinguished Member of the Technical Staff at Texas Instruments, where he is focused on driving test manufacturing excellence throughout the company. He joined Texas Instruments after graduating from the University of Kansas in 1980 with his Bachelors of Science degree in Engineering Physics. He was awarded "Outstanding Senior in Physics and Astronomy" that same year and remains a proud "Kansas Jayhawk".

Throughout his career, Dale has contributed at Texas Instruments in a variety of positions from his first role as Product Engineer onwards. He was quickly promoted to Test Engineering Manager for the Microprocessors group in 1981 and has been involved in test within the organization ever since.

Dale has had many significant accomplishments during his tenure at Texas Instruments. He was instrumental in developing TI's current approach to managing test equipment productivity, he invented and holds the patent on TI's final test manufacturing process to ensure test quality, and he was the first to implement multisite testing on TI's high-pin-count digital signal processing (DSP) and micro-controller unit (MCU) products.