SEVENTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop™

March 6 - 9, 2016

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive - Keynote

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BiTS 2016 Burn-in & Test Strategies Workshop

Keynote Address

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 9:00 am

Chip Overtest
Are ICs Tested too Much?

Dale Ohmart

Texas Instruments

BiTS 2016 Burn-in & Test Strategies Workshop

Keynote Address – Abstract

Dale Ohmart

We need to define test differently. It is easy to fall into the trap of considering test to mean "prove every part shipped is good", and then one step further to "test must verify all the specs of the part to ensure it's a good part". But this thinking leads to ever increasing test complexities and spiraling test costs. A better way to look at test is that the semiconductor manufacturing process builds defects and test is a sorting process to eliminate those defects from the shipped population. Test cost and test capital trends in the semiconductor industry will be examined with a discussion on how much test is affordable. What are the real-world limitations to test throughput? Are there "optimal" target values for test time and multisite count? What are the impacts of test on device yield? And how does the test process itself impact its own intrinsic yield? In addition to exploring these questions, do new requirements, such as non-electrical test and 3D assembly, also change these "answers"? Many thought provoking questions will be covered in this keynote, which will change how you think about test!

BiTS 2016 Burn-in & Test Strategies Workshop

Keynote Address – Biography

Dale Ohmart

Dale Ohmart is currently a Distinguished Member of the Technical Staff at Texas Instruments, where he is focused on driving test manufacturing excellence throughout the company. He joined Texas Instruments after graduating from the University of Kansas in 1980 with his Bachelors of Science degree in Engineering Physics. He was awarded "Outstanding Senior in Physics and Astronomy" that same year and remains a proud "Kansas Jayhawk".

Throughout his career, Dale has contributed at Texas Instruments in a variety of positions from his first role as Product Engineer onwards. He was quickly promoted to Test Engineering Manager for the Microprocessors group in 1981 and has been involved in test within the organization ever since.

Dale has had many significant accomplishments during his tenure at Texas Instruments. He was instrumental in developing TI's current approach to managing test equipment productivity, he invented and holds the patent on TI's final test manufacturing process to ensure test quality, and he was the first to implement multisite testing on TI's high-pin-count digital signal processing (DSP) and micro-controller unit (MCU) products.

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Chip Overtest
Are ICs tested too much?

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Texas Instruments

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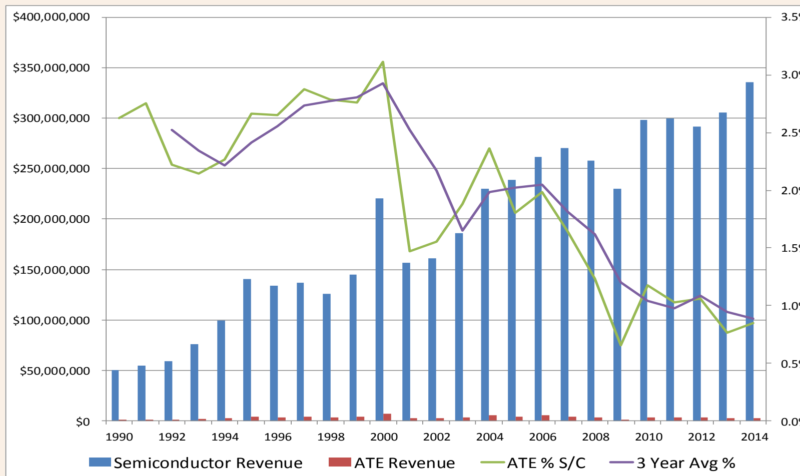
TEST COST TRENDS

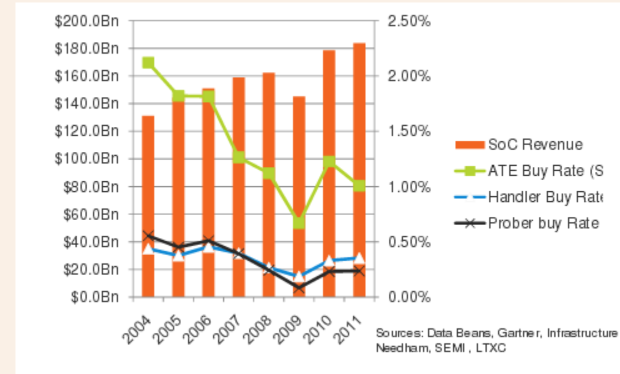
Industry Semiconductor and Test

Industry ATE Revenue vs S/C Revenue



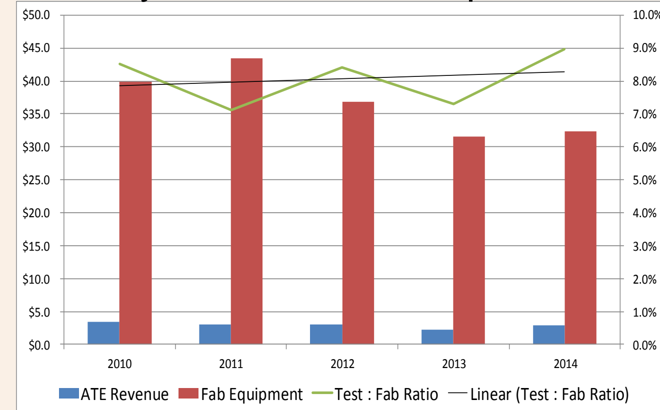
Source: Gartner, iSupply

Handler/Prober Capital Contribution



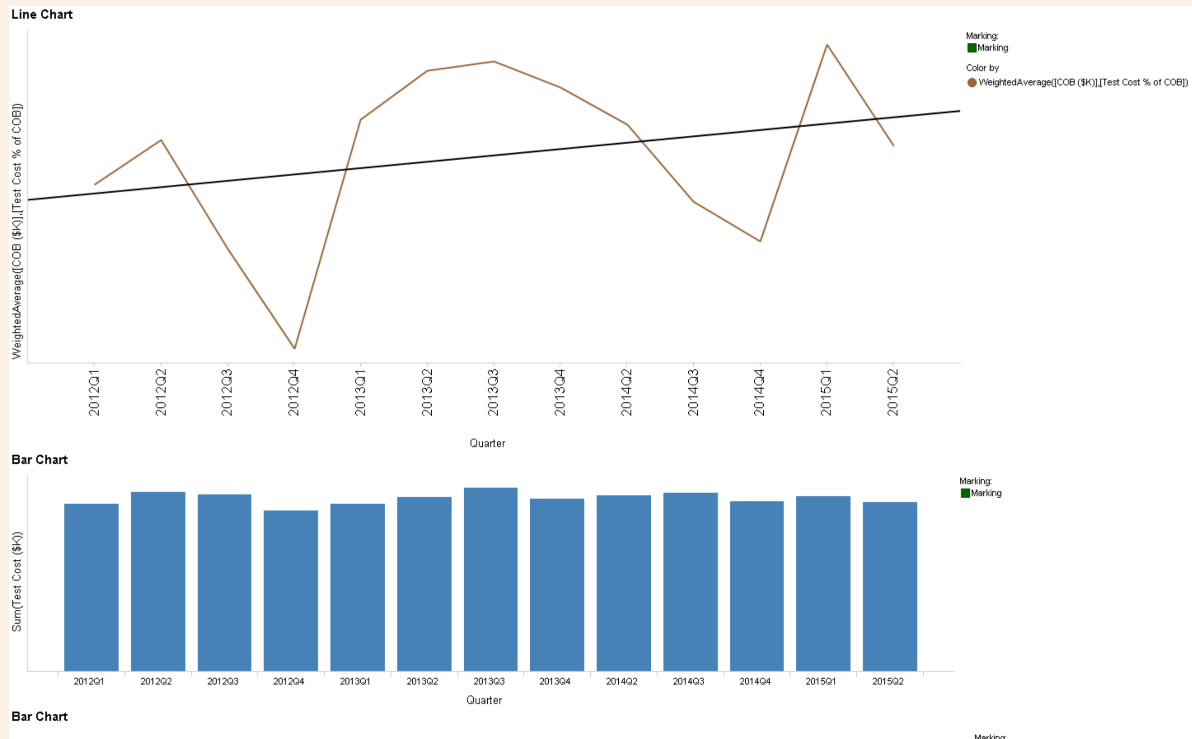
- ATE (Tester) Capital % S/C Revenue flat around 1% for 5 years
- Test cell capital is about ½ ATE and ½ handling & infrastructure
- Test capital compared to FAB capital is increasing slowly over 5 years
  - Test contribution to total manufacturing cost is **increasing**
- Depreciation is about ½ of manufacturing test cost
- **Total test cost is roughly 4% of S/C revenue**
- **Test capital is an increasing proportion of total capital spending to manufacture ICs**
  - Is test cost as a percent of total manufacturing cost going up?

Industry Test and FAB Capital and Ratio



Source: SEMI, SEAJ

TI Test Cost % Cost of Build Trends



- Slight uptrend at TI over past few years
  - Strongly influenced by move to Industrial / Automotive

End Use Changes

Bifurcation of Worldwide Semiconductor Revenue by End-use Application from 2012–2017

End-use application	2012	2013	2014	2015	2016	2017
Data processing	39.30%	39.50%	39.90%	39.40%	39.70%	39.50%
Communications	28.70%	29.10%	29.00%	29.50%	29.40%	29.50%
Consumer	14.30%	13.80%	13.20%	12.80%	12.00%	11.40%
Industrial	8.30%	8.30%	8.60%	8.70%	9.10%	9.30%
Automotive	8.20%	8.20%	8.20%	8.50%	8.80%	9.20%
Military and civil aerospace	1.20%	1.20%	1.10%	1.10%	1.10%	1.10%
Total	100%	100%	100%	100%	100%	100%

Market Realist

Source: Gartner

- Industrial and Automotive growing
- Test Requirements are increasing
  - Multiple temperature insertions
  - BurnIn

Trends Summary

- Test Cost % of Total Manufacturing cost is increasing
  - Higher equipment prices
    - ATE prices may have reached a bottom
    - Driven by demand for higher multisite
  - Automotive / Industrial driven test requirements
- Challenge to Test Professionals
  - Why is the test contribution to total IC cost increasing?
  - Is this increase acceptable?
  - How can test cost reduction be accelerated?
  - What is acceptable test cost?
  - Is more test the best way to achieve better quality?

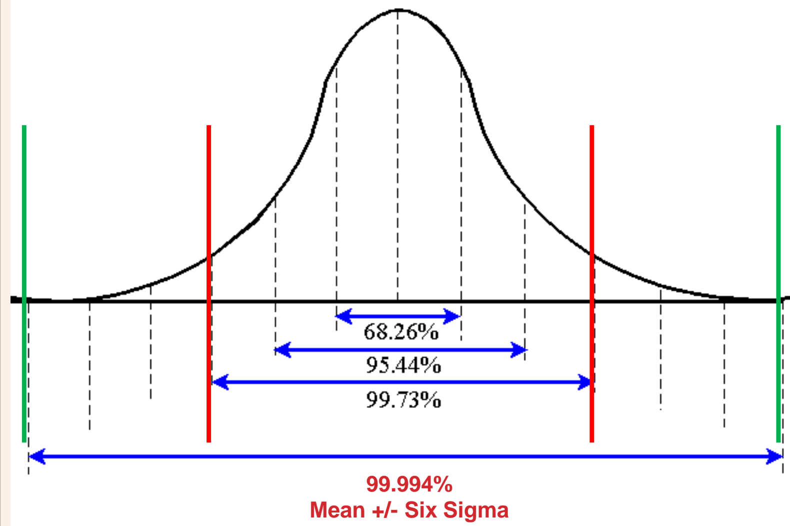
MANUFACTURING TEST & QUALITY

Purpose of Manufacturing Test

- IC Manufacturing is not Defect Free
  - Manufacturing Defects
    - Outliers, misprocess, damage, etc
    - Statistically "special causes"
  - Parametric Limits
    - Common Causes
- CHIP is *finished* when it reaches test!
  - Test generally does not add "manufacturing value"
    - Exception – Trimming or Programming devices
  - Any test cost is difficult to justify
- Test is a 100% Inspection process
  - Intended to "inspect out" any REJECT units
- **The statistics are not favorable for success**

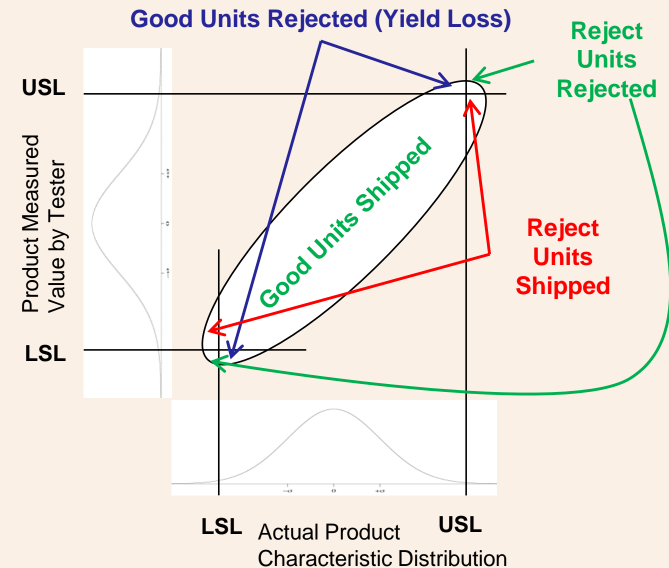
> Inspection does not improve the quality, nor guarantee quality. Inspection is too late. The quality, good or bad, is already in the product. – Dr. W Edward Deming

Test and Common Causes of REJECTS



- Spec Limits @ +/-3 Sigma
  - 0.27% of product non-conforming (2700 DPPM)
  - Test will be required to attempt to distinguish from within a smooth distribution
- Spec Limits @ +/-6 Sigma
  - 0.006% of product non-conforming (60 DPPM)
  - No need to distinguish from a continuum

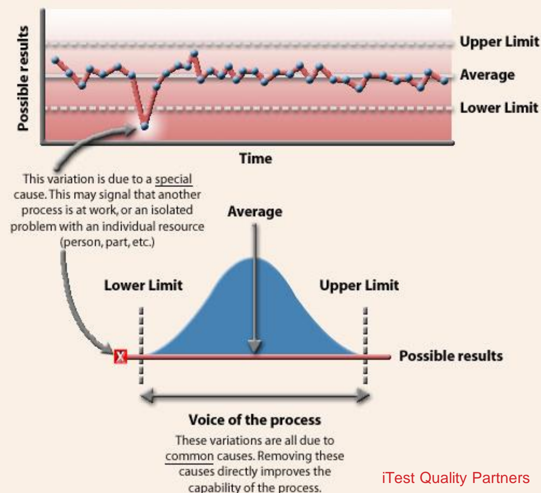
Four outcomes of 100% inspection



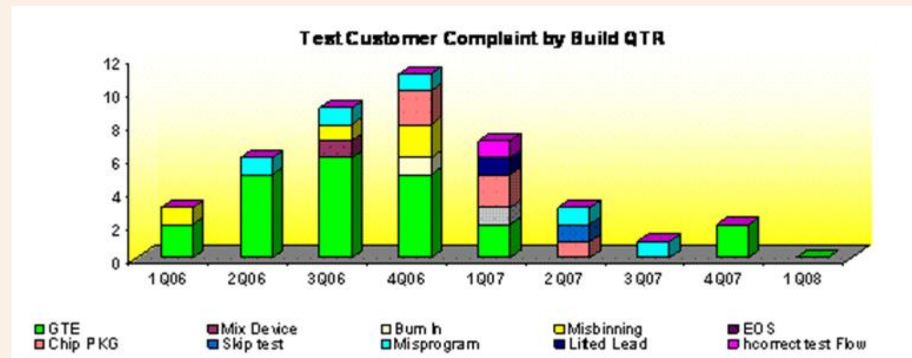
- Product and ATE both have common causes of variation
- Every tested parameter has measurement uncertainty
- If DUT performance is near the product spec limit, then sometimes the Pass/Fail result will be incorrect
- **Result is these four outcomes of 100% inspection, including YIELD LOSS and REJECTS SHIPPED**

Test and Special Causes of REJECTS

- Manufacturing defects are relatively easy to identify
  - Most units simply won't function
  - Even if the unit functions, measurements will be far from spec limits
  - Problem of tester measurement variation of measurements very near spec limit will not happen
- Customer identified rejects are defects
  - If they are easy to identify, **how do they escape to customers???**
  - Where are the common cause customer returns?

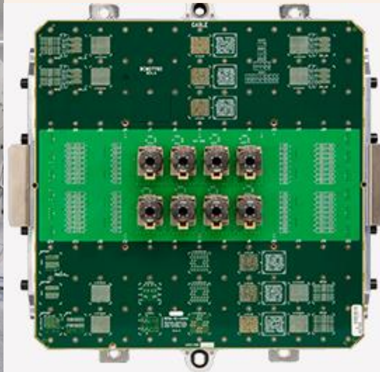


iTest Quality Partners



Test Special Cause Examples

Handler DUT I/F ATE



Tester/Handler Communication

- Tester
  - Fail H/W
  - Wrong Program
- Handler
  - Bad temperature
  - Wrong settings
  - Critical jam
  - Sort error
- DUT I/F
  - Fail H/W
  - Wrong component
- T/H Comm
  - Comm errors

Common Cause Customer Returns?

- Common cause “Reject Units Shipped”
  - Operate correctly
  - One or more parameters is close to P/F limit
  - Are not typically returned by customers
- Avoid the logic of
  - Sort out defective units   EQUALS
  - Verify every unit is good EQUALS
  - Test every spec on every unit
- To Reduce
  - Reject Units shipped
  - Test cost
  - Test-introduced Yield loss

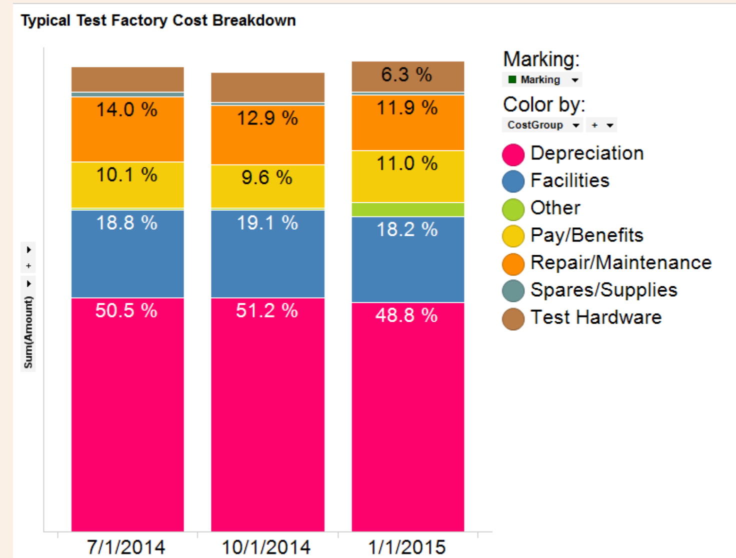
Manufacturing Test & Quality Summary

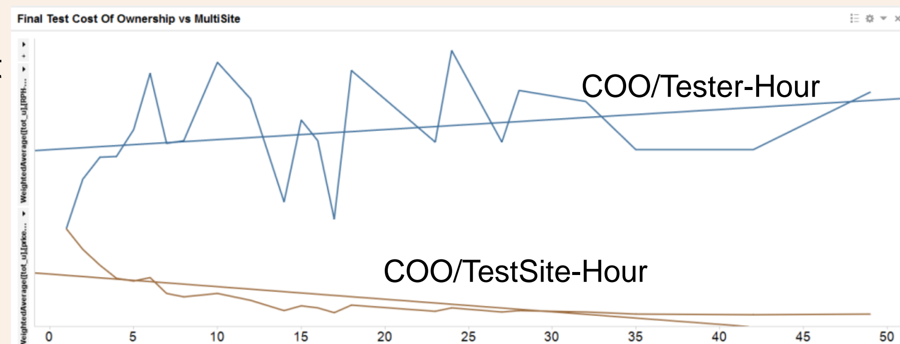
- Objective is ***sort out the defective units***.
- Understand sources of variation
  - In the product being tested
  - In the test process.
- Using test to truncate distributions causes
  - Test-related scrap (Yield loss)
  - Some rejects to ship.
- Avoid the "test every spec" trap
- Manging test cost is a key requirement

UNDERSTANDING TEST COST

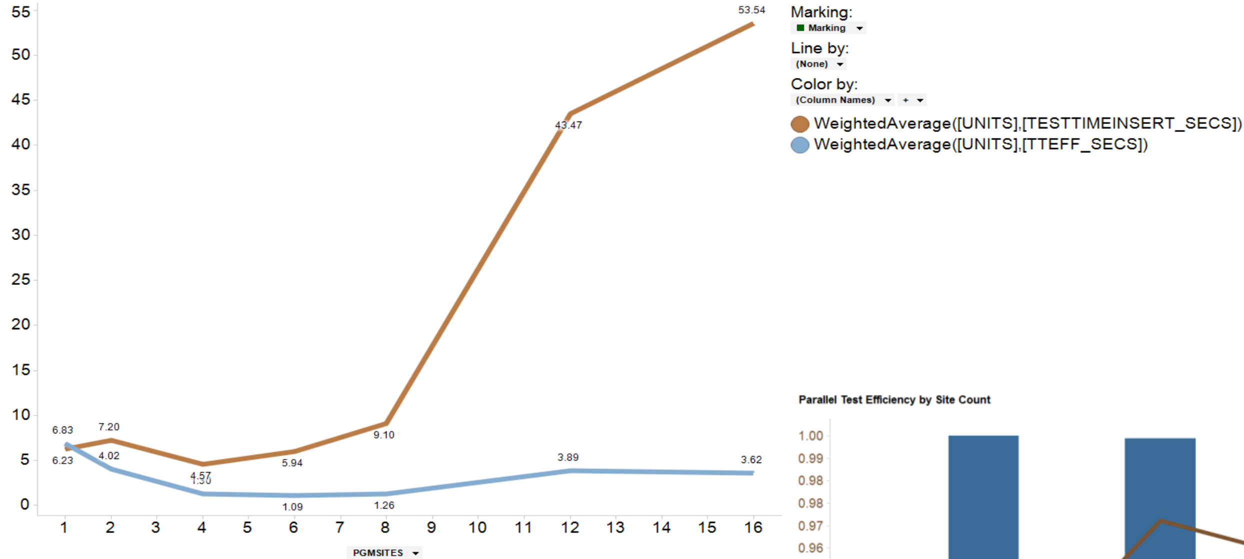
Understanding Cost of Ownership

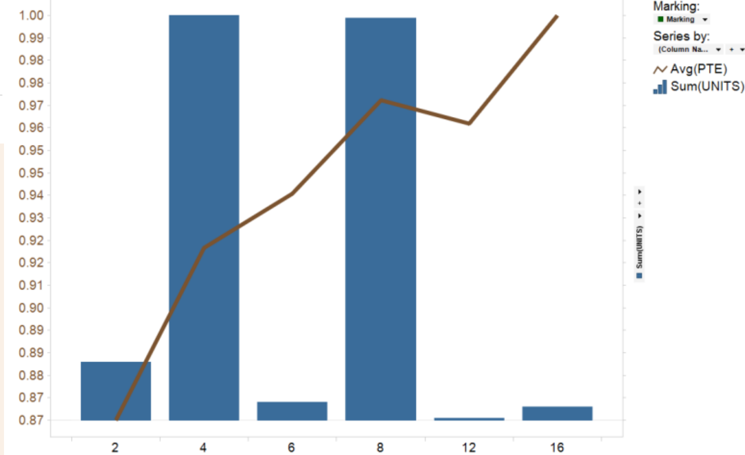
- Cost of Ownership
  - Investment drives cost
    - Facilities
    - Depreciation
    - Maintenance
  - Capital decisions critical
    - Equipment price
    - Equipment configuration
    - Equipment reliability
    - Facilities requirement
- COO per Test Site
  - Multisite improves COO
  - Factory flexibility
    - Configuration management
    - Must consume the sites





Understanding MultiSite Test

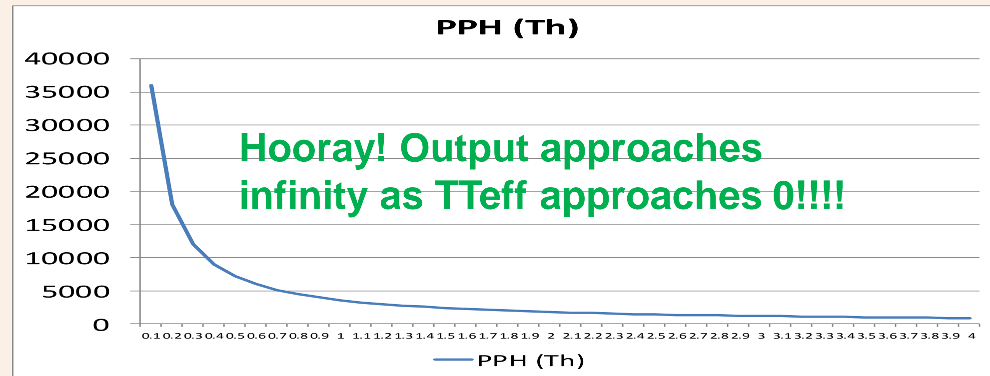


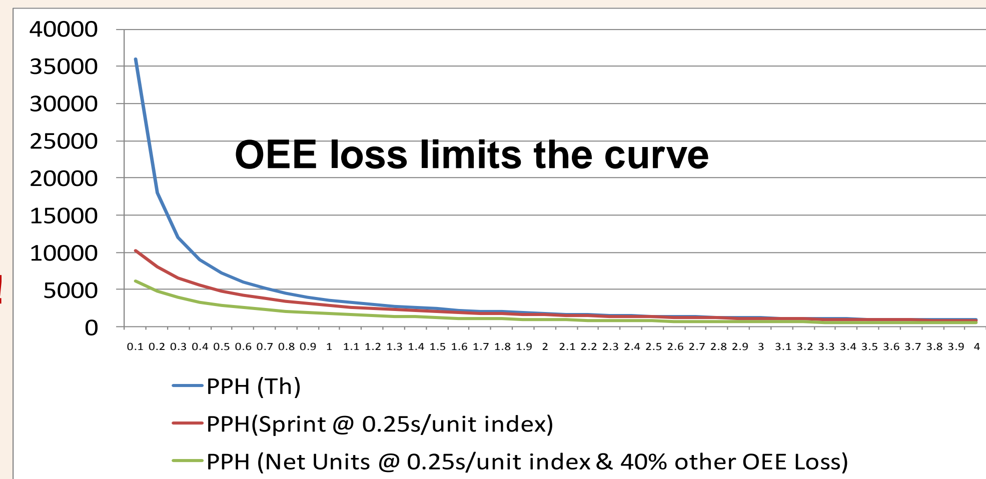


- Multisite is one approach to reduce TTeff
  - More tester resources = higher COO
    - Do those resources (ie, capital costs) have high utilization?
  - Higher DUT Interface costs
    - More complex loadboard
    - More contactors
  - PTE Challenges
- **Multisite can be an expensive approach to TTR**

Understanding PPH

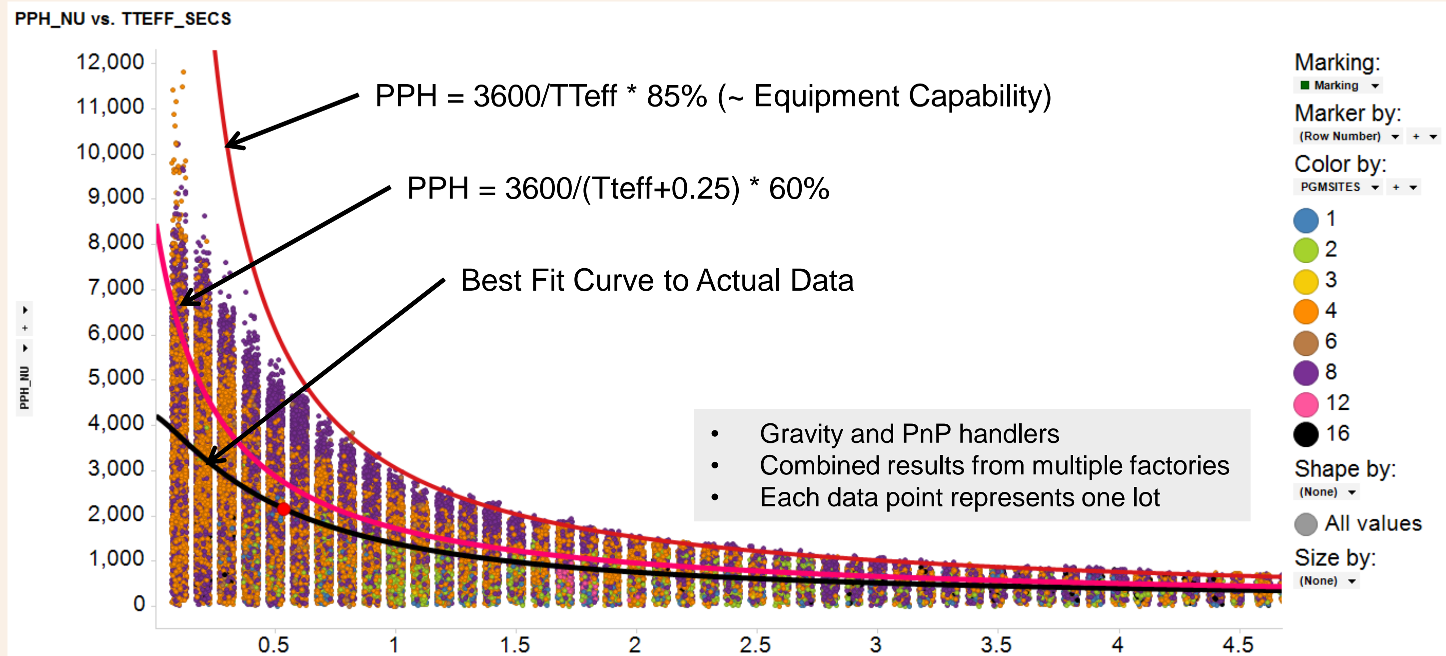
- PPH
  - Not just Test Time
    - 3600 / TTeff
  - OEE losses limit PPH
    - 3600 / (TTeff+Index) * OEE
    - Handler
      - Index
      - Load/Unload
      - Sort
    - Stops
      - Jam
      - Temperature
      - Socket
    - Between Lots
      - Program change
      - Board change
      - Contactor change
  - Model using
    - 0.25s/unit Index
    - 60% OEE
    - **6100PPH @ 100ms**
- **Test Engineer is appalled!**
- Time for a reality check



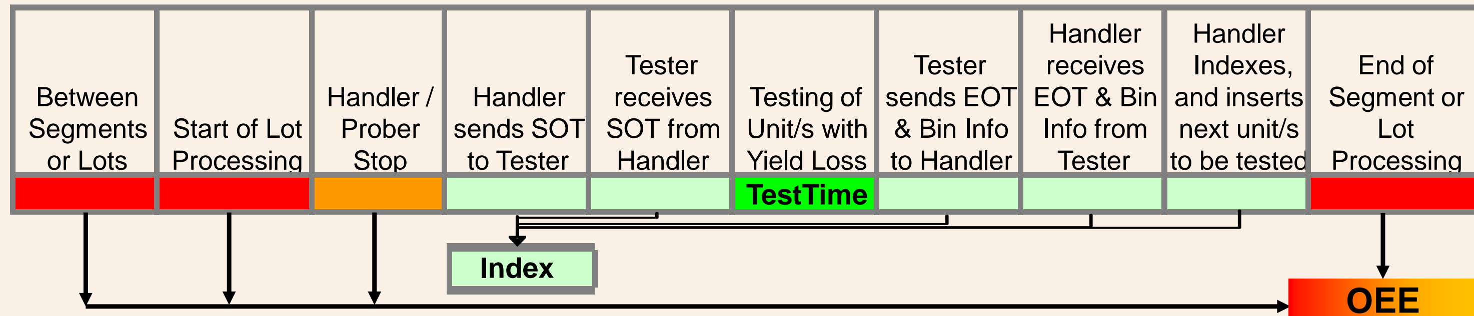


Understanding PPH

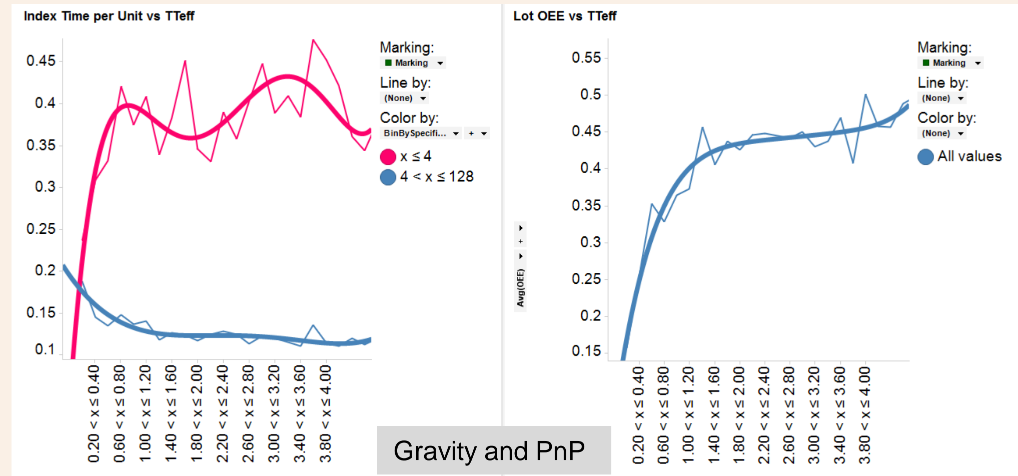
- Recent TI factory data
  - Does not even achieve what looked like a conservative model
  - Test time is not the only Test Output limit
- **What are these Index Time and OEE losses, anyway???**



Understanding PPH

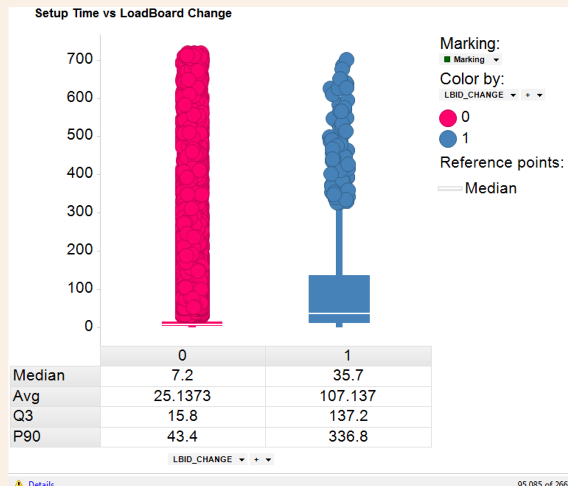


- At low test time
  - Multisite Index Time increases
  - OEE decreases
- Diminishing returns
  - Multisite
  - TTR

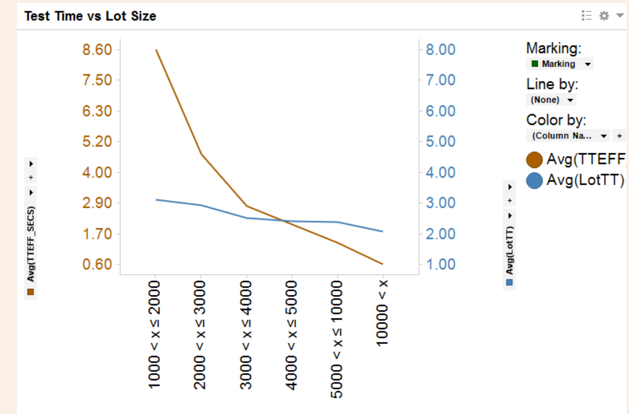


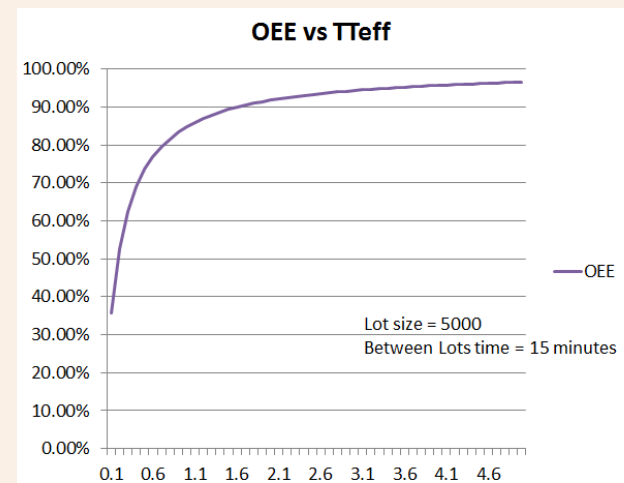
Understanding OEE Impact

- OEE Model
  - Lot Test Time (LotTT) = TT/unit * Units
    - Will be approximately steady, longer TT/unit generally correlates to smaller lot size
  - OEE= LotTT/AllTime
    - AllTime = LotTT + Overhead
    - OEE = LotTT/(LotTT+Overhead)
    - OEE Approaches 0 as TT approaches 0
- Operational impact example
  - Changing loadboard costs > 1 hour!



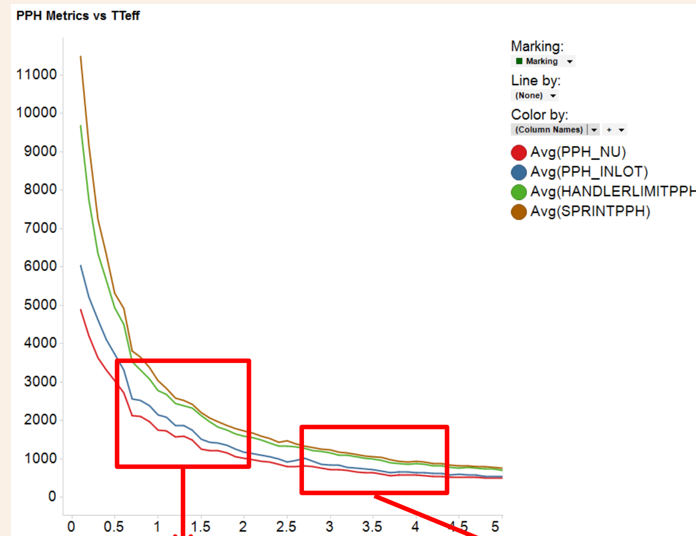
	0	1
Median	7.2	35.7
Avg	25.1373	107.137
Q3	15.8	137.2
P90	43.4	336.8

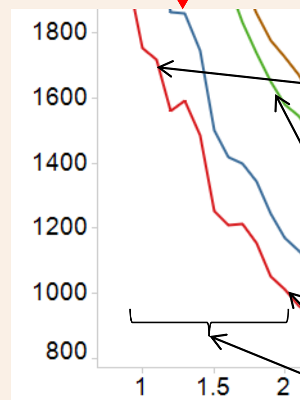




Test Time and OEE Impact

- HandlerLimitPPH to PPH_NU Gap
  - Operational
    - Handler stops
    - Between Lots
- OEE and TT impact similar
- Resource decisions
  - TTR
    - Product-by-product
    - Test Solution change/release
  - Operational Improvement
    - Factory-wide impact
    - Lower change overhead
- Find the most bang for the buck!



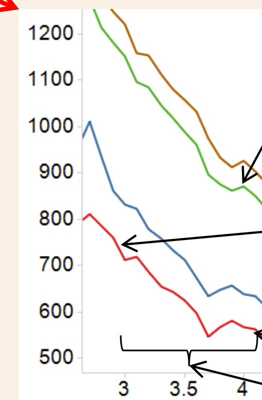


1753PPH 73%

1582PPH 56%

1011PPH

50% TTR



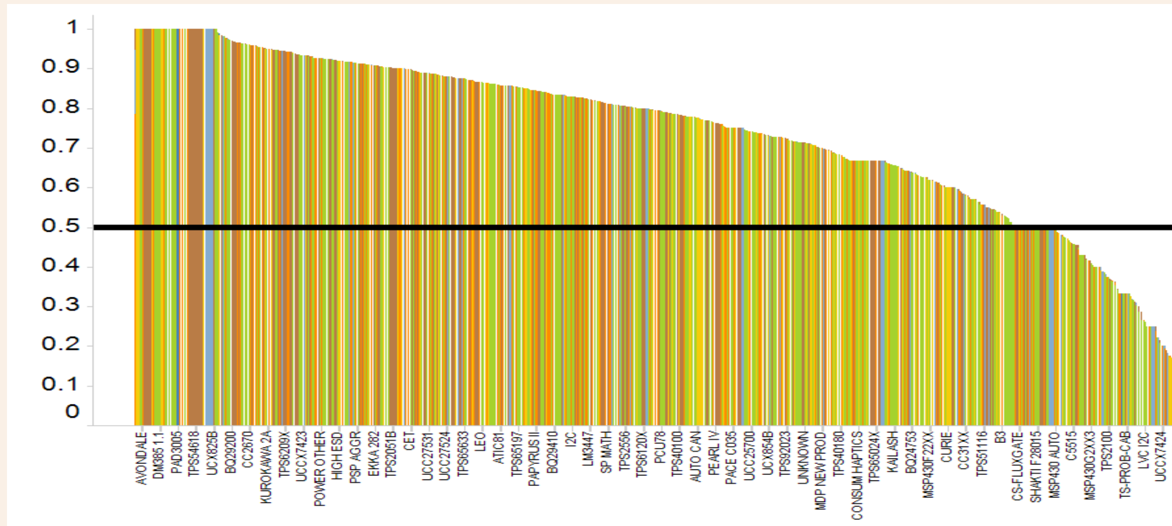
870PPH 53%

712PPH 25%

567PPH

25% TTR

Test Solution and OEE Impact



- Test Solutions have a major impact on OEE
  - Yield stability
  - DUT Interface design
    - Reliability
    - Maintainability

Test Cost Summary

- Only two controlling variables
  - COO
  - PPH
- PPH is equally controlled by
  - TTeff (Test time per unit)
  - Handler cycle time (Index or other limiters)
  - OEE (Utilization)
    - OEE can be a function of test solution design
- Diminishing returns
  - TTeff @ about 1 sec – 2 sec
  - Multisite – when TTeff approaches limit

REDUCING TEST COST

Approaches to Test Cost Reduction

- COO Reduction
  - Depreciation – Price matters
  - Pay/Benefits – Reliability, Automation
  - Maintenance – Reliability
  - Facilities – Equipment complexity matters (footprint, energy load)
  - Test Hardware
- Test Time Reduction
  - **Higher Multisite – Today's "magic bullet" from ATE suppliers**
  - Tester overhead – Value Added Theoretical Test Time (VAThTT)
  - Less test – Fewer insertions, less test/insertion
- Handling Cycle Time Reduction
  - **Separate test from sort – Another "magic bullet" for handling limits**
  - **Faster handler – Super fast turret handlers**
- OEE Improvement
  - Target rich environment

Suppliers concentrate on selling these

Where is the effort on the other variables?

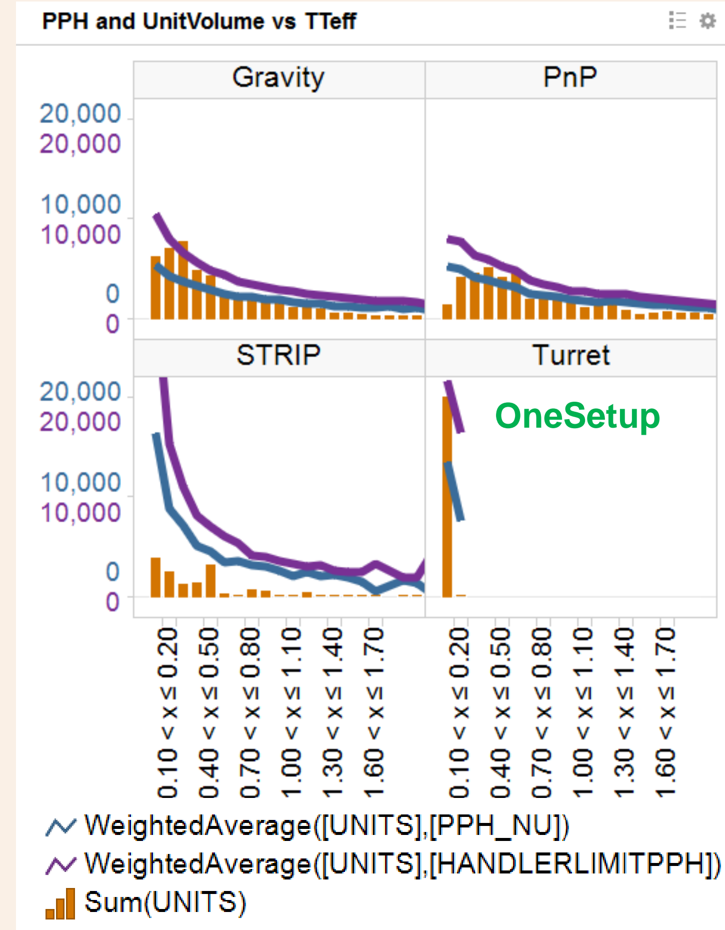
Could it be: These don't sell new equipment?

monthly Trend for JAN2016 - FEB2016

IFLEX	Dates	
	JAN2016	FEB2016
OEE	39.40	37.48
OEE (P)	36.71	35.56
OEE (R)	2.69	1.92
OEU	51.77	57.23
Idle Tester Count	4.94	5.48
DT DETAILS		
No Material	2.91	11.87
Non-Usage	14.67	10.42
No Operator	3.79	7.48
Handler|Prober Empty	6.66	5.36
Index Time	4.35	3.62
Handler|Prober Jam	3.41	3.09
Handler|Prober Soak	2.71	2.12
Tester Waiting	2.41	2.00
Device Setup	1.87	1.64
Handler|Prober Stopped	1.99	1.63
Handler|Prober_Unloading	1.68	1.53
Program Load	1.64	1.49
Handler|Prober Output Full	1.27	1.06
WaitForUnits	1.05	0.98
SPC Rules Stop	1.31	0.88
Handler|Prober Door Open	0.83	0.71
Handler|Prober_Loading	0.77	0.66
Handler|Prober Guard Band	0.67	0.58
Handler|Prober OK	0.63	0.54
Handler|Prober Input Empty	0.54	0.43
Waiting On Support	0.39	0.43
Comm Time	0.41	0.36
Production New Lot	0.41	0.34
Temperature Stabilization	0.28	0.30

Evaluating the "Magic Bullets"

- Strip test / High multisite
  - Pros
    - High multisite support
    - High throughput at low TTeff
  - Cons
    - More expensive testers
    - Sort burden is shifted
      - Cost
      - Throughput
      - Quality
    - Final Test is not "Final"
- Turret
  - Pros
    - High throughput capability
      - With OneSetup rules in place
    - Integrate Test and PostTest
    - Single-site
  - Cons
    - Small packages
    - <200ms test time
- Both are specialized
  - Benefits are at low TTeff



TTR Approaches vs Cost, Yield and Quality

	Higher Multisite	Tester Overhead Reduction	Less Test	OEE Improvement
Depreciation – Price matters				
Pay/Benefits – Reliability, Automation				
Maintenance – Reliability				
Facilities – Equipment complexity matters (footprint, energy load)				
Test Hardware				
Higher Multisite – Today's "magic bullet" from ATE suppliers				
Tester overhead – Value Added Theoretical Test Time (VAThTT)				
Less test – Fewer insertions, less test/insertion				
Separate test from sort – Another "magic bullet" for handling limits				
Faster handler – Super fast turret handlers				
OEE Improvement - Target rich environment				
Quality				
Yield				

- Multisite drives other cost and quality metrics wrong way
  - It may make sense in some cases, but evaluation is a MUST!
  - **TI has actual cases where doubling multisite reduces PPH**
- Less test drives cost and quality metrics right way
  - **Is this a surprise?**

Conclusions

- Test Cost is not improving fast enough
  - Test % total IC manufacturing cost is growing
- Test is not achieving the quality objective
  - Customers still receive rejects
  - Some are observable, some are not
  - Still rejecting GOOD units
- Optimal test time
  - Traditional equipment about 1 sec TTeff
  - Turret and Strip about 100ms Tteff
- Optimal multisite depends on impact to other cost drivers
  - Must be determined for every case
  - Many variables
- ICs **are** overtested, yet the test process is incorrect
  - Spending too much
  - Losing yield
  - Still shipping rejects, getting customer returns

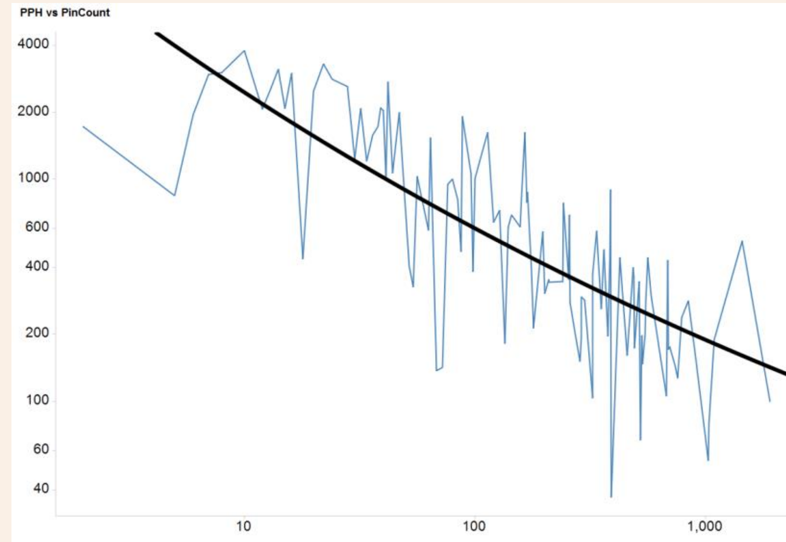
Improvement Thoughts

- Less emaphasis on parametrics
  - Focus on identifying manfacturing defects
  - Simpler, less expensive equipment
- Less complex DUT Interfaces
  - Stop building testers on the DIB Board
- More focus on OEE
  - Better development/manufacturing collaboration

NEW REQUIREMENTS AND TEST COST

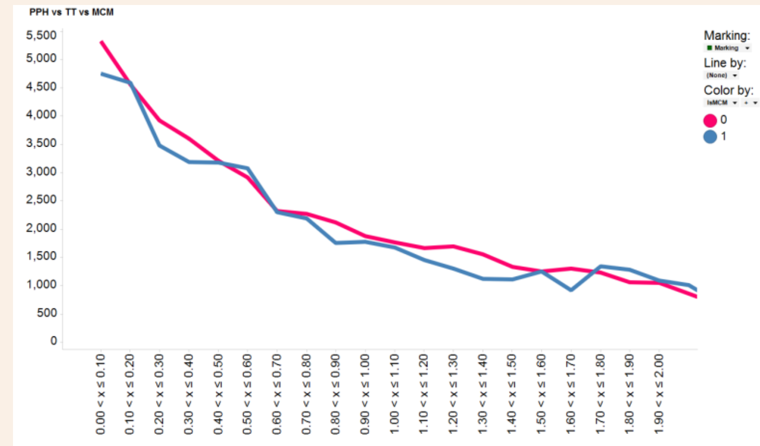
A Few New Requirement Examples

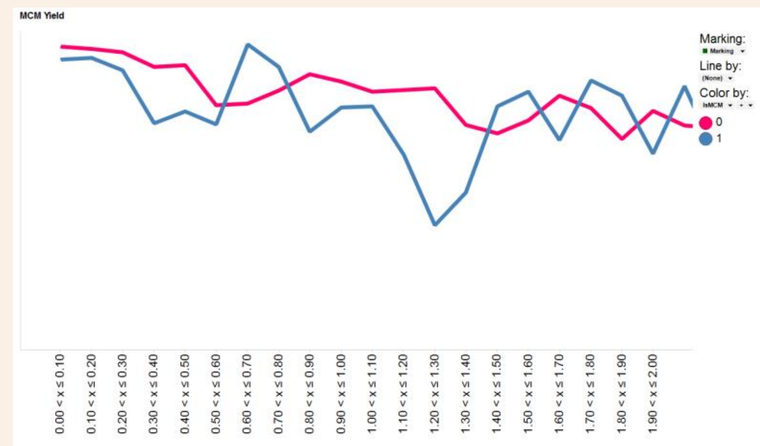
- Extreme electrical performance
  - Very high pin count
    - COO increase
    - PPH impact
  - Very high voltage
    - Specialized setup
    - OEE / PPH impact
    - COO / Loading challenge
  - Very high power
    - COO increase

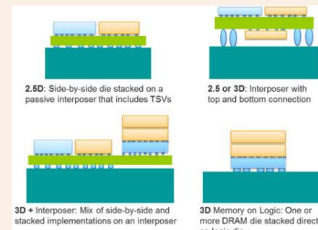


A Few New Requirement Examples

- MultiChip solutions
  - MCM
    - PPH impact
    - Yield
  - 2.5D/3D
    - More chips – more yield impact
    - Additional insertions!
      - Subassemblies
      - Partial stacks







A Few New Requirement Examples

- Other than electrical
  - Sensors
  - MEMs
  - Magnetics
  - Optical
- Challenges
  - Handling
  - Stimulus
  - Measurement
- Potential cost impact
  - Specialized equipment
    - Cost, Flexibility (ie, OEE/PPH)
  - Yield