
SEVENTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
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Mesa, Arizona
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Poster Session

BiTS Workshop 2016 Schedule

Frontiers Day

Monday March 7 - 3:30 pm

Poster Session

"WiGig Test"

Bert Brost – Xcerra

"Re-balling BGA with Gold Plated Copper Spheres, the Need and the SMT Challenges"

Emad Al-Momani, Srikanth Mothukuri, Jack Mumbo - Intel Corporation

"Thermal Test Methodology for Validating Automotive Semiconductor Packages"

Ying Feng Pang, Amy Xia – Intel Corporation

"Insitu 256 Node Resistive Leakage Tester"

Gordon Cowan, Rich Zavala - HighRel, Inc.

BiTS 2016 Burn-in & Test Strategies Workshop

HighRel, Inc.

In-situ 256 Node Resistive Leakage Tester

Mr. Gordon Cowan, President and CEO
Mr. Rich Zavala, Vice-President of Engineering

Challenges

- Data from previous testing was more generic in terms of location of failures within the DUT. Test structures are tested in groupings of pins
- DUT coverage of the testing was not complete using DUT card type of testing per old test interface equipment. Only 30 channels of testing available on current systems test
- HAST test durations are typically 200 Hour tests at 25 hr-25 hr-50 hr-100 hr test intervals with removal of the DUTs from system to gather test data for failures

System Overview / Solutions

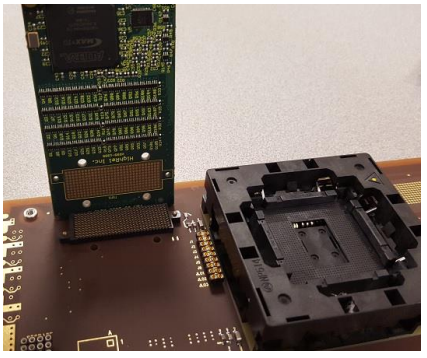
- Leakage Current Measurement in the range of 1-100 µA [+/- 1µA]. Range is set by user, per channel. Once the threshold current is met, voltage is removed from test structure during the stress test. Structure is identified and shut down. More precise data is gathered and recorded
- In-System Monitor and Report up to 256 DUT test nodes.
- Eliminates the need for removal of the DUT from environmental test to perform additional DUT testing causing decreased cycle time in product and process validation to production

Hardware

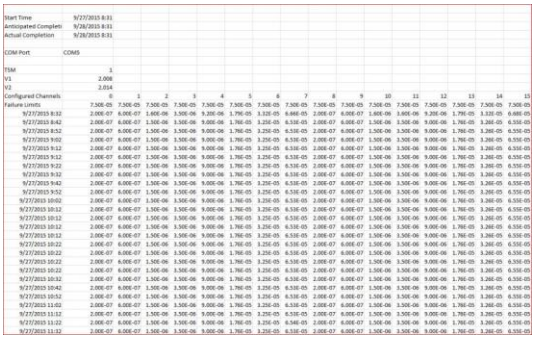
- Test system module (TSM) is 2.5” x 3.0” in size.
- Powered by a single 5Vdc supply and up to two external 1-5Vdc power supplies provide power to DUT
- 16 banks of 16 channels hosting 10K measurement resistor to GND
- 300-pin SMT compression connector used to interface to DUT
- Data management handled by local TSM microprocessor
- High precision ADC used to measure and capture data logged
- Entire TSM measurement set of 256 channels completed < 1 min
- Conformal coated to achieve long life within hostile environments

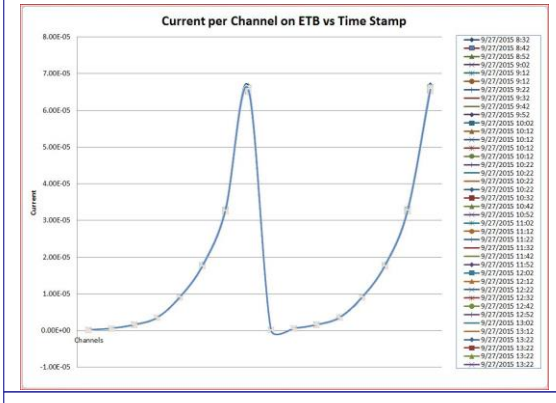
TSM and DUT test board

300 pin Connector Interface



Test Data with Time stamps





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256 Node Channel Watcher

Software

- Windows PC driven
- Embedded microcontroller resides on TSM
- Graphical User Interface (GUI) user friendly shows all system DUT information to user in single page format

Software (cont.)

- Win PC logs TSM measurement data on regular basis, show pass/fail condition of each of the 256 channels
- Application layer connects with embedded processor via single USB port and standard 1-wire communication reducing I/O pins
- Multiple TSMs available to PC for test / data management via embedded processor communication board
- Data management through simple *.csv formatted files
- Recipe files stored with test condition data, min/max fail parameters and frequency of data collection
- Test results are collected with time-stamp for each cycle measurement

GUI snapshot

Conclusion / Solutions

- Can be used in any series mode, low side sense current measurements
- Voltage is removed from DUT to preserve fail points at set threshold levels as the DUT degradation occurs
- Precise data is gathered for the location of the failed DUT structures
- 8.5 X more coverage of the DUT captured data
- TSM basically viewed as 256 low current measurement meters and the data stored in disk file information files
- Developed for HAST systems, but can be adapted to any environmental system test
- 10K resistor may be changed to rescale to other leakage range requirement
- Operator handling of DUT is kept to a minimum

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