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**BiTS**

Workshop **上海** Shanghai

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**Archive - Session 2**

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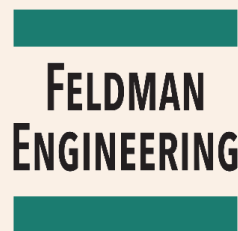
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## Session 2

Frank Zhou  
Session Chair

## BiTS Shanghai

### East Meets West

#### **"WLP Probing Technology Opportunity and Challenge"**

Clark Liu - PowerTech Technology Inc.

#### **"Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket"**

Colin Koh - Test Tooling Solutions Group

#### **"Signal Integrity & Impacts by Connector Structures"**

Jiachun (Frank) Zhou - Smiths Connectors

#### **"LPDDR4 Signal & Power Performance Optimization By Hardware"**

Yuanjun Shi - TwinSolution Technology

# Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket

**Colin Koh, Paul Gunn,  
Muhammad Syafiq, Takuto Yoshida**  
**Test Tooling Solutions Group**



**2015 BiTS Workshop  
Shanghai  
October 21, 2015**

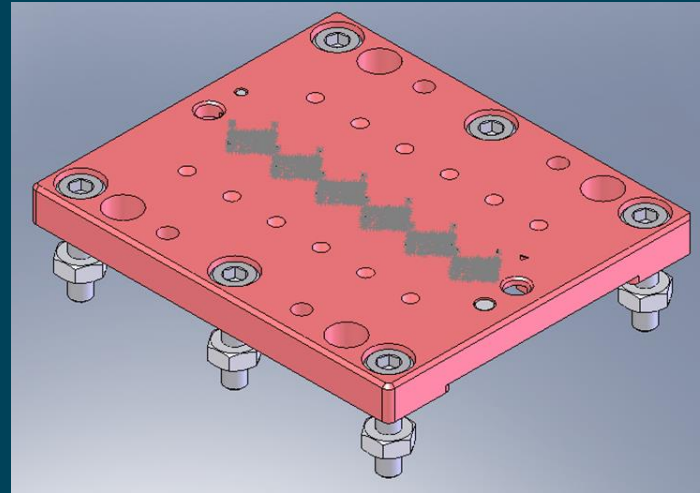


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- Conclusion

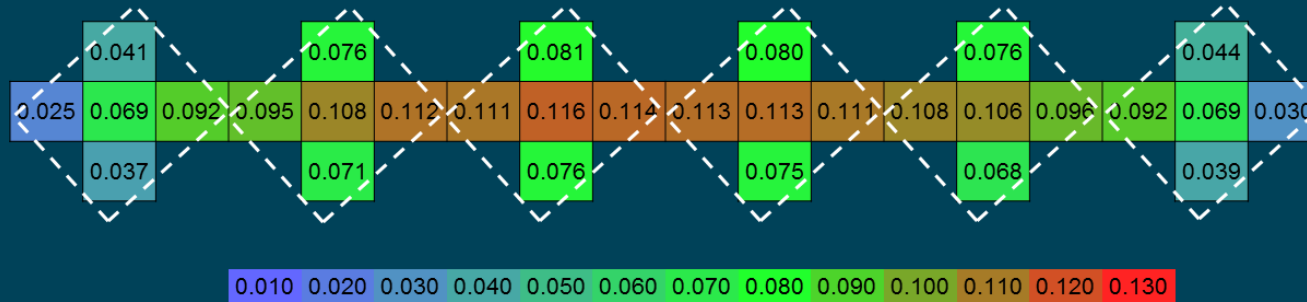
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## Socket 1 Design



- Total 1656 pins for 6 devices
- 1 Top Plate (TP) Design
- Socket side 6x M3 screws to keep TP coplanar at pin areas
- Without FEA

## Socket 1 Coplanarity Measurement

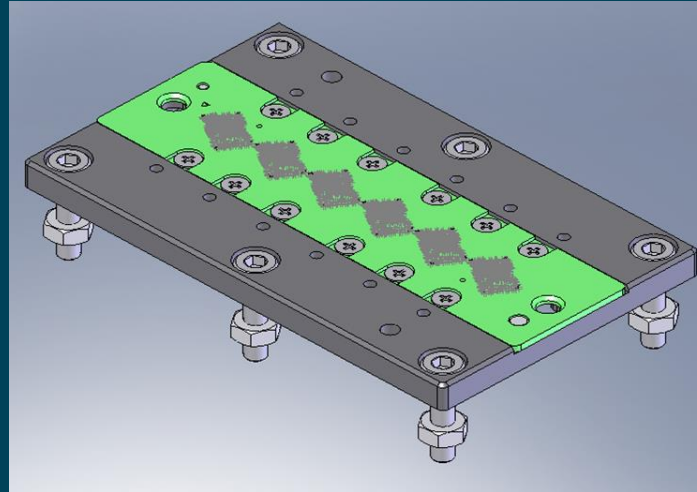


- Target 0.050mm for coplanarity
- Max. 0.116mm coplanarity from measurement
- Warp page trend shows at center area
- TP hardness is not enough
- Tight screws is far from pin areas
- FEA is required for next design



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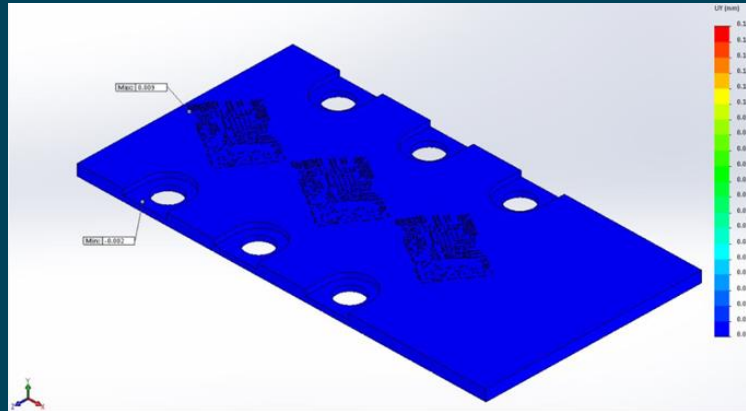
## Improved Socket 2 Design



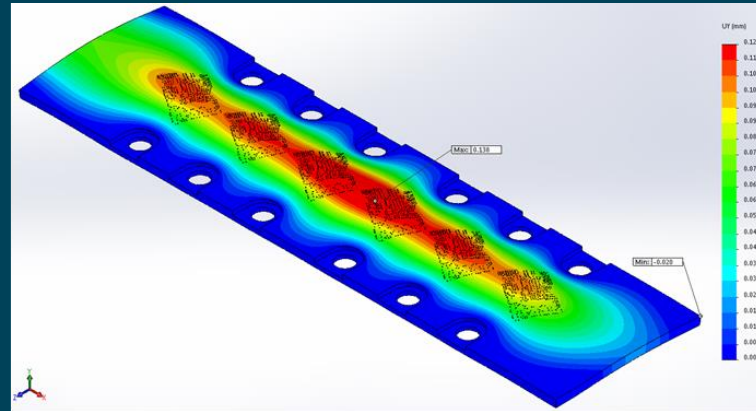
- Total 2370 pins for 6 devices
- Improvements
  - Stainless Steel Holder & Ceramic Peek TP
  - 12x TP screws closer to pin area
  - Design with FEA simulation

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## First FEA Simulation for Socket 2



Nominal Case

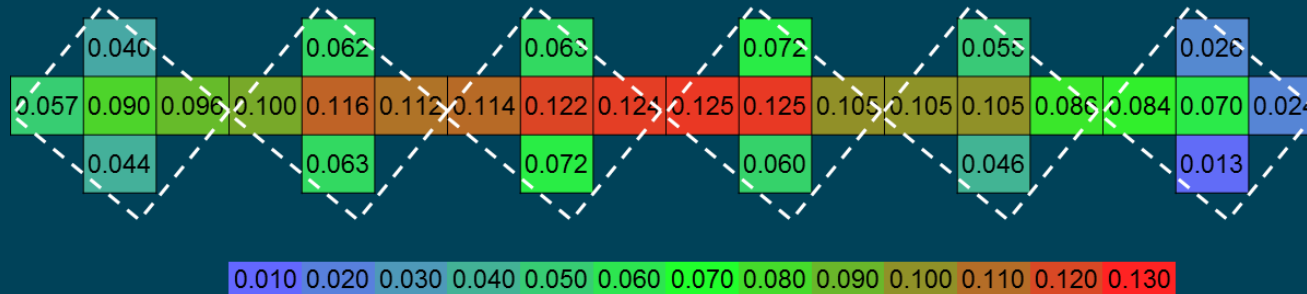


Worst Case

Items	Nominal Case	Worst Case
Coplanarity of TP [mm]	0.011	0.158

- Coplanarity values are different in nominal and worst case
- We estimated actual coplanarity close to nominal case

## Socket 2 Coplanarity Measurement



- Target 0.050mm for coplanarity
- Max. 0.125mm coplanarity from measurement
- Coplanarity measurement close to worst case
- Need to improve the FEA

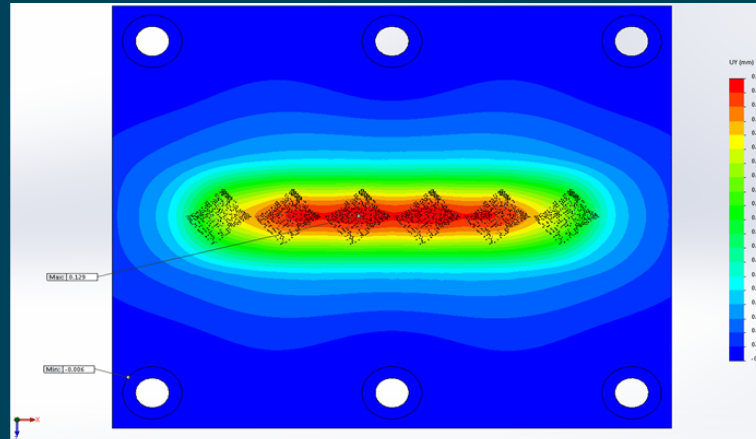
## FEA Simulation Improvement

- Implement elastic membrane technique
  - To predict deformation
  - To predict stress values
- Elastic membrane technique provides
  - More stiffness reliability
  - More robust design
- Refer to Prabakaran and Pal, Finite Element Analysis using Elastic Membrane Technique for Test Socket Design Optimization (BiTS, 2008)

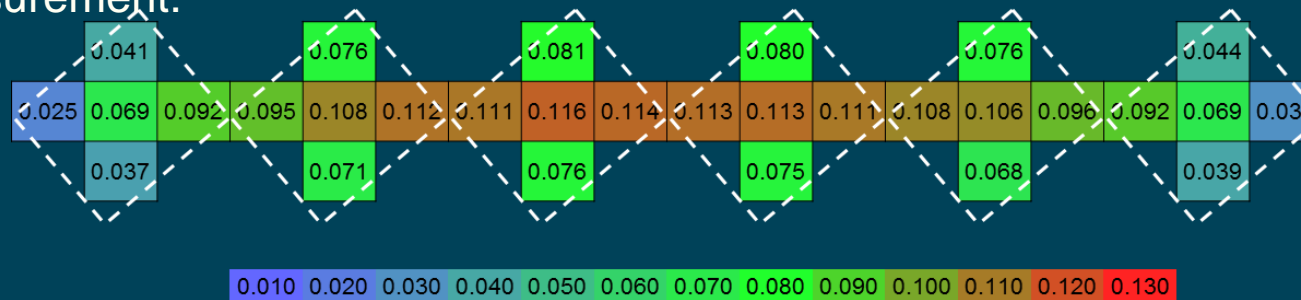
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## Improved Socket 1 Simulation & Measurement

Simulation:



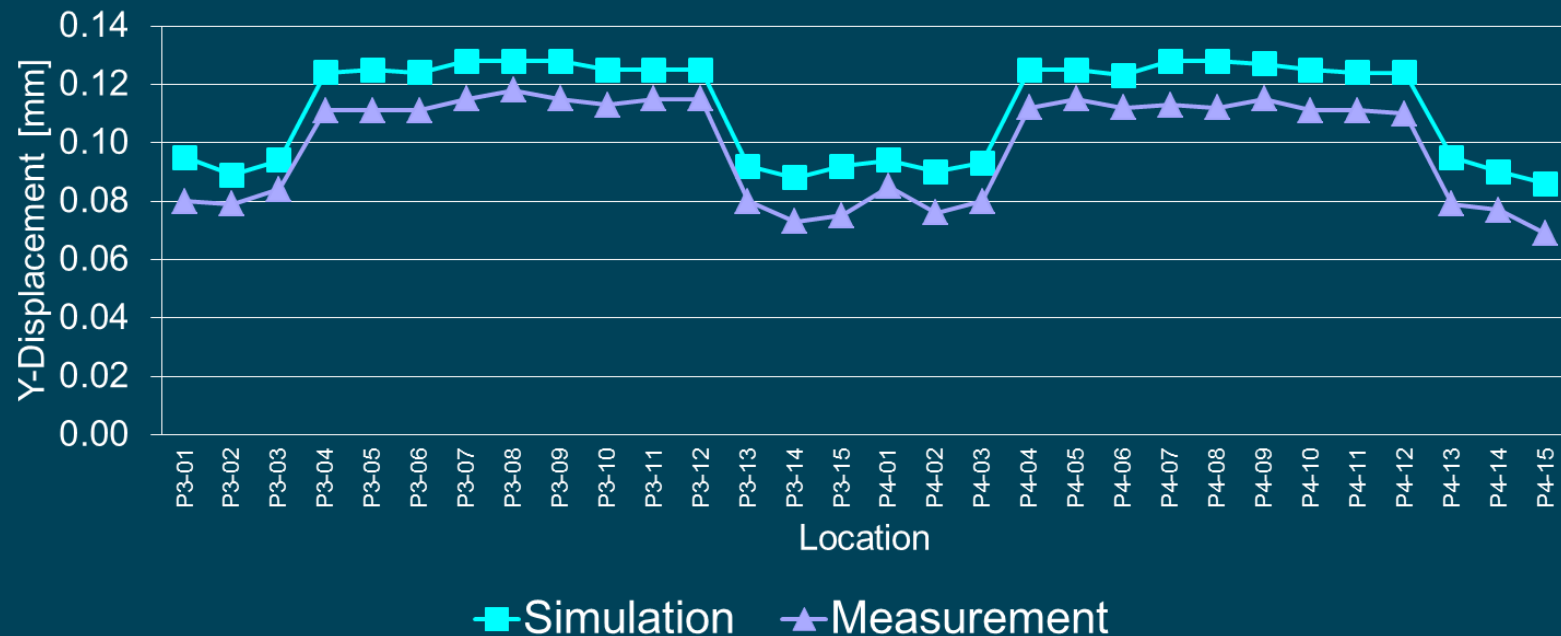
Measurement:



- Max. 0.129mm coplanarity from improved simulation
- Max. 0.116mm coplanarity from measurement

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## Compare Socket 1 Simulation and Actual Measurement

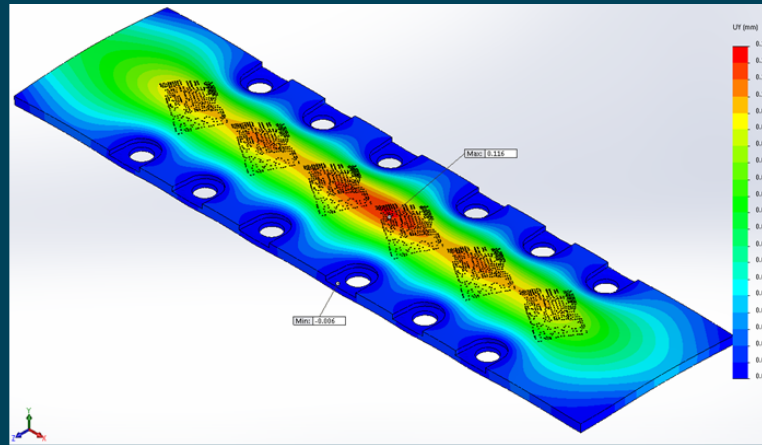


- Coplanarity error rate is 20% or less

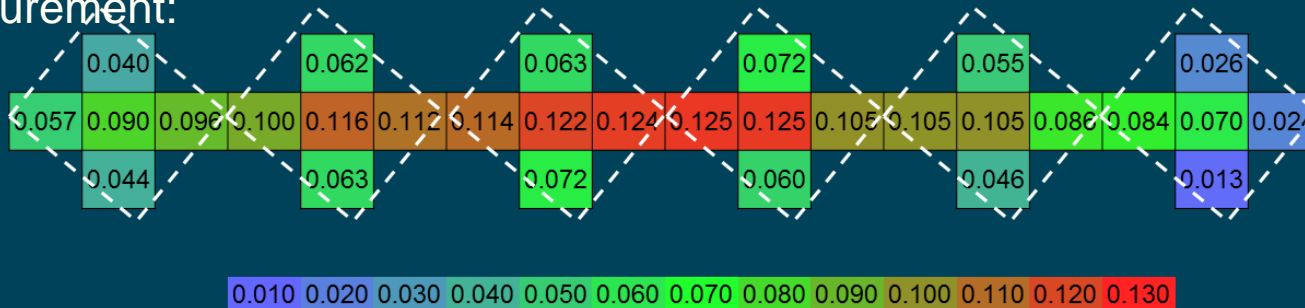
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## Improved Socket 2 Simulation & Measurement

Simulation:



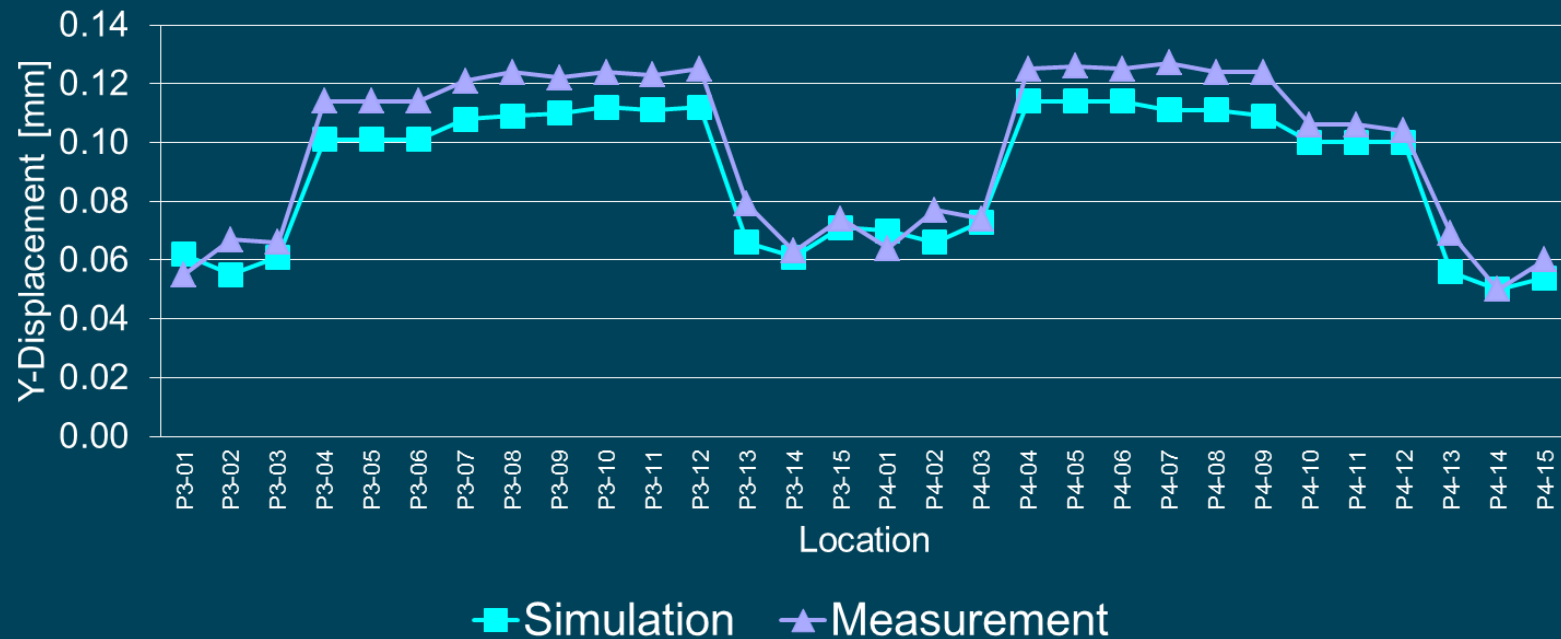
Measurement:



- Max. 0.116mm coplanarity from improved simulation
- Max. 0.125mm coplanarity from measurement

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## Compare Socket 2 Simulation and Actual Measurement

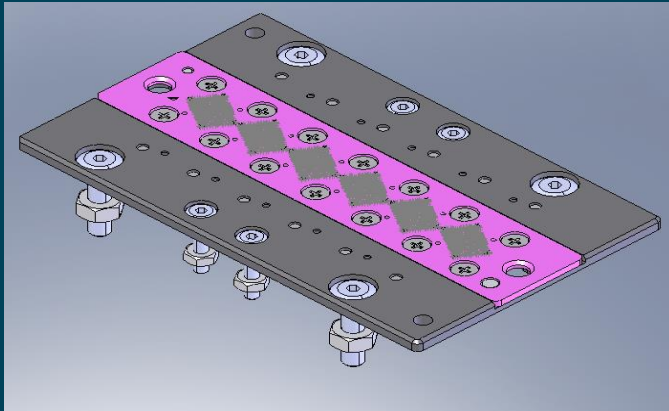


- Coplanarity error rate is 19% or less

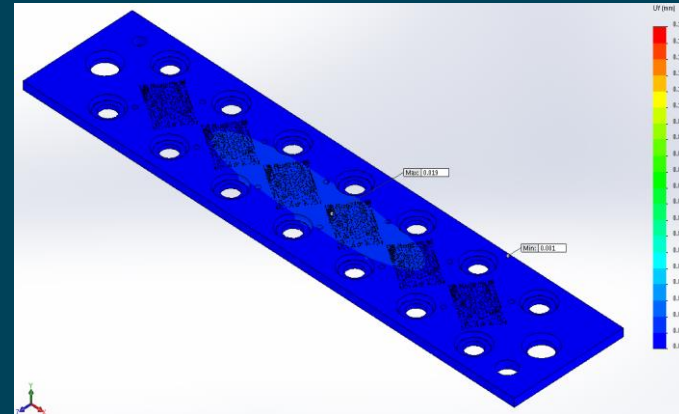


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## Improved Socket 3 Design



Socket Design



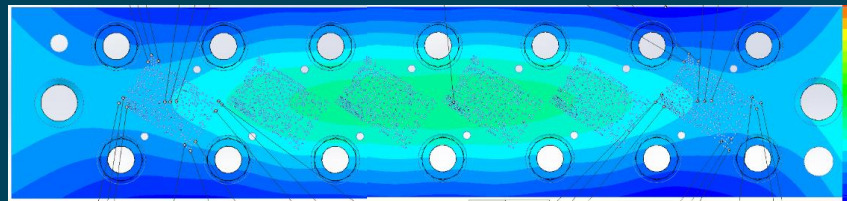
Improved Simulation

- Total 2430 pins for 6 devices
- Change TP material to Machinable Ceramic
- Target 0.050mm for coplanarity
- Max. 0.019mm coplanarity from improved simulation

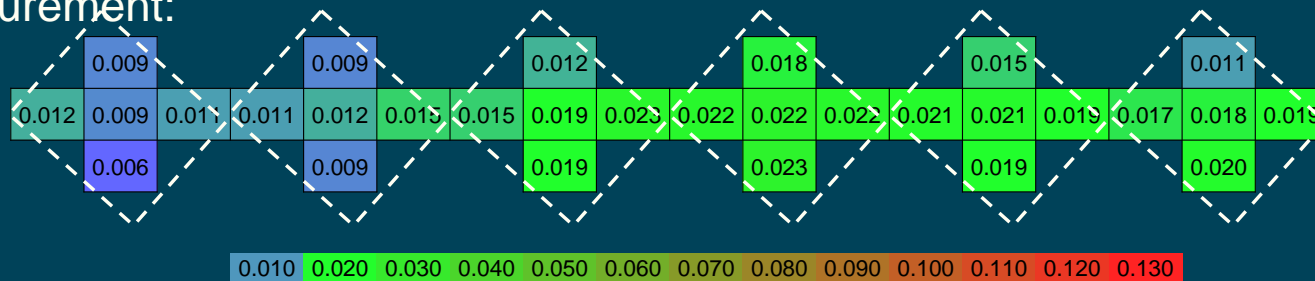
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## Improved Socket 3 Simulation & Measurement

Simulation:

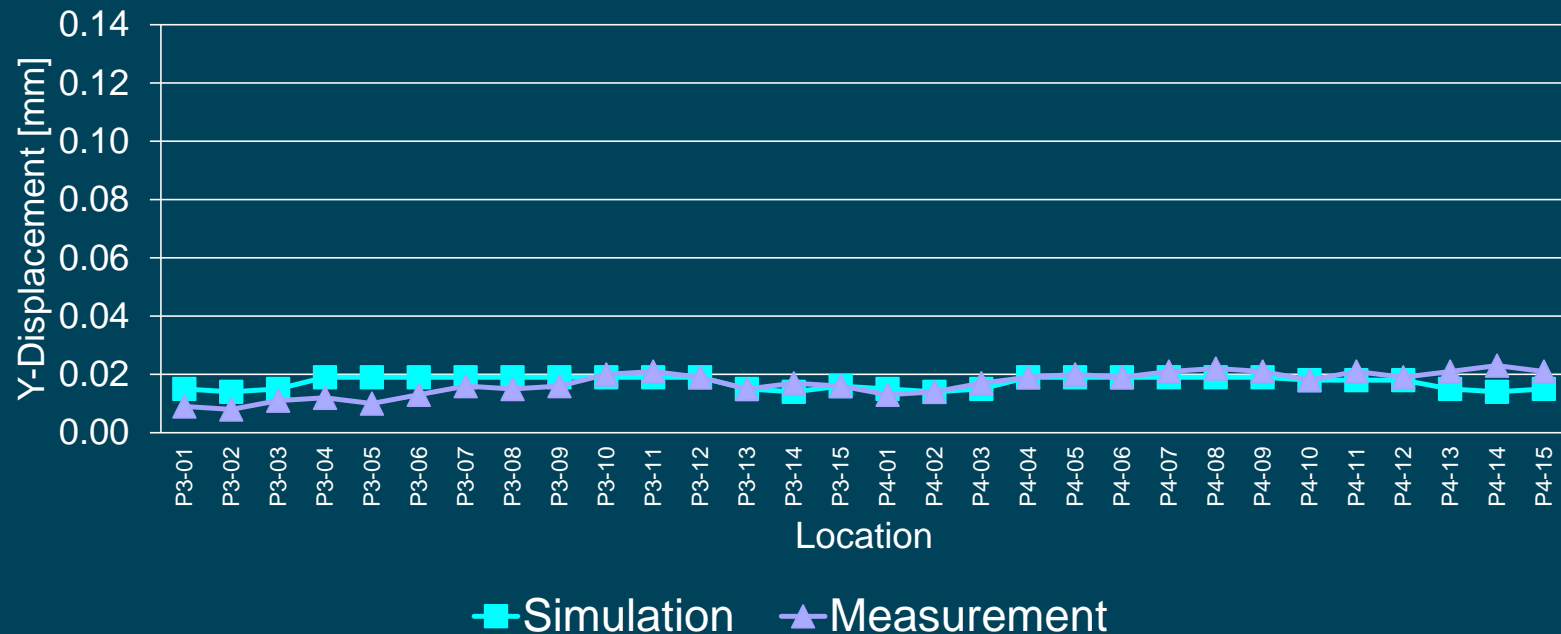


Measurement:



- Max. 0.019mm coplanarity from improved simulation
- Max. 0.023mm coplanarity from measurement

## Compare Socket 3 Simulation and Actual Measurement



- Coplanarity error rate is 21% or less

## Conclusion

- FEA simulation using Elastic Membrane technique proves good DFM relationship between design to actual socket
- FEA provides more robust design and stiffness to enhance product reliability

## Reference

- Prabakaran and Pal, 2008, Finite Element Analysis using Elastic Membrane Technique for Test Socket Design Optimization, Burn-In and Test Socket Workshop, Hot Topics Session