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October 21, 2015

Archive - Session 2

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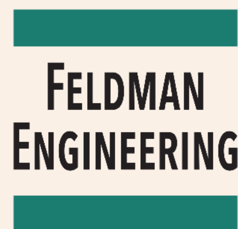

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Session 2

Frank Zhou
Session Chair

BiTS Shanghai

East Meets West

"WLP Probing Technology Opportunity and Challenge"

Clark Liu - PowerTech Technology Inc.

"Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket"

Colin Koh - Test Tooling Solutions Group

"Signal Integrity & Inpacts by Connector Structures"

Jiachun (Frank) Zhou - Smiths Connectors

"LPDDR4 Signal & Power Performance Optimization By Hardware"

Yuanjun Shi - TwinSolution Technology

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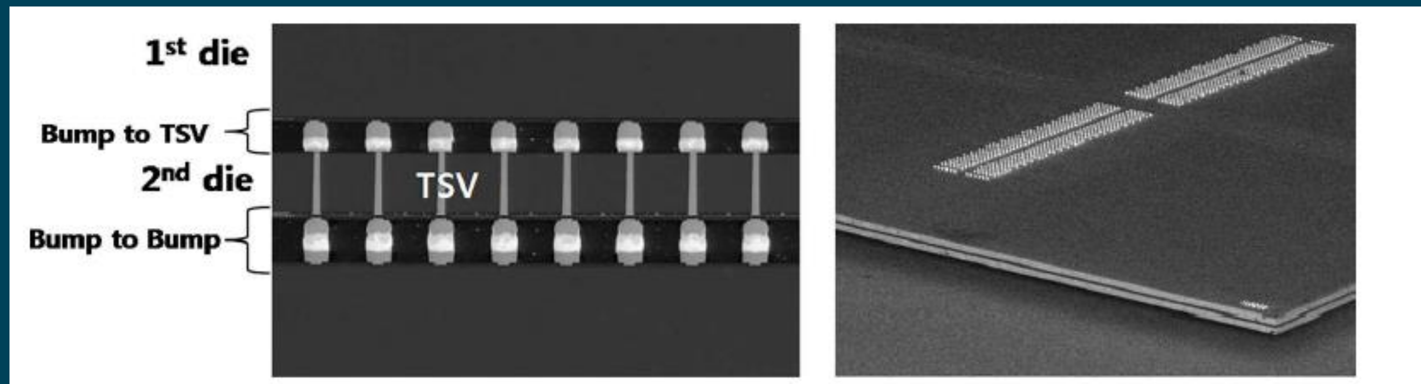
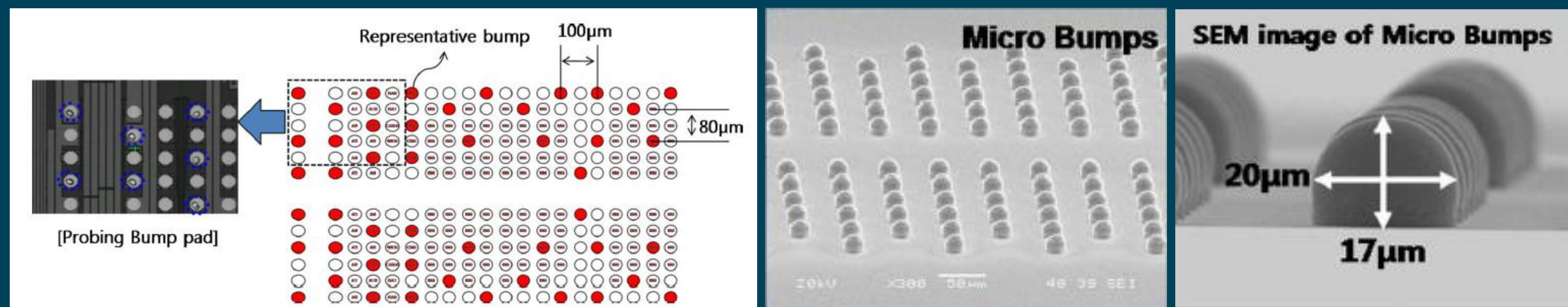
WLP Probing Technology Opportunity and Challenge

Clark Liu
Powertech Technology Inc.

2015 BiTS Workshop
Shanghai
October 21, 2015

Probing at 2Gb Wide I/O Bump Pad





Source : 2011 IEEE Samsung

More for WLP Probing Technology!

Tip Alignment

- Probe Tip Alignment – 0.3 mil Radial

Test Method

Daisy Chain Bump Structure

Planarity

- Probe Planarity < 0.5 mil (12µm)

Probe Mark

Before Contact

After Contact

*Over-Drive: 40µm

probing: 2 TDs

Probe Mark Area Under 30%

Evaluation of New Probe Technology on SnAg and Copper Bumps

28nm Mobile SoC Copper Pillar Probing Study

Probing Study of Fine-pitch Copper Pillars

2011: 150um Pitch Cu Pillar Probing

2012: 120um Pitch Cu Pillar Probing

2013: 100um Pitch Cu Pillar Probing

- In 2014, Cu Pillar is becoming the mainstream flip-chip packaging technology (Source: Yole)
- Key issue is "How to best prepare for fine-pitch Cu Pillar probing in high volume production?"

Wittig, Leong, Nguyen, Masi, Kister, Slessor

June 8-11, 2014

IEEE Workshop

2012 SWTW ASE_SV 50um Pitch Array

2014 SWTW FFI 80um Pitch CPB

WLP Probing Technology Opportunity and Challenge

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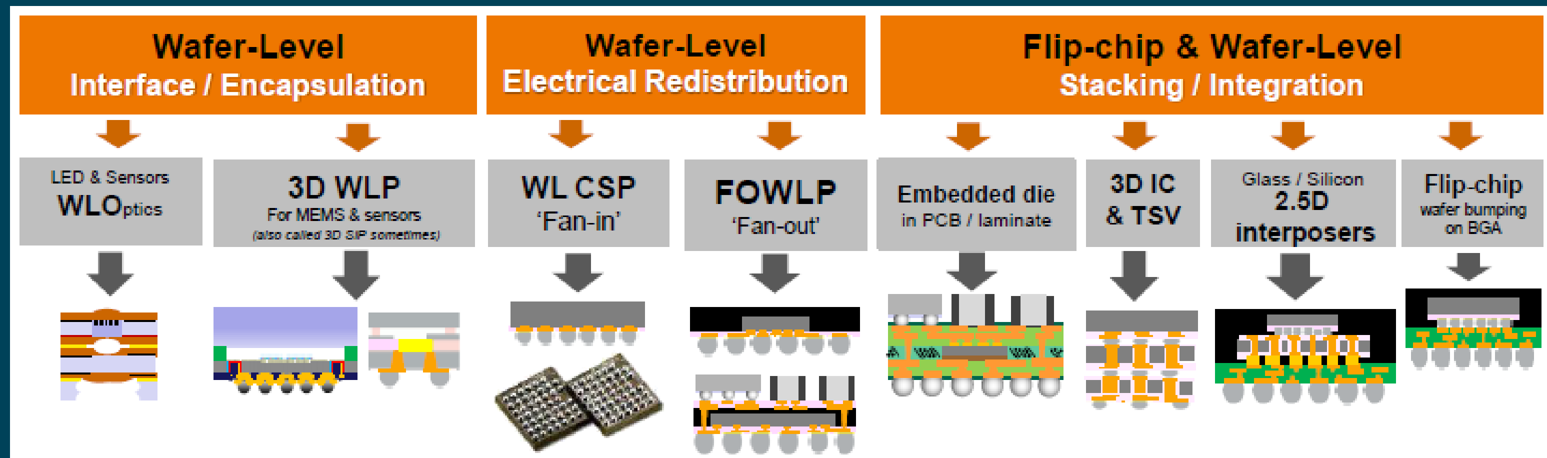
WLP (Wafer Level Packages)

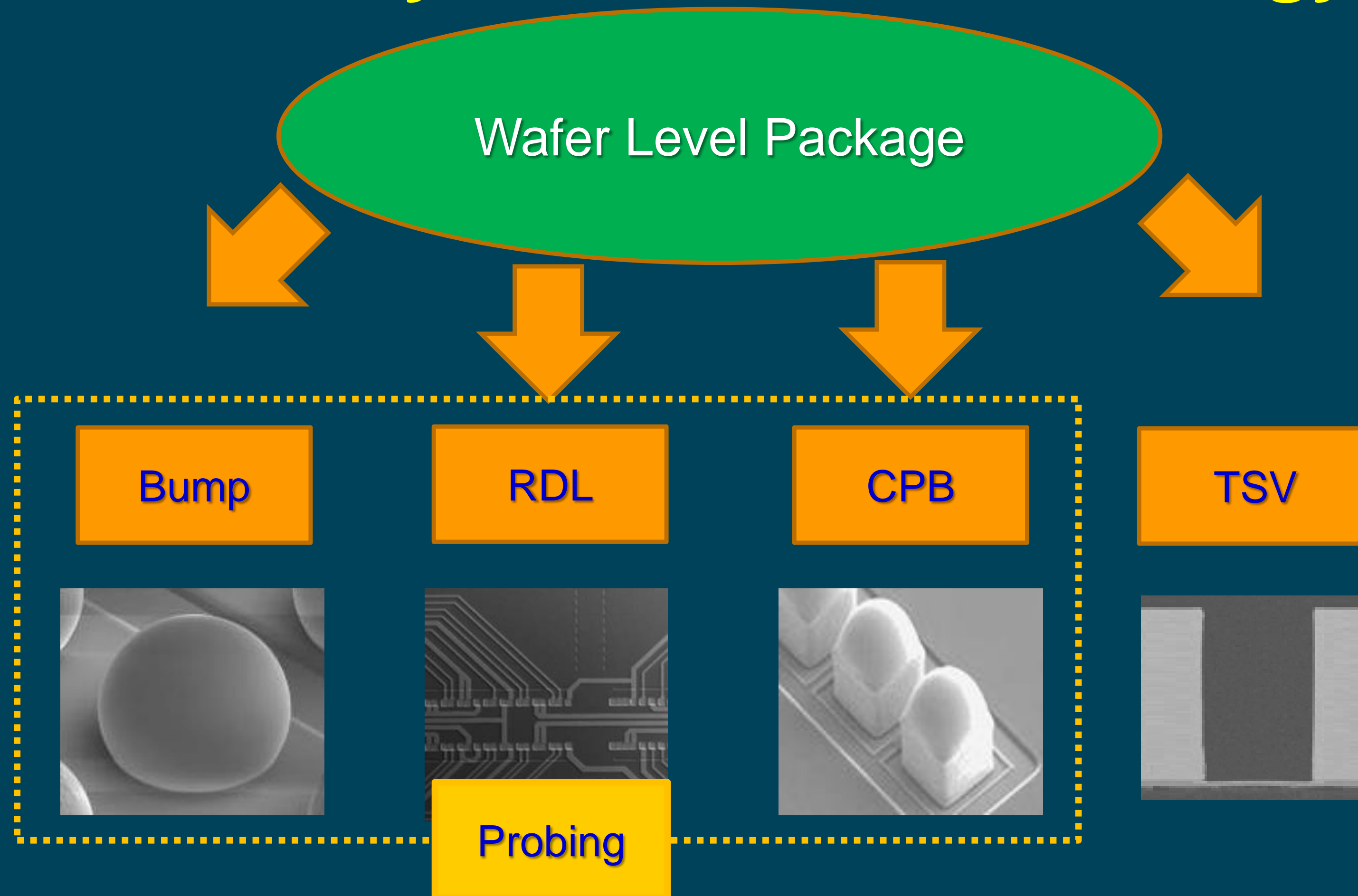


Wafer-level-packages have emerged in many different varieties that can be categorized into different advanced packaging technology platforms

Source : 2013 SEMICON Taiwan _ Yole

WLP manufacturing companies

Source : 2015 Yole


WLP Key Connection Technology
Wafer Level Package
Bump
RDL
CPB
TSV
Probing
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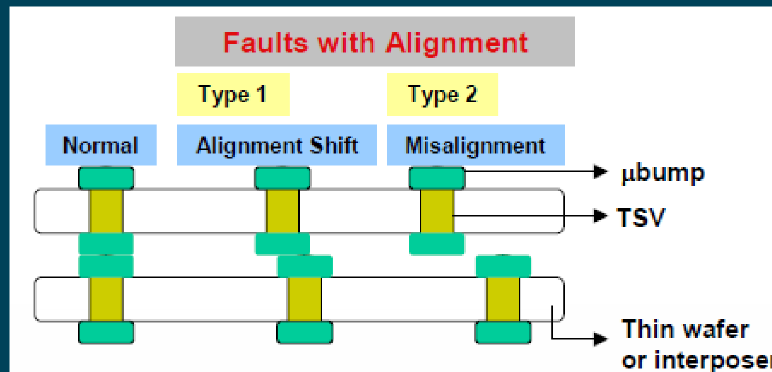
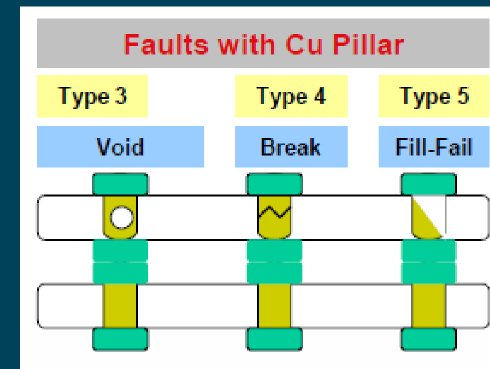
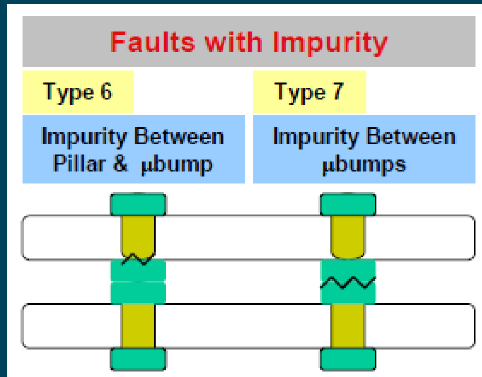
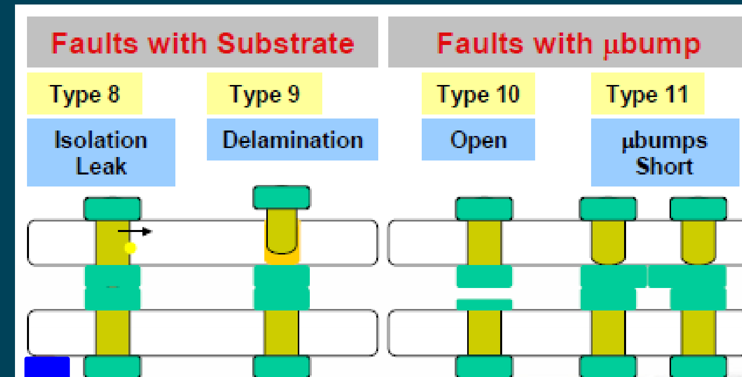
Electrical Fault Model for WLP Connectivity







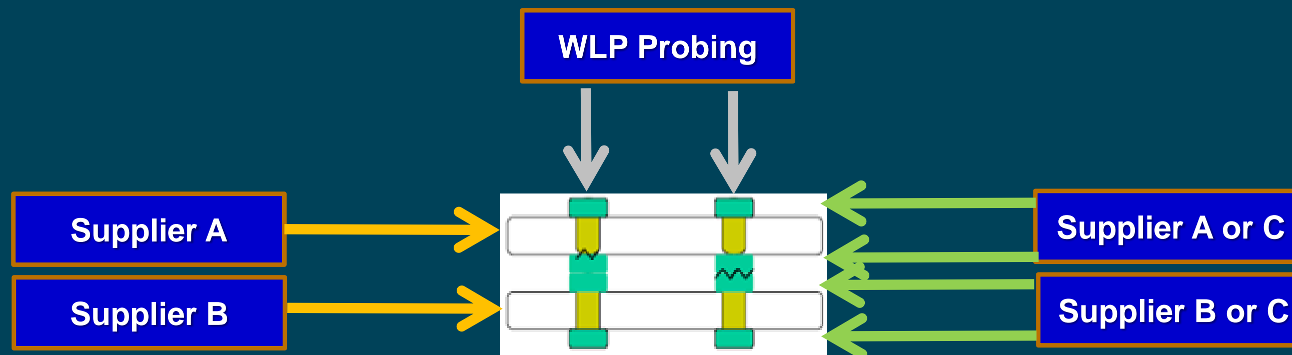


Source : 2010 IEEE 3D IC Workshop _TSMC

Fault Model for different test items

Fault Detection of Test Items											
	Fault Detection										
	Misalignment		Abnormal Cu pillar			Impurity		Substrate		micro-bump	
Test Item	Type 1	Type 2	Type 3	Type 4	Type 5	Type 6	Type 7	Type 8	Type 9	Type 10	Type 11
Continuity test		V		V					V	V	
Resistance test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
Capacitance test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
Leakage test	*V	V	*V	V	*V	*V	*V	V	V	V	*V
AC test	V	V	V	V	V	V	V	V	V	V	V

* means need high resolution measurement tool/method



Challenge?

Opportunity?

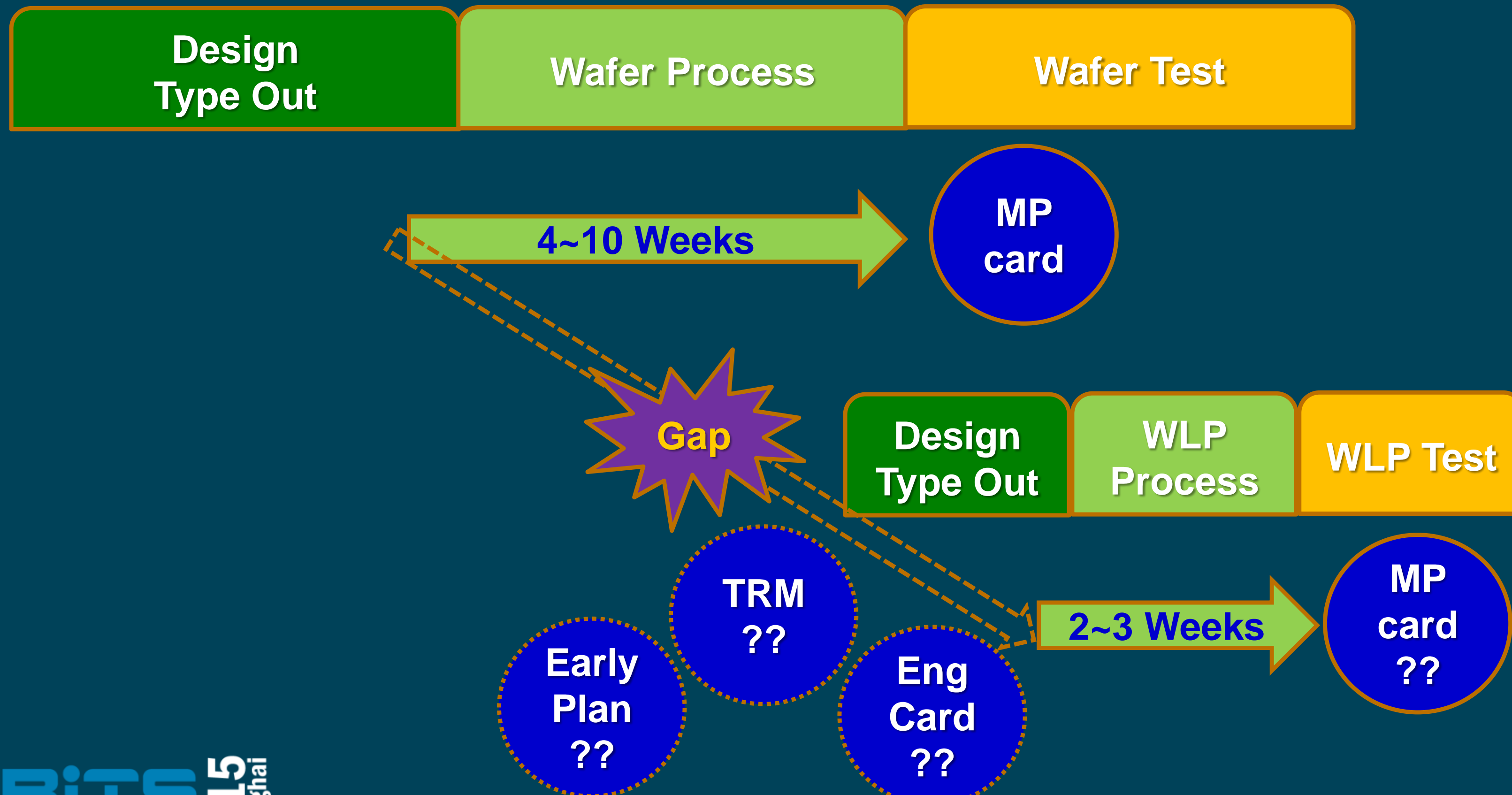
Cost?

New Model?

Technology?

Cooperation?

Source : NTHU


Case1: Tools Short Delivery Cycle Time?
Design Type Out
Wafer Process
Wafer Test
4~10 Weeks
MP card
Gap
Design Type Out
WLP Process
WLP Test
TRM ??
Early Plan ??
Eng Card ??
2~3 Weeks
MP card ??
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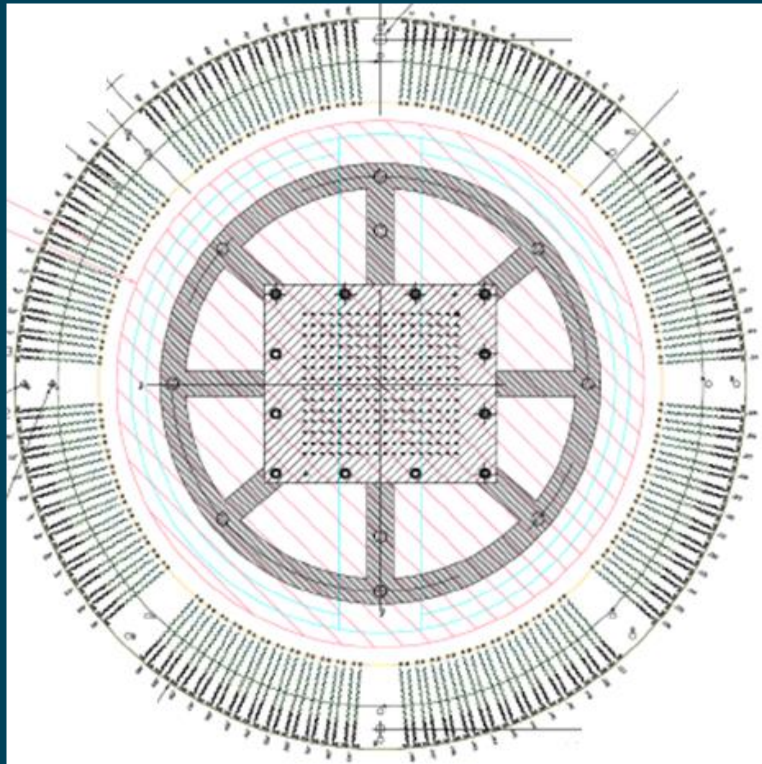
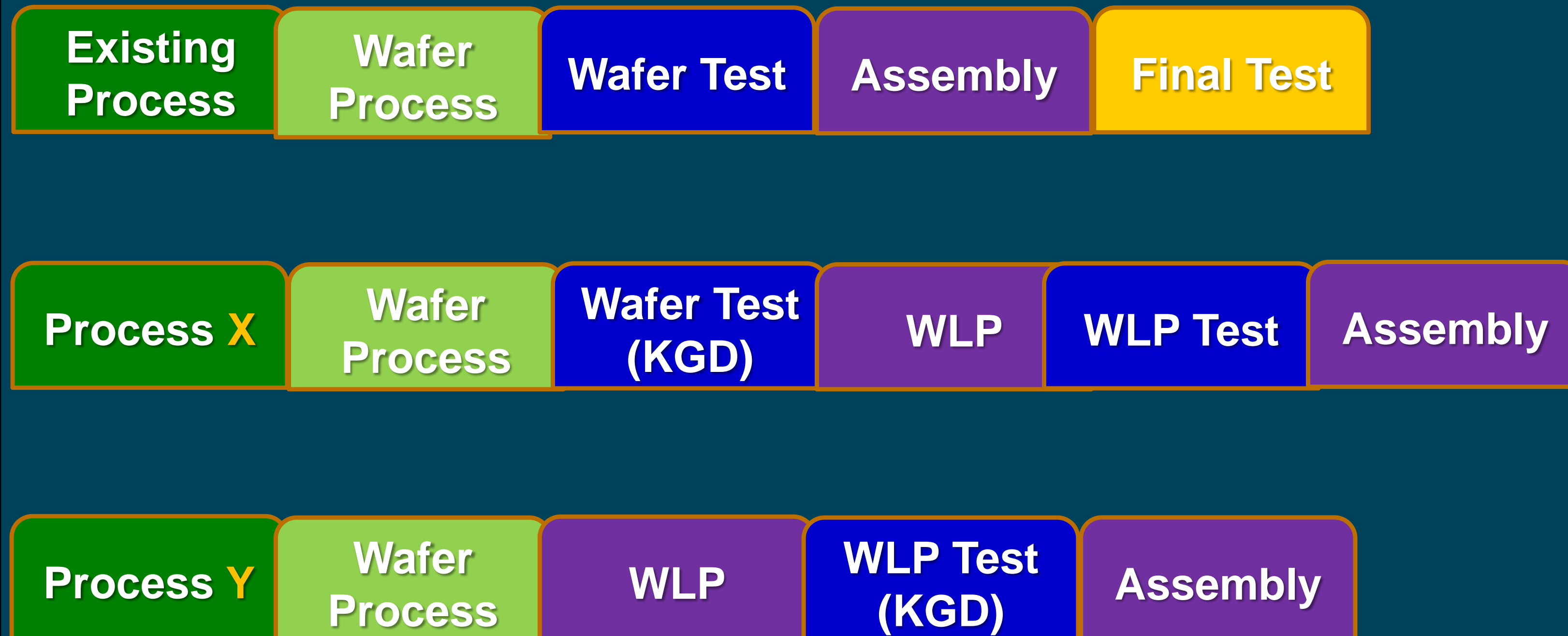
[Ex] WLCSP 256DUT Probe card



- Device: WLCSP
  - a. Diameter: 300um
  - b. Height: 180um ± 10%.
  - c. Pitch: 500um
  - d. TD : 10
  - f. Total Pin Count 2560 Pins

Delivery Time : 8 Weeks

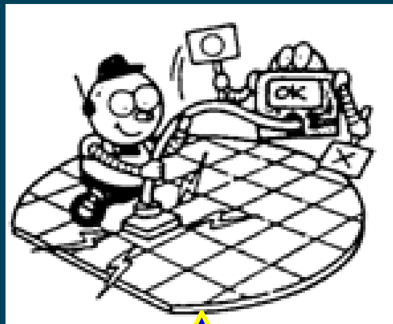
Case2: Process Change for more Chip Probing?

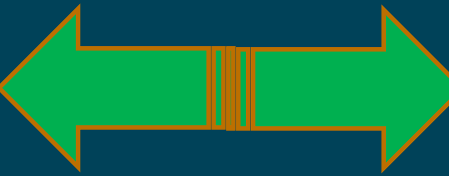


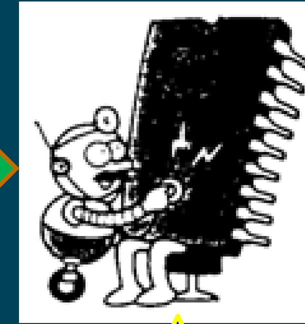
More WLP Test or More Final Test?

WLP Test

Final Test







- Fine Pitch
- Contact Force
- Silicon Base

um

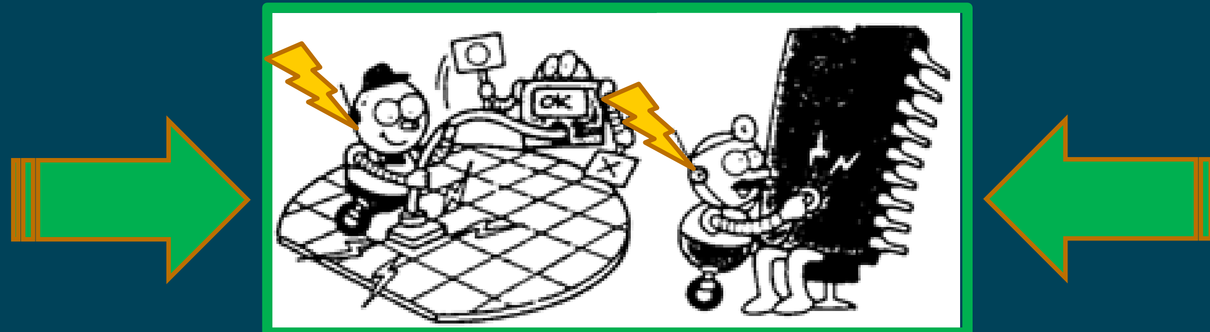
- Pitch Limit
- Clean/10K Cleanness
- Package Base

mm

Pictures Source : Mitsubishi

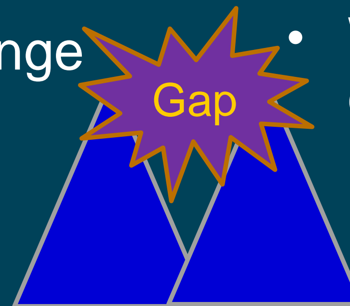
Wafer Test or Finial Test Vender @ WLP Testing?

- Wafer Test Vender
- Final Test Vender



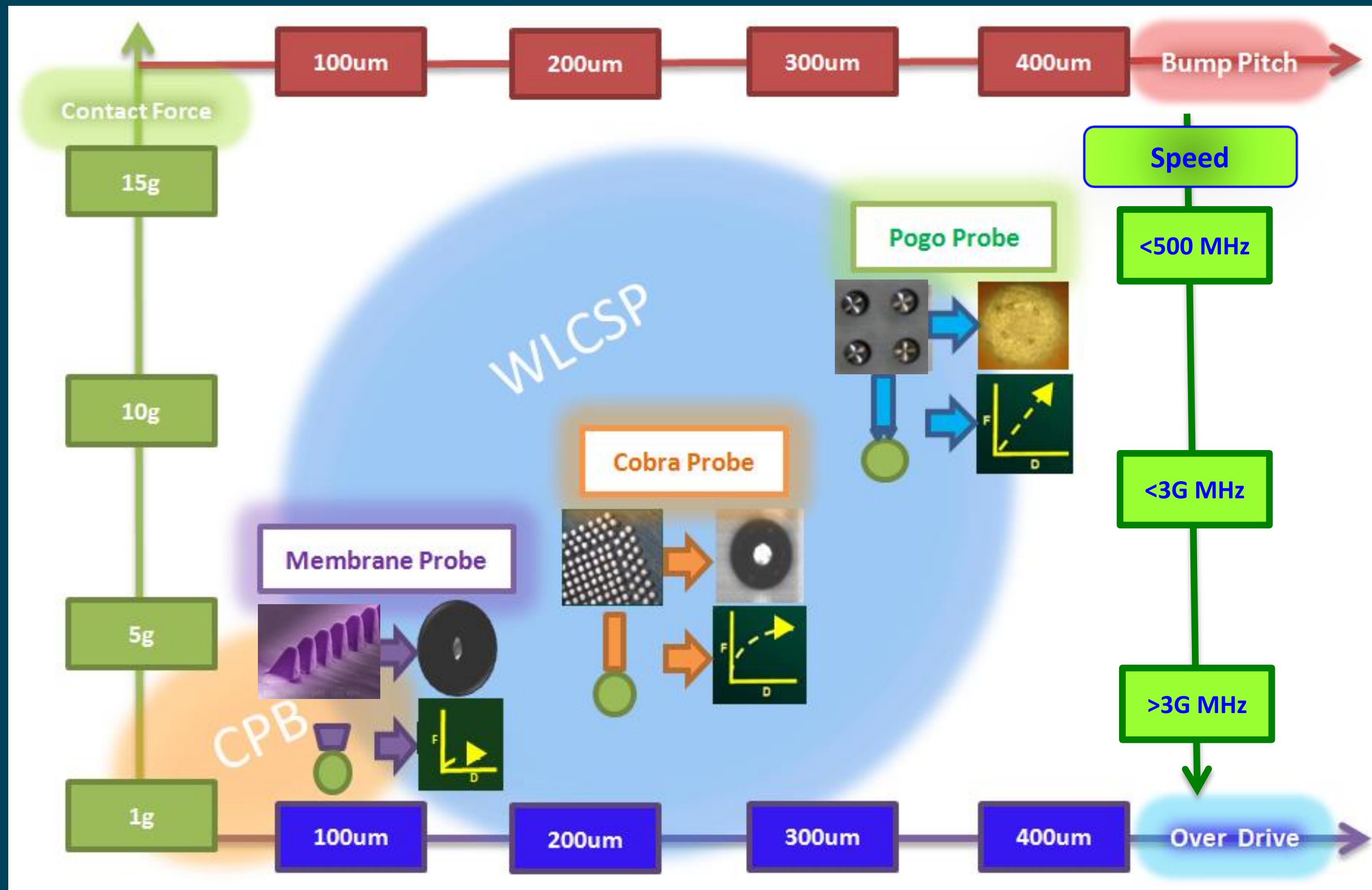
- Cycle Time Challenge
- Cost Challenge
- New Process Challenge

- Cooperation Model Challenge
- Wafer Level Business and Quality Requirement

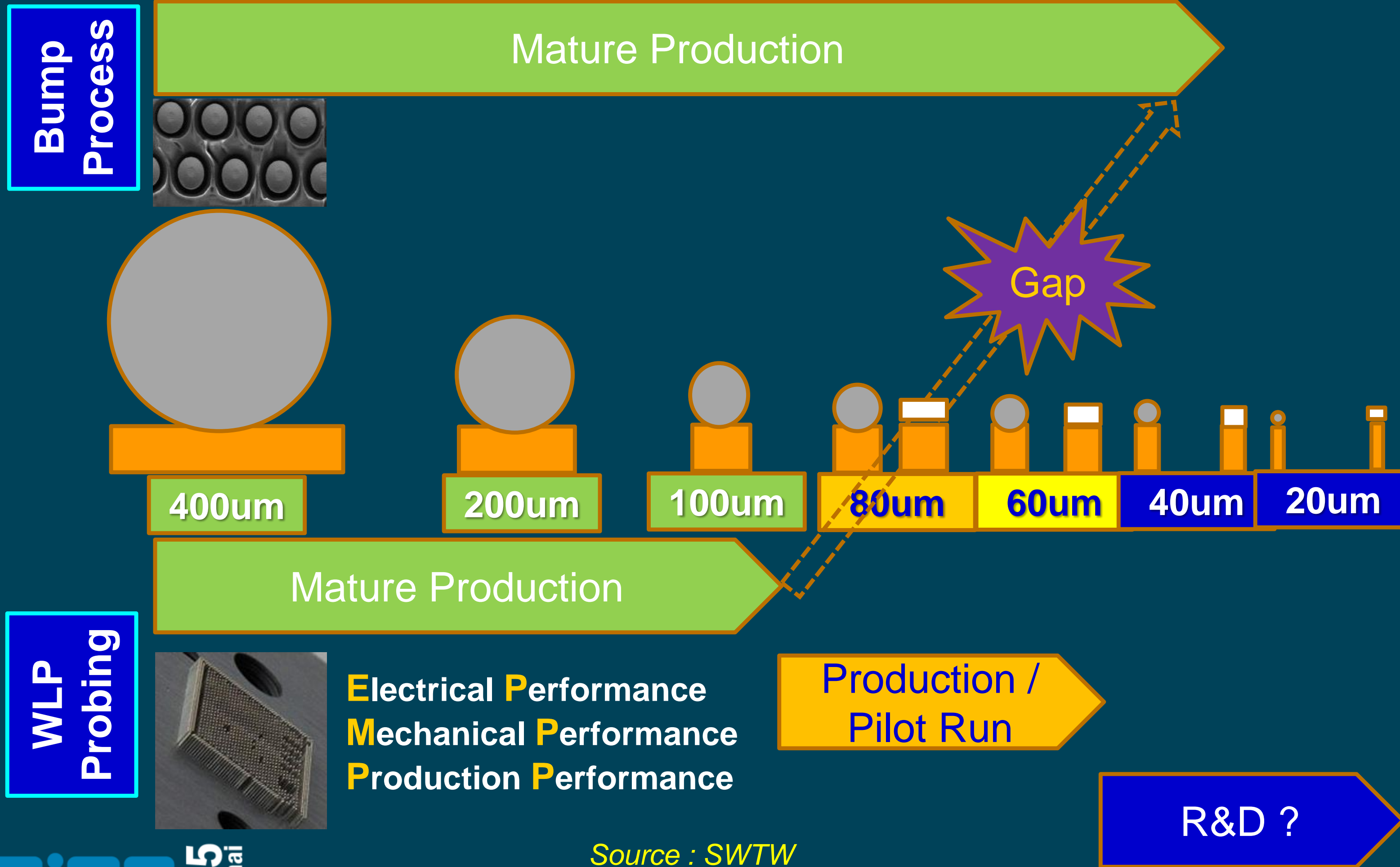


Source : Mitsubishi

WLCSP / CPB Probe Card Roadmap



Source : SWTW


Bump _ CPB Process & Probing Roadmap
Bump Process
Mature Production
Gap
400um
200um
100um
80um
60um
40um
20um
Mature Production
WLP Probing
Electrical Performance
Mechanical Performance
Production Performance
Production / Pilot Run
R&D ?
Source : SWTW
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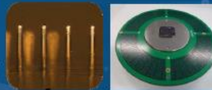
uBump for 25um Probing Challenges

Case 2: 40 µm pitch direct µbump probing
IMEC – Technoprobe - TEL

- **Imec's Blanket Micro-Bump (BMB) Design**
  - Includes JEDEC WIO2 foot-print (40 µm pitch)
  - Micro-bumps: ∅ 25 µm Cu and ∅ 15 µm Cu/Ni/Sn

- **Technoprobe's Probe Technology**
  - FT1.0 vertical needles, micro-wired space transformer
  - Probe card with single-bank WIO2



- **Test Equipment @ imec**
  - TEL P-12XLm automatic probe station
  - Agilent 4073 parametric tester
- **Evaluation Criteria**
  - Contact resistance (C_RES)
  - Probe marks

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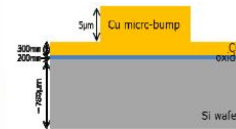
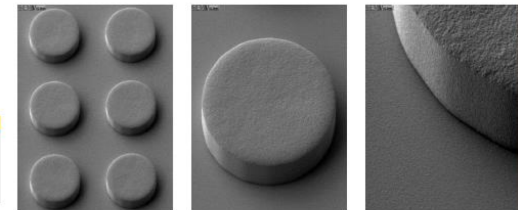
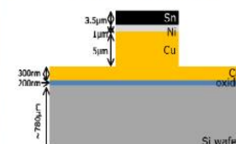
Case 2: 40 µm pitch direct µbump probing
Blanket Micro-Bump Wafers

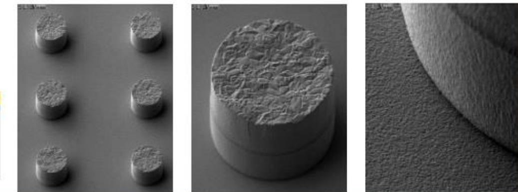
- ∅ 25µm Cu
- (10nm NiB coating)





- ∅ 15µm Cu/Ni/Sn





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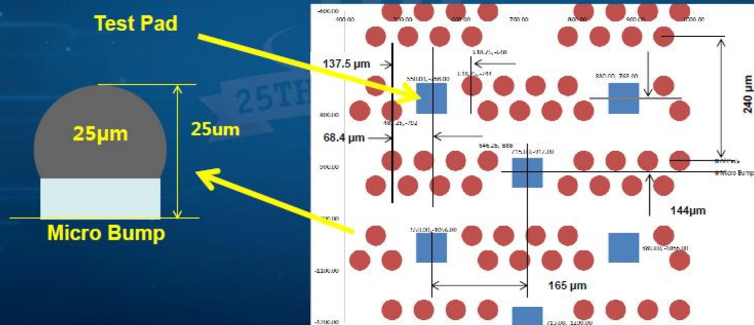
Source : SWTW 2015 IMEC/Technoprobe/ITS

HBM for 25um Probing Challenges

HBM Stack Probing

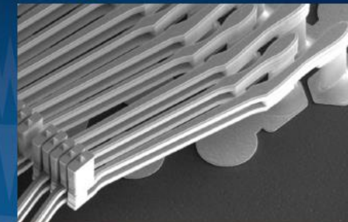
- Bottom of SoC device in the stack provides test pads in the field of Micro bumps

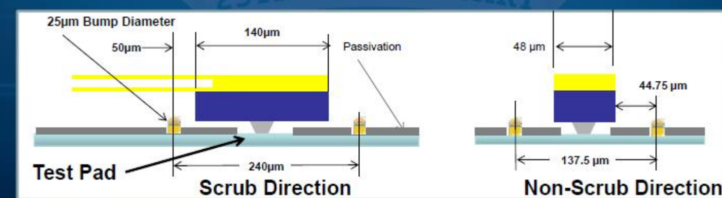


Marc Loranger
John Oonk
June 7-10, 2015 SW Test Workshop 7

Probing challenges

- Challenges:
  - Probe without damaging Micro Bumps
    - No issue with FormFactor MicroSpring®





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Source : SWTW 2015 FFI

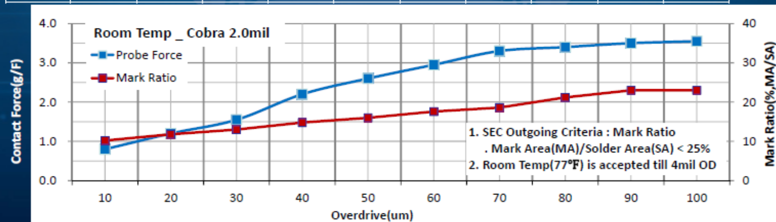
CPB for 50um Probing Challenges

Evaluation result by using wire type

F. Tip Force & Optical Mark Image(For TCFC Type)

Cu-P Diameter : 50um

Temp	10um	20um	30um	40um	50um	60um	70um	80um	90um	100um
Room	10.2%	11.8%	13.0%	14.8	16.0%	17.6%	18.6%	21.2%	23.0%	23.0%
Hot	10.2%	12.5%	14.4%	19.4%	21.2%	23.0%	27.0%	31.4%	33.6%	36.0%



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Process change for cost reduction

Present Process	New Process
Plate	Plate
Reflow	WLT
AVI	Reflow
WLT	AVI

SnAg
Copper

Before Reflow

After Reflow

Source : DIPSOL Website Figure
http://www.dipsol-jp.com/wp-content/uploads/

Type	Cres	Tip Force	Life Time
MEMS Flat	Bad	Good	Good
MEMS Point	Good	Good	Bad
Wire Point	Good	Middle	Bad
Cobra Flat	Bad	Bad	Good

- Table data is expectation grade (SEC Simulation)
  → Next Step Study

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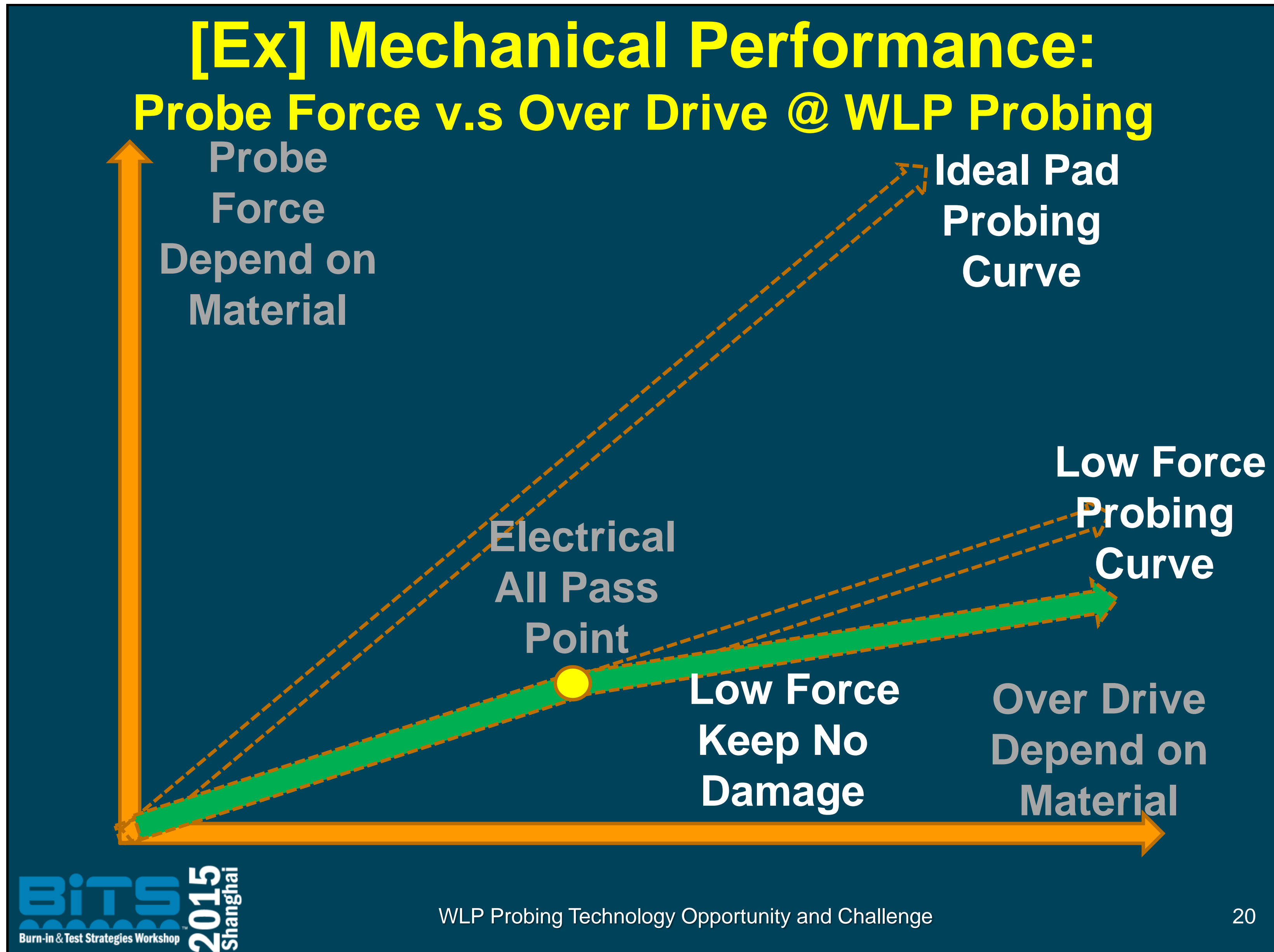
Source : SWTW 2015 Samsung


[Ex] Mechanical Performance:
Probe Force v.s Over Drive @ WLP Probing
Probe Force Depend on Material
Ideal Pad Probing Curve
Low Force Probing Curve
Electrical All Pass Point
Low Force Keep No Damage
Over Drive Depend on Material
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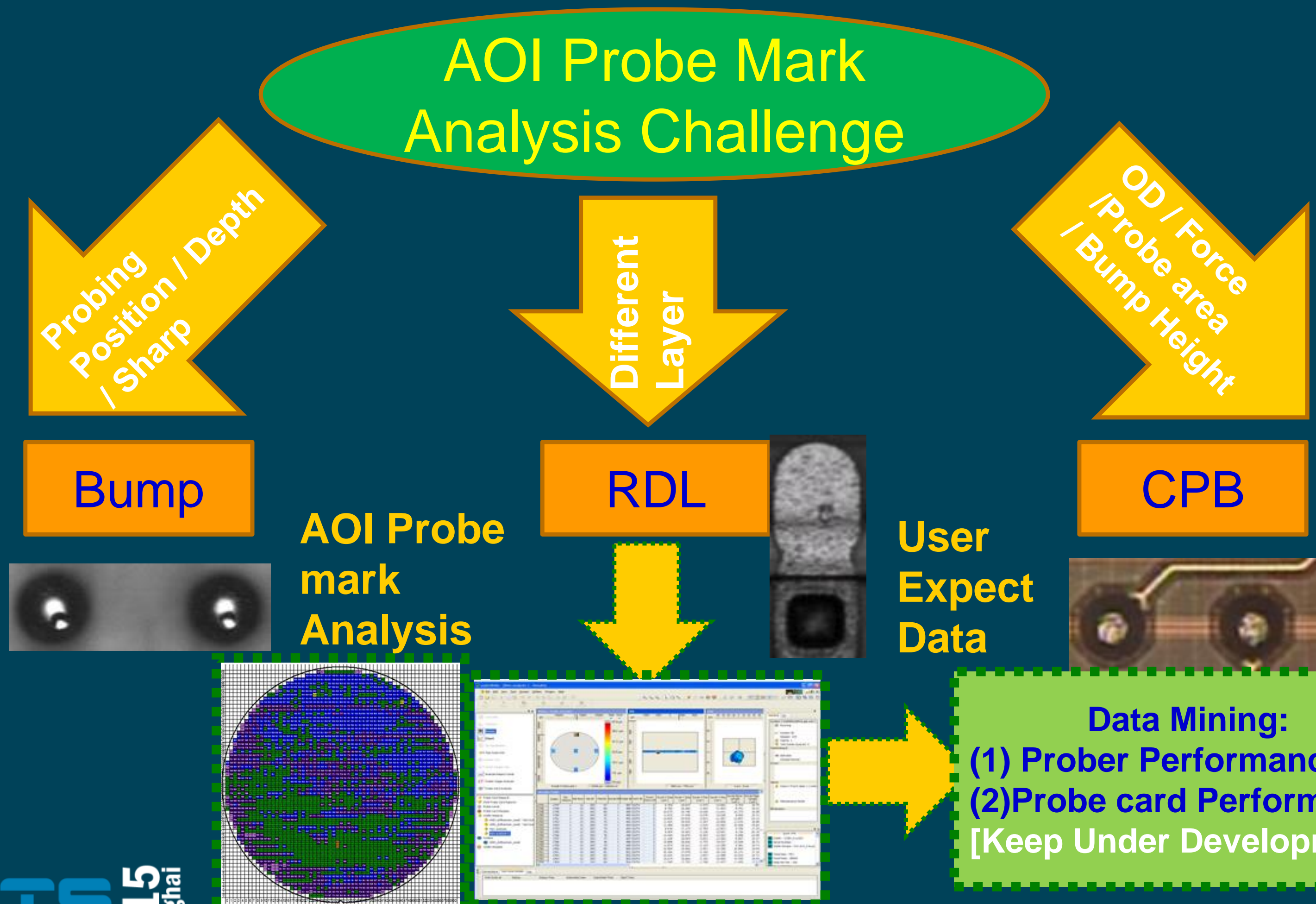
Case 3: Probe mark analysis Technology
AOI Probe Mark Analysis Challenge
Probing Position / Depth / Sharp
Different Layer
OD / Force /Probe area / Bump Height
Bump
RDL
CPB
AOI Probe mark Analysis
User Expect Data
Data Mining:
(1) Prober Performance
(2)Probe card Performance
[Keep Under Development]
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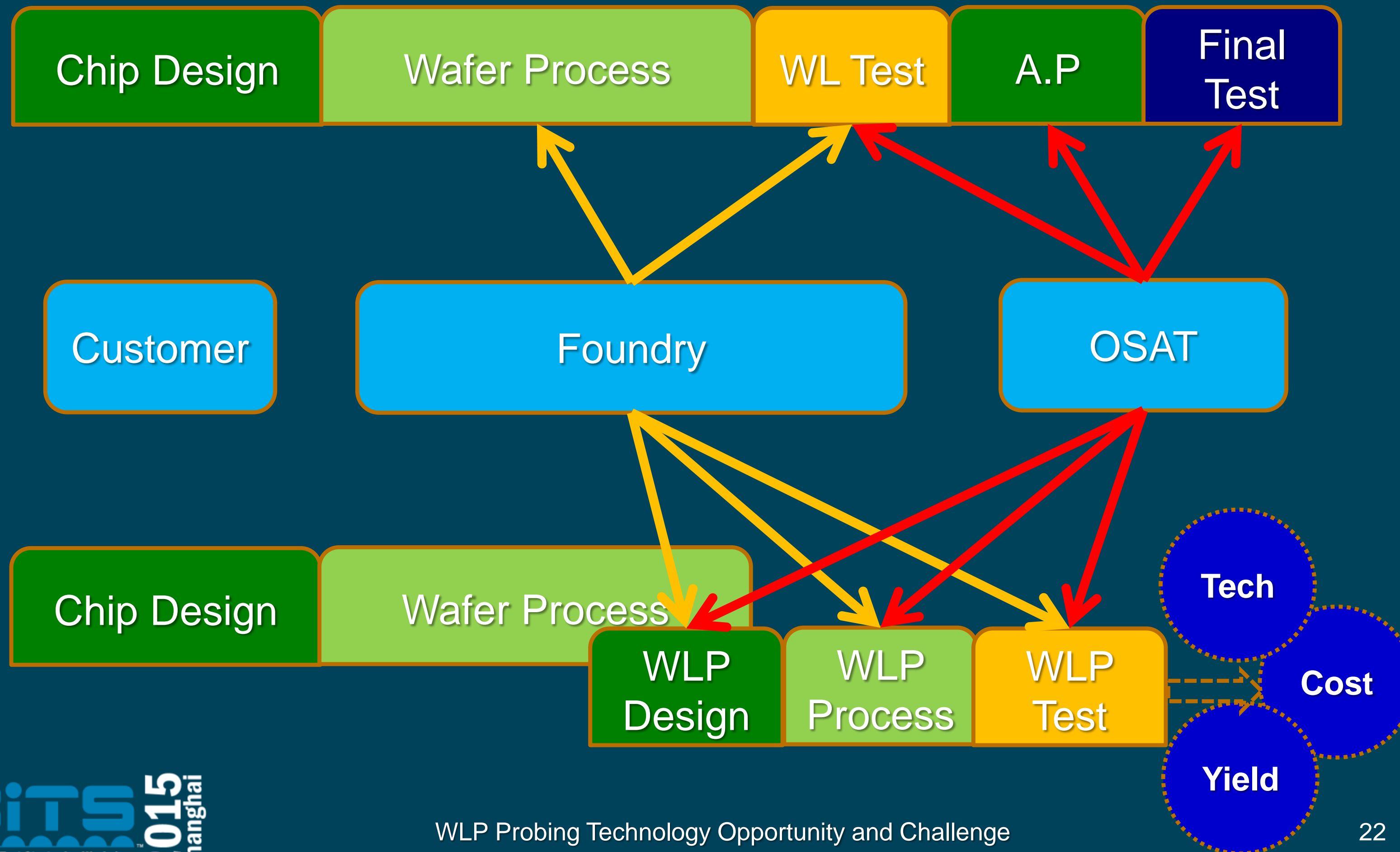
Case 4: Business or Process Change?
Chip Design
Wafer Process
WL Test
A.P
Final Test
Customer
Foundry
OSAT
Chip Design
Wafer Process
WLP Design
WLP Process
WLP Test
Tech
Cost
Yield
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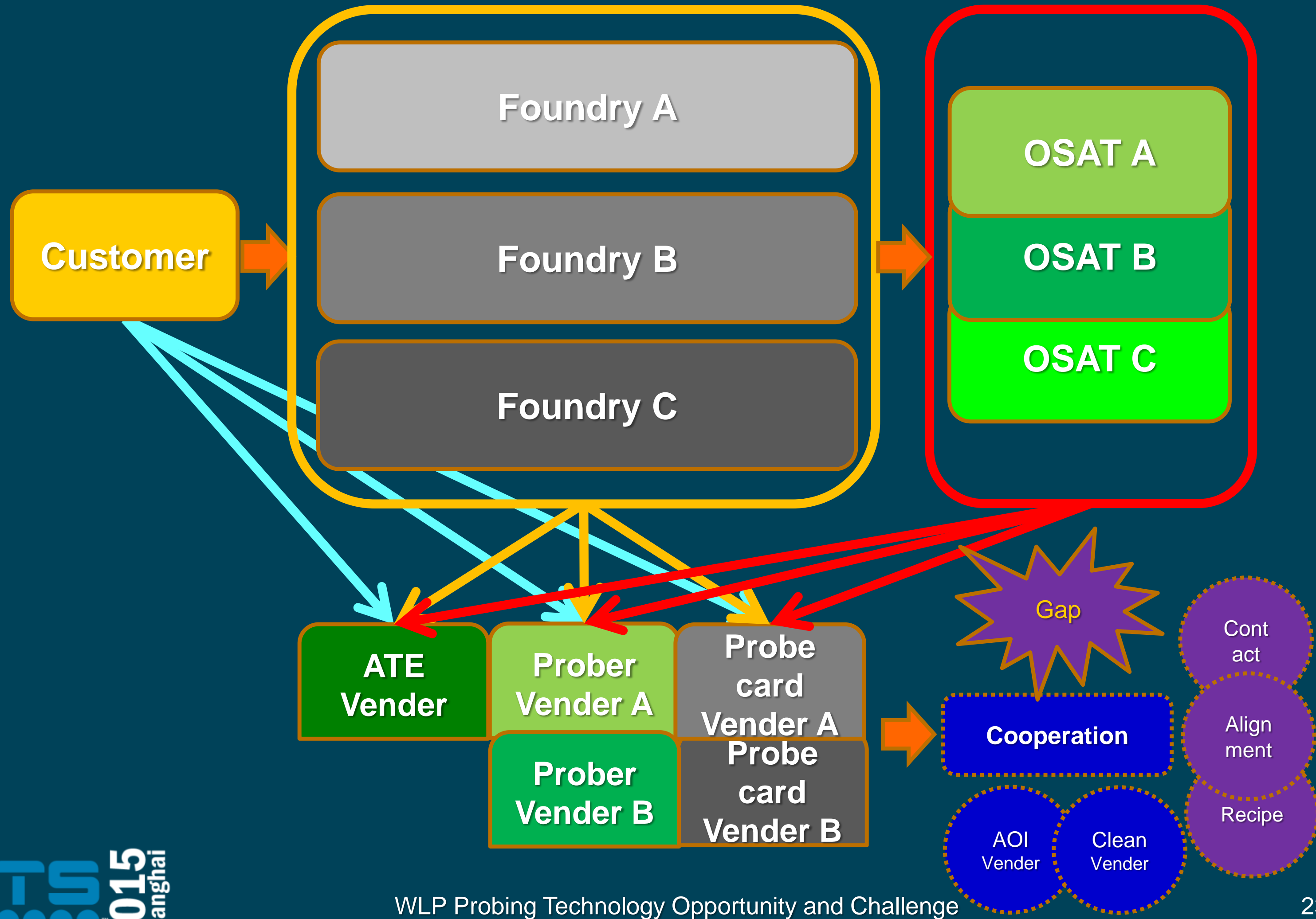
SCM: Same Issue but different site?
Foundry A
Foundry B
Foundry C
Customer
OSAT A
OSAT B
OSAT C
ATE Vender
Prober Vender A
Prober Vender B
Probe card Vender A
Probe card Vender B
Gap
Cooperation
Cont act
Align ment
Recipe
AOI Vender
Clean Vender
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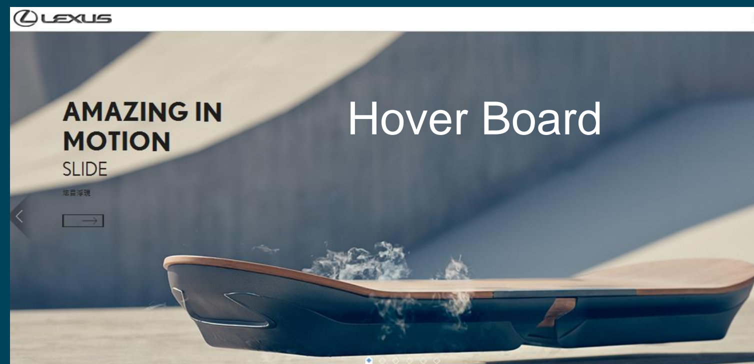
Conclusion



- Cooperation from Customer to Equipment Supplier (Design House /Foundry/OSAT/Vender).
- New opportunity for Wafer/Final Test I/F Suppliers.
- The Evolution Business Model will start changing.

Source : Google/Lexus