

Burn-in & Test Strategies Workshop

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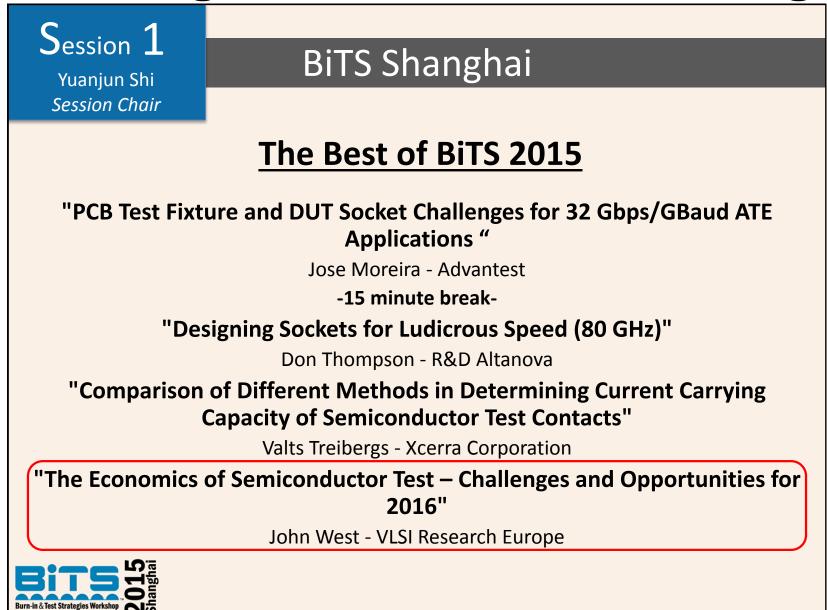
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The Economics of Semiconductor Test Challenges and Opportunities for 2016

John West VLSIresearch



2015 BiTS Workshop Shanghai October 21, 2015



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Overview

- What's happening now?
- What's next?
- How will this impact the cost of test?
- Review



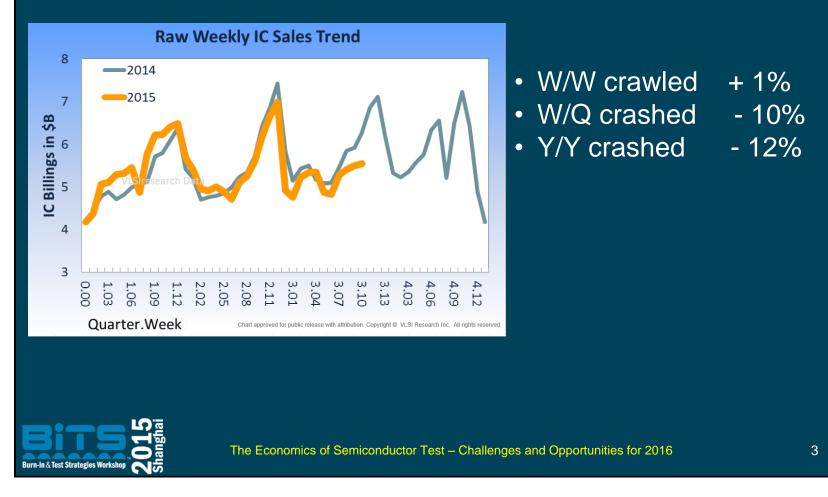
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Semiconductors – Into Negative Territory

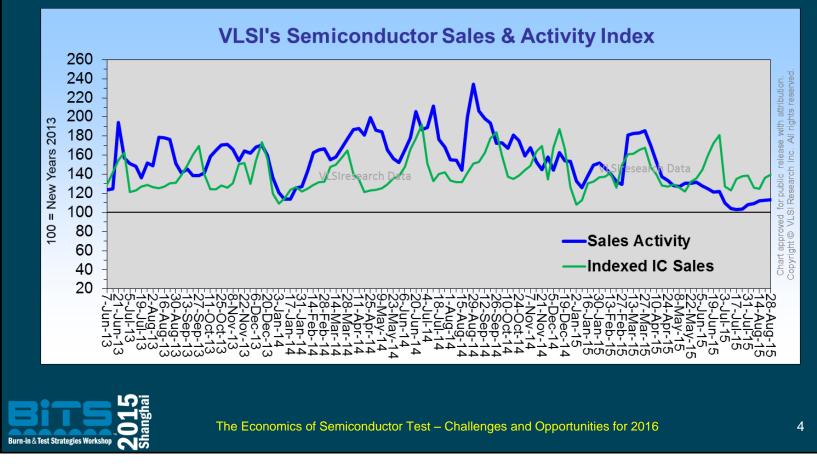
Raw IC Sales: weekly data for 2015 mapped over 2014



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Semiconductors – Into Negative Territory

Trending down since August 2014



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Key Indicators

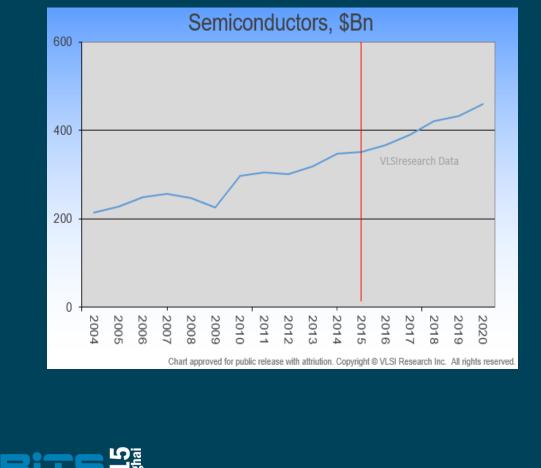
- Inventory to billings ratio for semiconductors trending upwards to 1.5 months
- Chip prices falling rapidly after 2 years' stability
- Peak capacity utilization rate reached 90% this summer, compared to 95% in 2014



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Industry Growth – Needs a New Driver



2015 is flat at 0.7% 2016 up 4.4%

Long-term Growth 5.6%

Electronics Demand Weak: last 4 years below long term trend

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Next generation devices to drive near term growth..

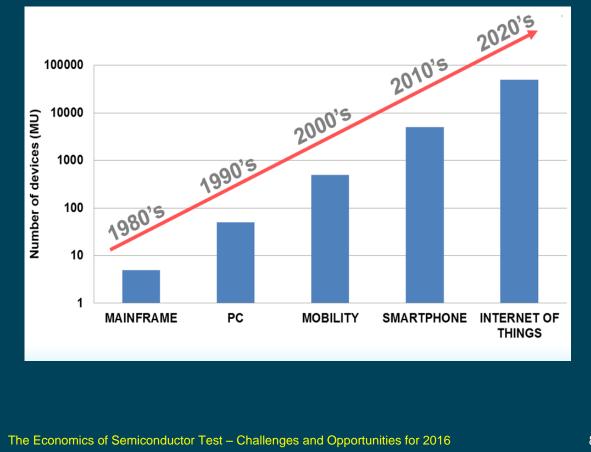
- Server/High Performance Computing
 - ARM based devices
- Personal Computing
 - Merging Tablet and PC
- Communications
 - 4G LTE
 - Expansion to mid-tier phones
 - Network upgrades
 - 64bit Application processors
 - Next Gen WLAN
 - Next Generation PCI Express



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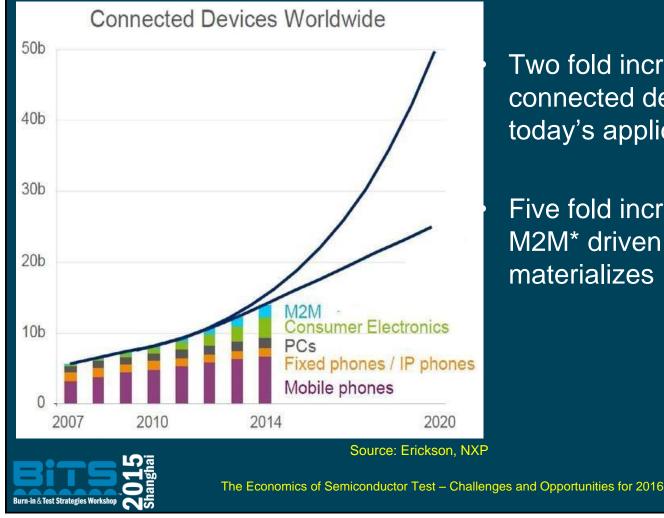
The power of 10 required to drive next wave of growth



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Volume of Devices Will Explode

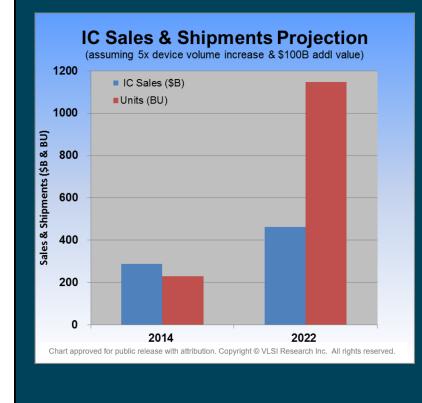


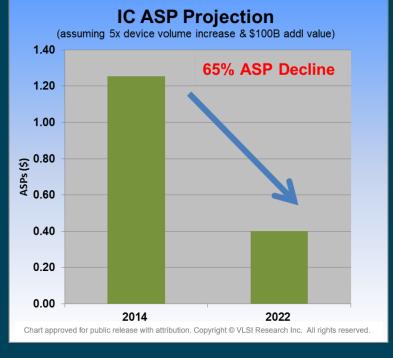
Two fold increase in connected devices in today's applications

Five fold increase, if M2M* driven expansion materializes

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IC ASPs Have to Be Significantly Lower







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Lower ASP's Impact on Manufacturing

INDUSTRY ECONOMICS

- Moore's law has to continue
- Productivity gains have to continue
 - Higher throughputs
 - Better yields
 - Improved Time-to Market
 - Bigger factories
- Industry concentration
- 450mm

TEST ECONOMICS

- Better, faster, cheaper testers
 - Burden on Test OEMs
- Better, faster, cheaper DFT
 - Burden on internal test development
- Higher level of parallel testing
 - Multi-wafer production test?
 - Higher level parallelism at package test



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Two Test Challenges for IoT

How to test all of the IoT devices at low cost?

How to test the high end devices for cloud infrastructure?

- Very large volumes
- Short test times
- Leadless packages
- Small die sizes
- Highly efficient manufacturing
- Wide range of products –
 ICs, MEMS, Sensors, etc
- Time to Volume

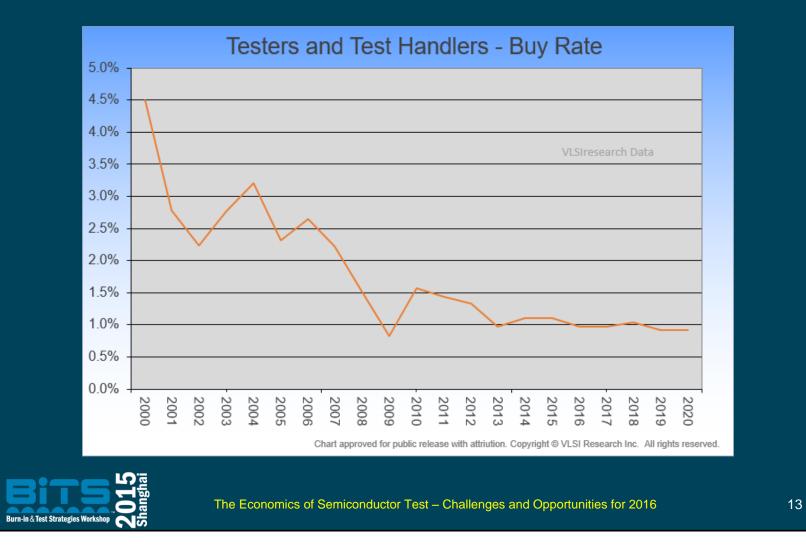
- 20nm and below devices
- 3D integration
- Highly customized manufacturing
- Time to Quality -> Ramp Risk



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Spending on Test Equipment is Not Growing..



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How is This Possible?

Parallel Test

Modular Testers

Design For Test

Increased use of OSATS - higher utilization rates and lower costs

Consolidation – ATE vendors and Chipmakers

Probe Cards and Load Boards with Higher Functionality

But other (difficult to quantify) costs are growing...

Systems test, software, and overtime



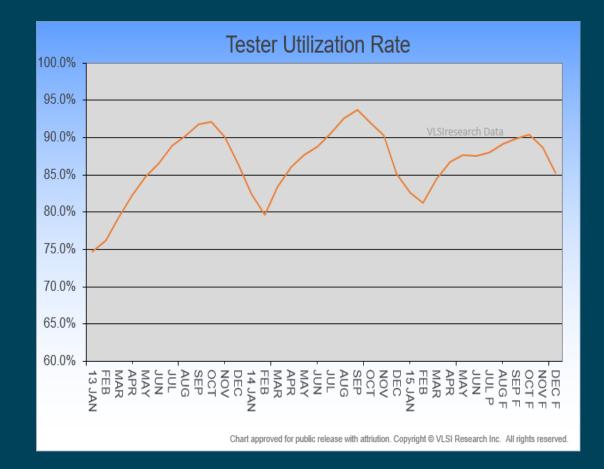
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Tester Utilization

Consistently above 80%

Enabled by OSATS and flexible test platforms





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Consolidation

Top 5 ATE companies account for 88% of market in 2014

Advantest and Teradyne account for 78% of total test sales

Xcerra, DGC Systems and SPEA combined make up the next 10%

35 other suppliers provide the remaining 12%

Chipmakers Consolidating too:

Intel / Altera NXP / Freescale Cypress / Spansion Qualcomm / CSR Avago / LSI / Broadcom? Triquint / RF Micro Infineon / International Rectifier Others...



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Test Consumable Costs Going Up...

Probe Card, Socket and Interface Board Costs causing concern with chipmakers.

Not just cost issues. Chipmakers often have to accept a lower level of performance than they would like at the leading edge.

Long lead times for probe cards and interface boards

But consumables do add functionality to ATE



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Test Consumables, \$M 1750 1500 1250 1000 750 500 Probe Cards 250 Test & Burn-In Sockets Interface Boards 0 200 2002 2004 200 2000 200: 2008 2009 2018 2005 2006 2010 2012 2013 2014 2015 2016 2017 2019 Chart approved for public release with attribution. Copyright © VLSI Research Inc. All rights reserved

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Semiconductor Test in China

Chinese OSATs

JCET in top 10 Others gaining share

5% of probe cards going to China

10% of test and burn-in sockets going to China

Expect trend to continue as cost pressure increases and more chips made in China



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Challenges and Opportunities

Usual issue: overall cost of test is going up

Some costs hard to measure for the industry as a whole what is the right amount to spend on test?

Not helped by restricted information transfer and lack of transparency between companies in the supply chain

No one has all the solutions and it's a problem for everyone - big and small

Test is getting more difficult...

...so developing the right test strategy and right partners is more critical than ever



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