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Session 1
Yuanjun Shi
*Session Chair*

BiTS Shanghai

# The Best of BiTS 2015

**"PCB Test Fixture and DUT Socket Challenges for 32 Gbps/GBaud ATE Applications "**

Jose Moreira - Advantest

**-15 minute break-**

**"Designing Sockets for Ludicrous Speed (80 GHz)"**

Don Thompson - R&D Altanova

**"Comparison of Different Methods in Determining Current Carrying Capacity of Semiconductor Test Contacts"**

Valts Treibergs - Xcerra Corporation

**"The Economics of Semiconductor Test – Challenges and Opportunities for 2016"**

John West - VLSI Research Europe

BiTS Burn-in & Test Strategies Workshop 2015 Shanghai

# PCB Test Fixture and DUT Socket Challenges for 32 Gbps/Gbaud ATE Applications

超高速信号(32Gbps/Gbaud)的测试: 电路板与测试基座的设计与挑战

**Jose Moreira[1], Christian Borelli[2], Fulvio Corneo[2]**
[1]Advantest, [2]STMicroelectronics

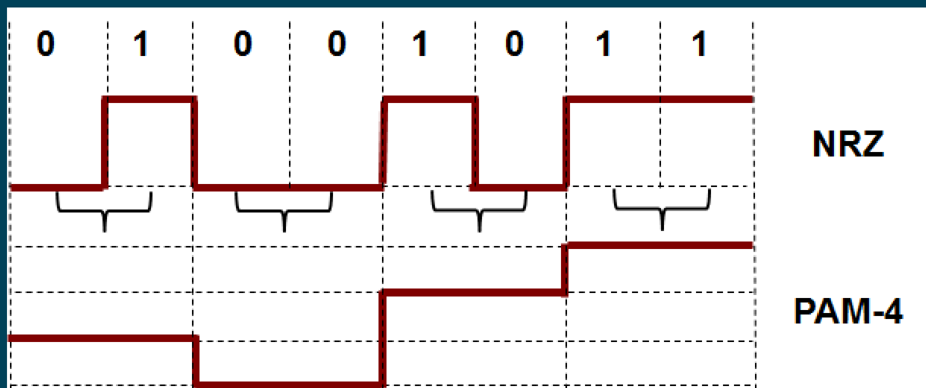
2015 BiTS Workshop
Shanghai
October 21, 2015

## Presentation Outline

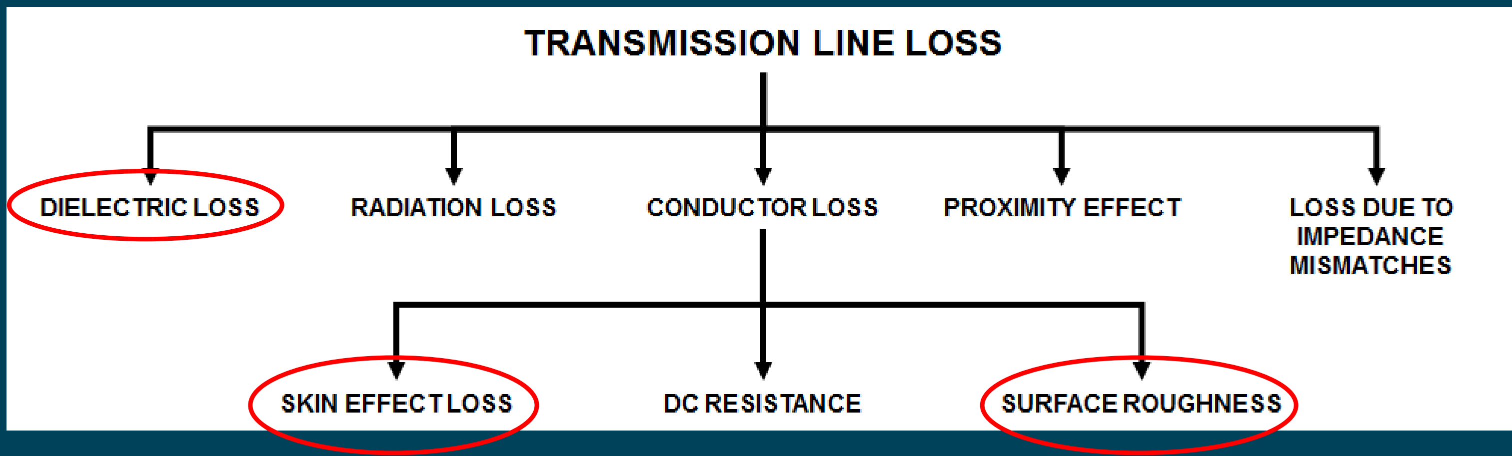
- 32 Gbps/Gbaud ATE Challenges
- PCB Signal Trace Loss and DUT Socket Impact
- Example of a 28/32 Gbps ATE Test Fixture and Measurement Solution
- DUT Socket Challenges
- Measurement Results
- Conclusions

# 32 Gbps/Gbaud Test Fixture Challenges

- with standards like 100Gb Ethernet pushing for higher bandwidths, 25-32 Gbps applications are now reaching volume production on Automated Test Equipment (ATE)
- even when using external loopback in volume production, the DUT socket can be critical
- multi-level signaling like PAM-4 is now being considered at 32 and 56 Gbaud data rates. The challenges will be tougher than with NRZ signaling due to the degradation in signal to noise ratio

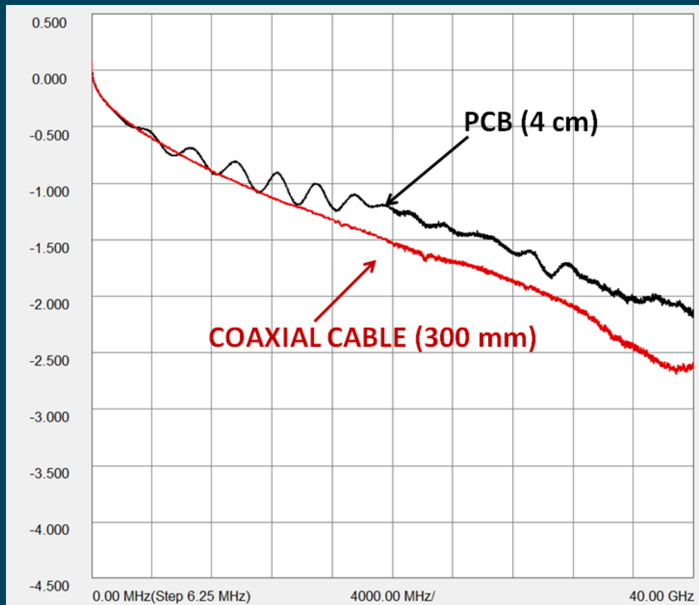


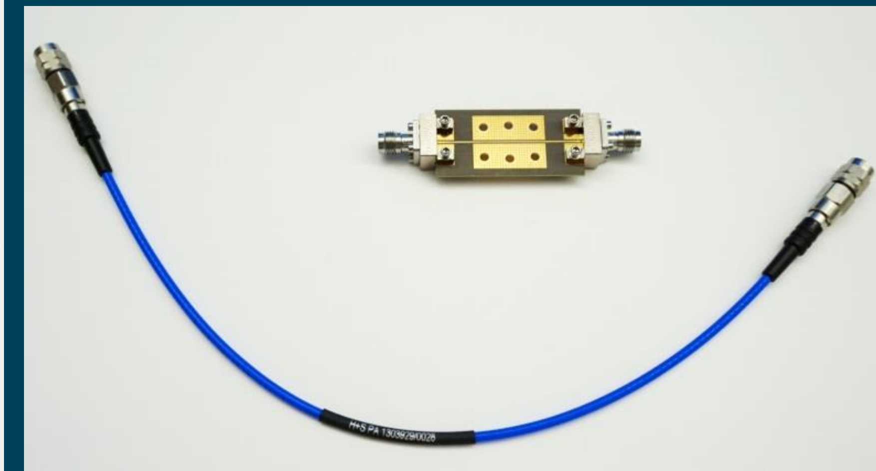
# PCB Signal Trace Loss Factors




- surface roughness becomes an important factor for 25-32 Gbps test fixtures. It was not at 10 Gbps
- equalization becomes even more important to compensate for the signal path loss

# Coaxial vs PCB Signal Trace

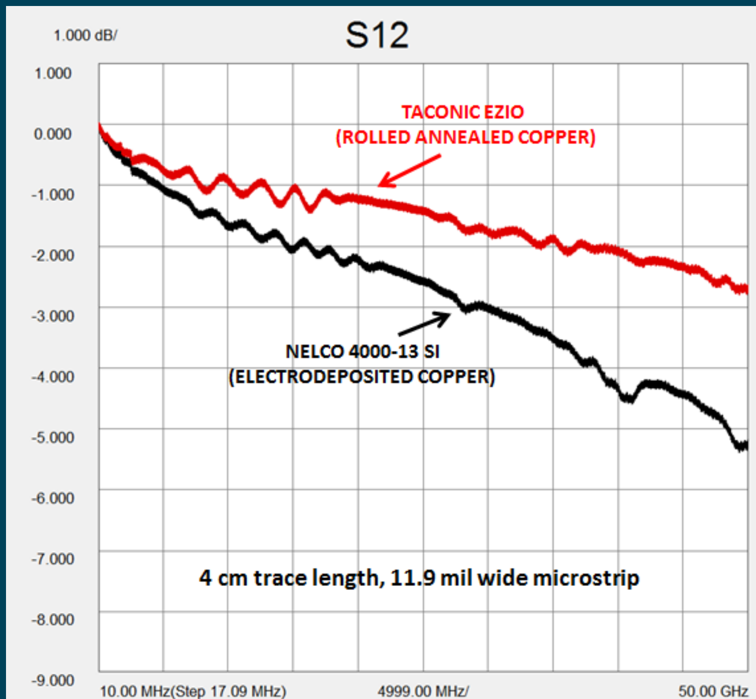


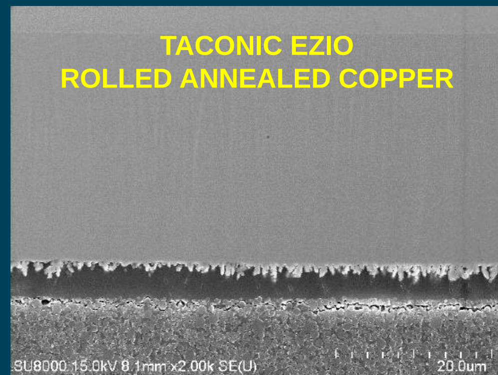



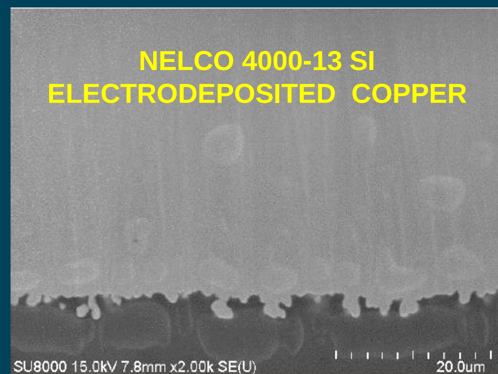
- **PCB signal trace loss is critical. If possible use coaxial cabling as much as possible to keep the PCB trace loss to an absolute minimum**

# We Cannot Buy Our Way Out of The Signal Trace Loss Problem

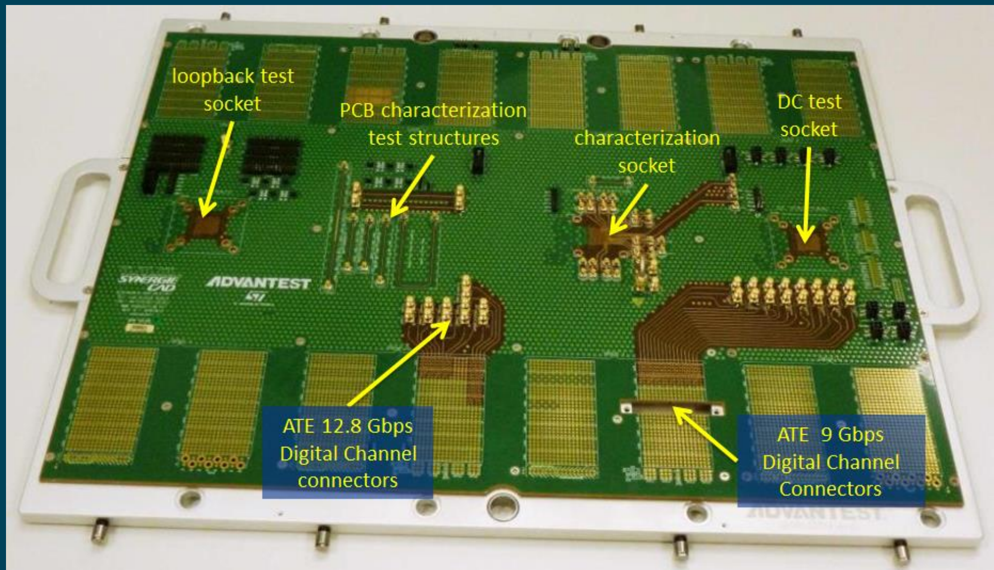
- PCB technology does not scale like Silicon (e.g. 56 Gbps at 10 nm CMOS)
- there have been advances in dielectric and copper foil technologies but they cannot cope with the data rate increase



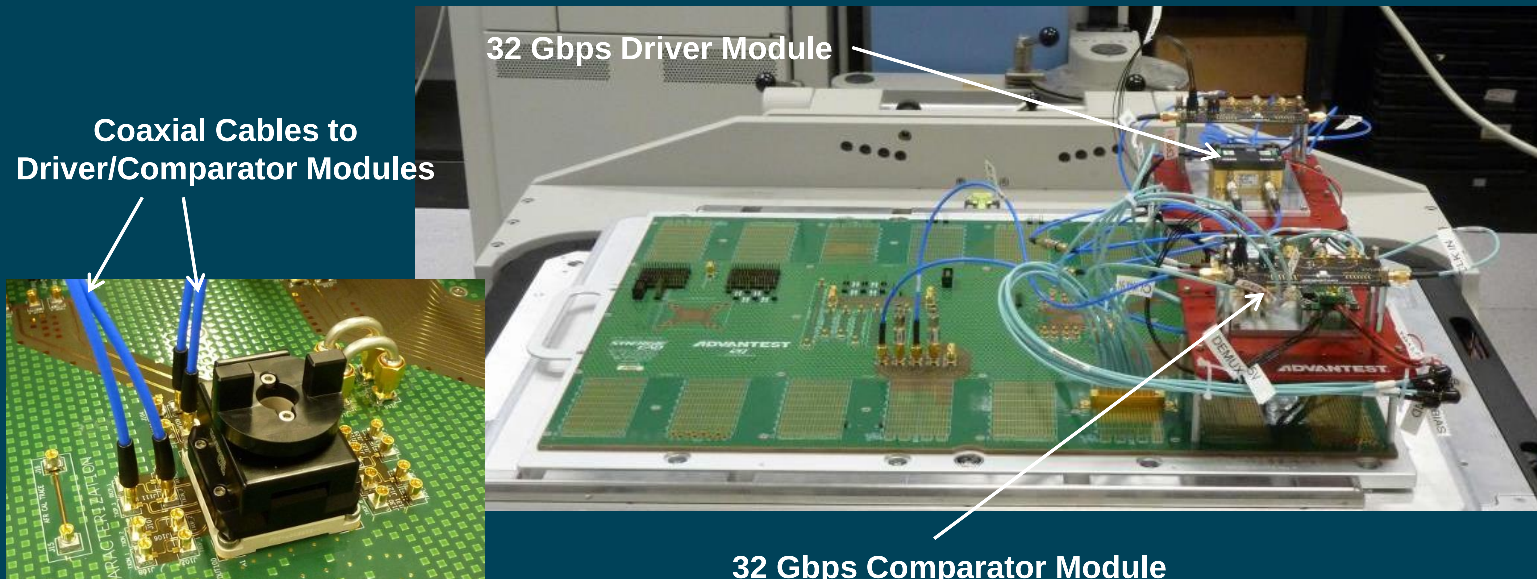
# ATE Test Fixture for 28/32 Gbps Characterization




- **objective is to keep PCB signal traces to a minimum length and transition to coaxial cable as soon as possible**
- **high-speed connectors are MMPX with 3D EM optimized footprint**

**REFERENCE [1]**

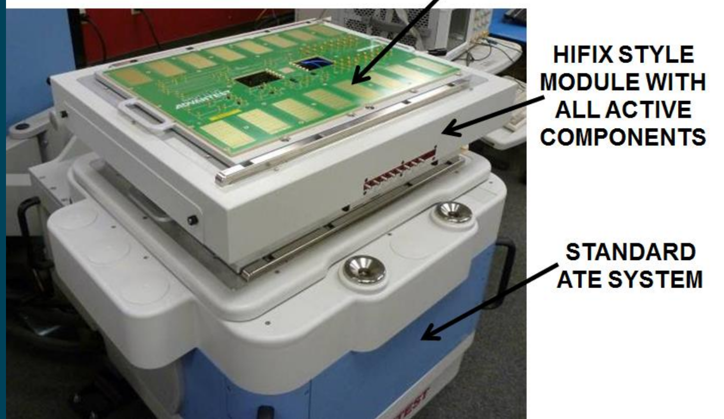
# 28/32 Gbps ATE Characterization Setup

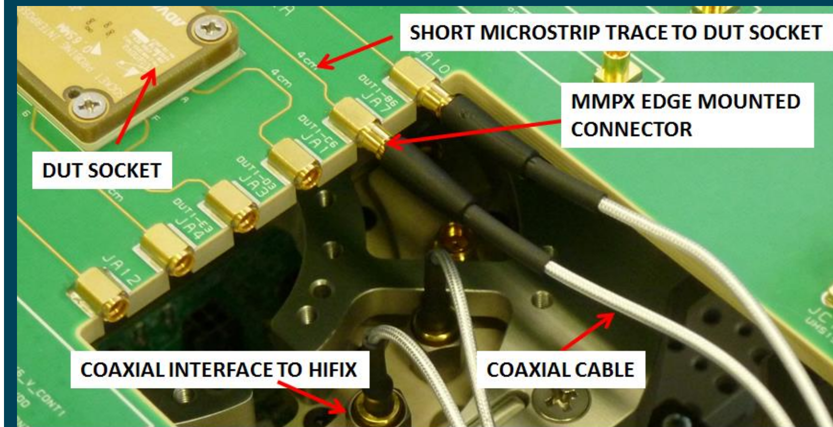



- low cost pragmatic approach for at-speed characterization for data rates of 28/32 Gbps and above
- excellent signal integrity because most of the signal path is coaxial cable with a very short stripline

REFERENCE [1]

# 28/32 Gbps Production Setup

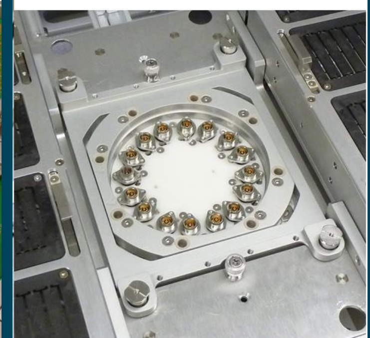



- good signal integrity by continuing to keep PCB signal trace length to a minimum
- production worthy, handler/prober integration possible
- coaxial blind mating interconnect interface

TEST FIXTURE SIDE

HIFIX SIDE

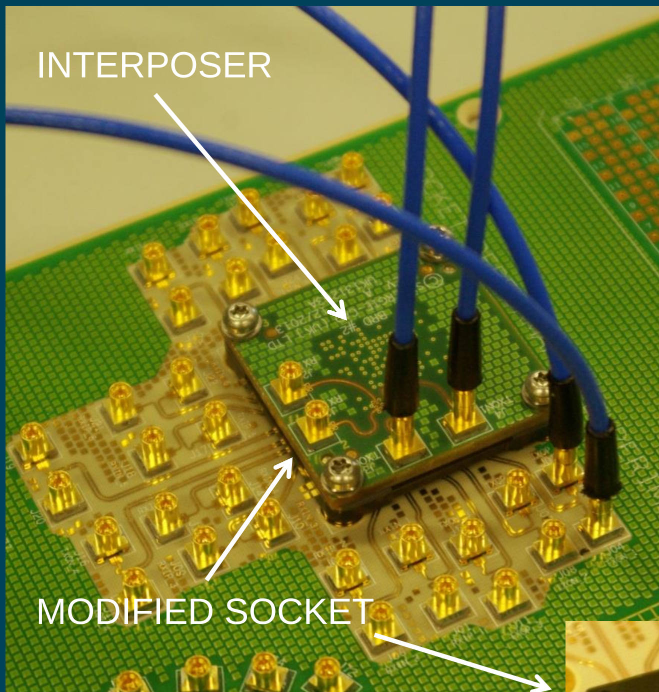


REFERENCE [1,7,8]

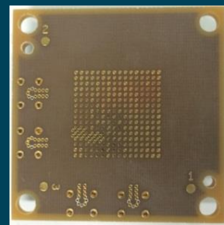
# Socket Technologies

- socket technologies for high-speed digital applications can be divided into three main categories:
  - **Standard Pogo Pin (everyone likes it, cheap and reliable)**
  - **Coaxial Pogo Pin (sounds expensive)**
  - **Elastomeric (great performance but what about volume production?)**
- for high-speed digital applications we need to remember that we can have very large BGAs unlike high-speed memory or RF applications. Socket compliance is critical
- and as always we have the same struggle:
  - **characterization vs production**
  - **performance vs reliability**
  - **low cost (whatever we think is low cost)**

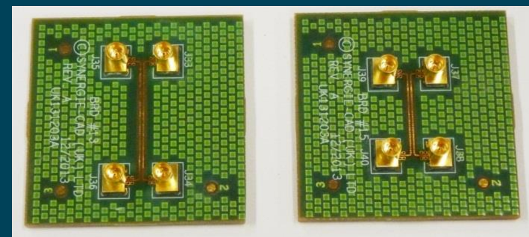
## DUT Socket Evaluation Setup




Interposer Bottom Side

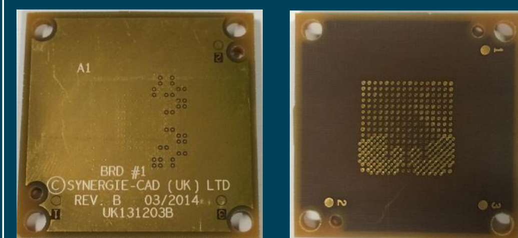


De-Embedding Test Fixture



Different I/O Lane Interposers

Micro-Coaxial Probing Interposer



REFERENCE [2,3,4,5]

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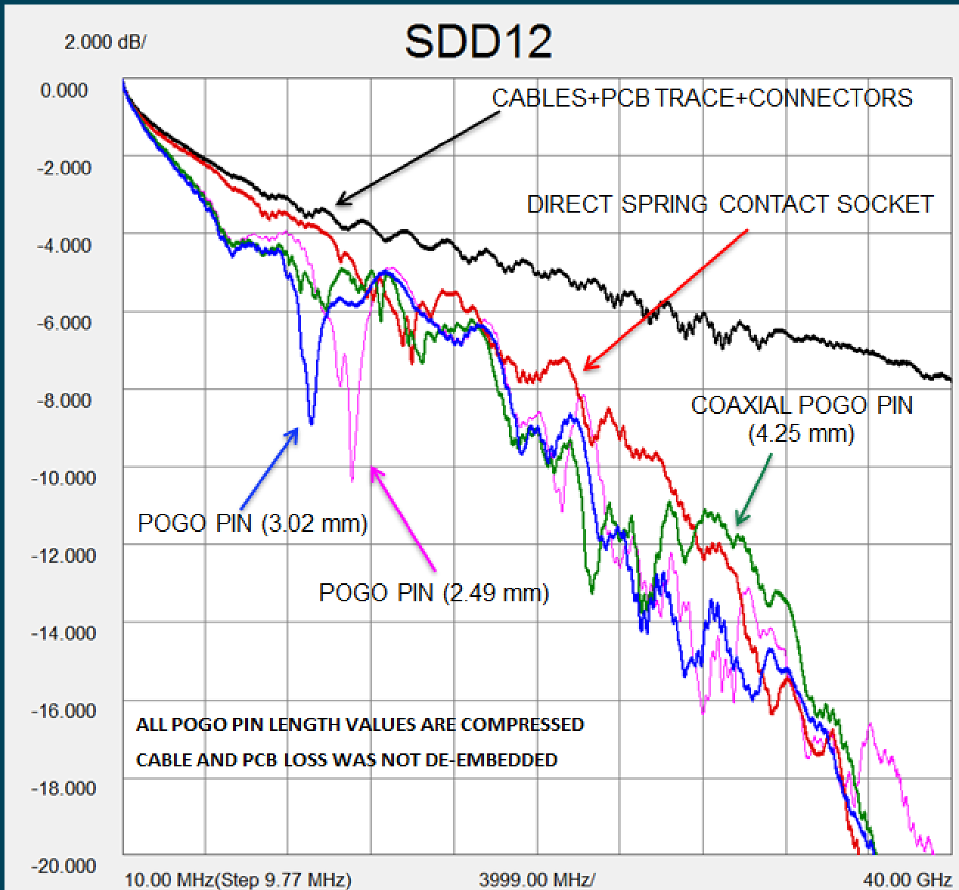
## Socket Measurement Results (TX0)




NO ELASTOMERIC SOCKET IN THIS COMPARISON

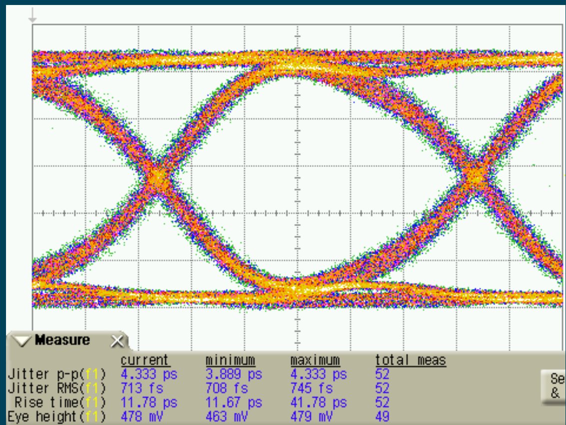
- pogo pin socket shows resonances at 9 GHz and 11 GHz
- the direct spring contact socket presents the best results
- note that this is not a socket only problem. It is a socket plus ballout plus microstrip transition problem

### BGA BALLOUT

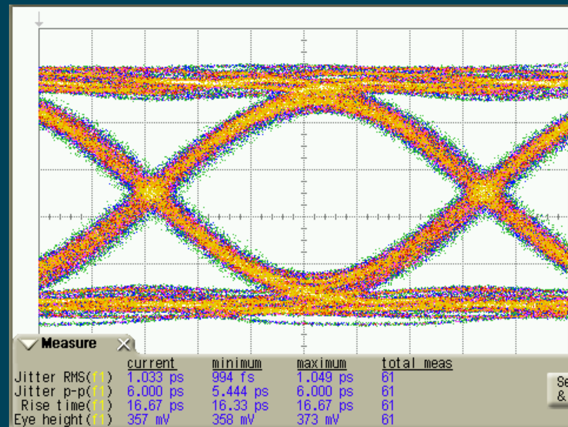
| | | |
|---|---|---|
| DUT PIN | GND | TX1 |
| DUT PIN | GND | TX1 |
| GND | TX0 | GND |
| GND | TX0 | GND |
| GND | POWER | GND |

# 32 Gbps (PRBS7)

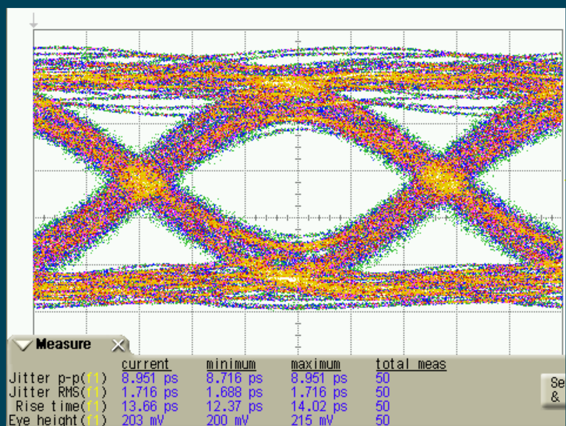
NO SOCKET



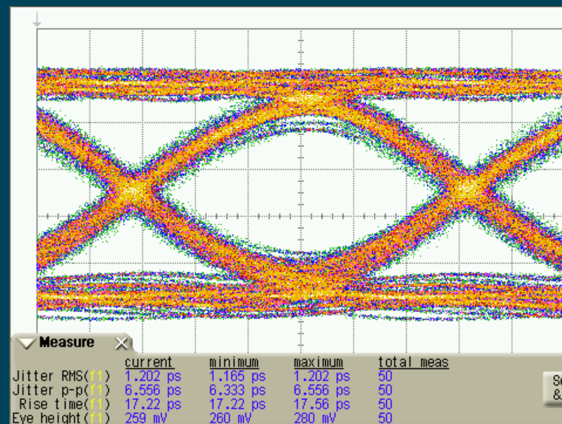

DIRECT SPRING CONTACT SOCKET



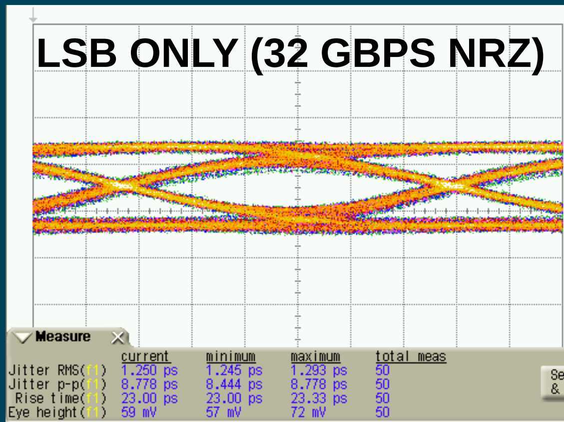

POGO PIN SOCKET (3.02 mm)

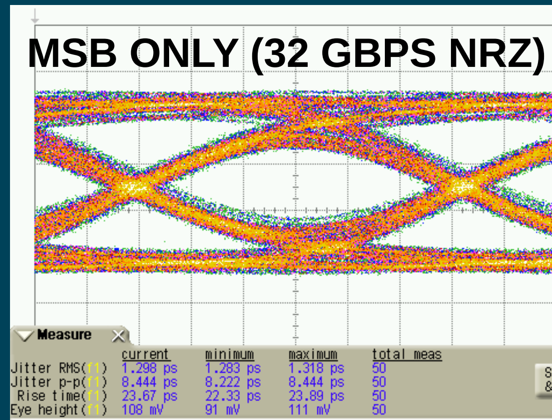


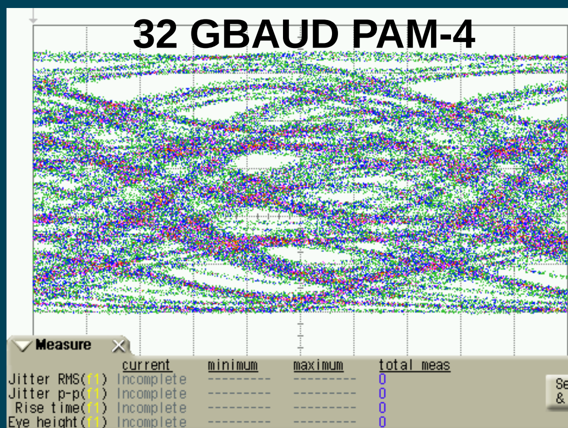

COAXIAL POGO PIN SOCKET

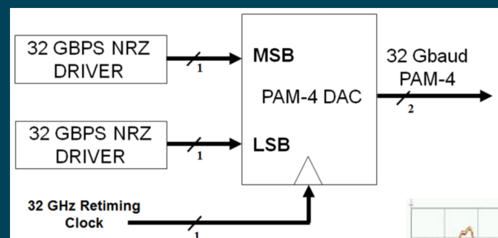


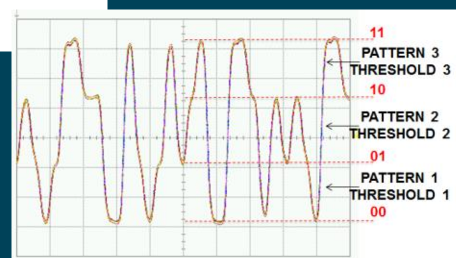
## 32 Gbps is not 32 Gbaud
## (The PAM-4 Signaling Challenge)



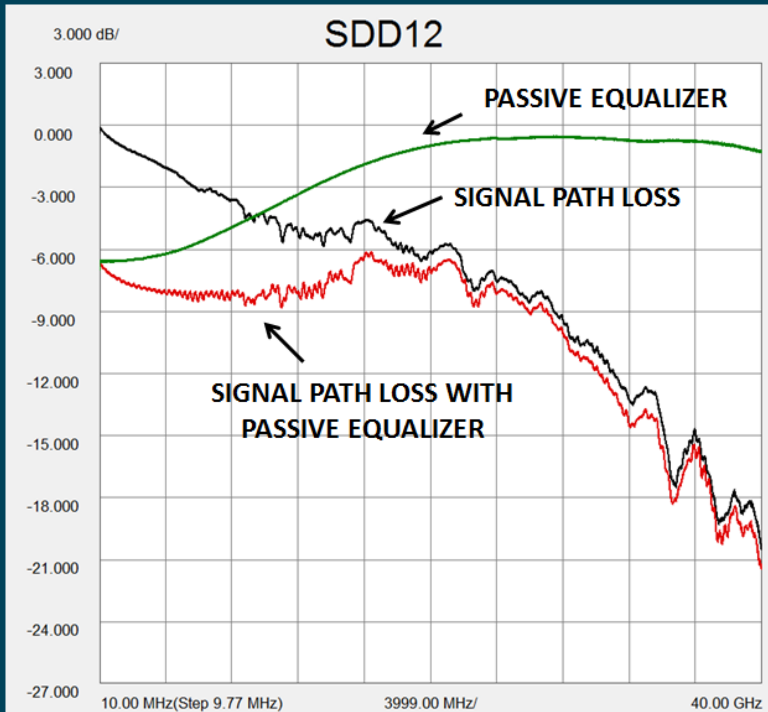



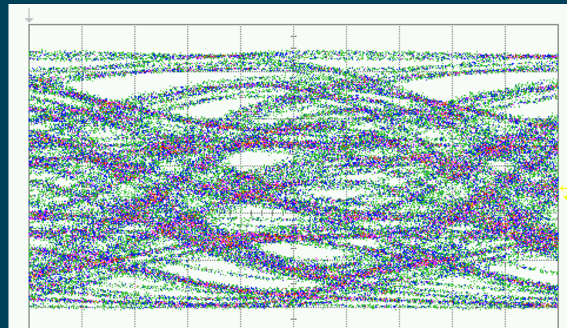

**DIRECT SPRING CONTACT SOCKET**

**REFERENCE [6,7]**

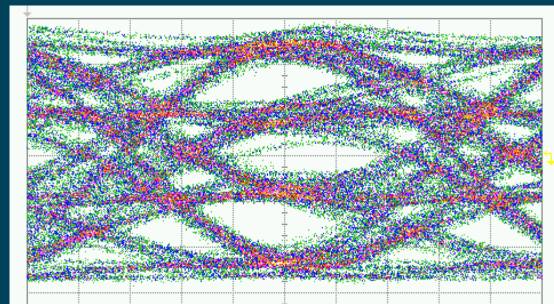
# Equalization To The Rescue (As Always)




32 GBAUD PAM-4 (NO CTLE EQUALIZER)



32 GBAUD PAM-4 (WITH CTLE EQUALIZER)



Designing a CTLE equalizer for 32 Gbps/Gbaud (i.e. DC to e.g. 40 GHz) is far from trivial

REFERENCE [7,8]

# Conclusions

- 25-32 Gbps characterization and production testing requires re-evaluating the test fixture and DUT socket design strategy used for the 10 Gbps I/O generation
- because of the PCB trace loss it is import to keep the signal trace length to a minimum and if possible use coaxial cabling
- for these data rates standard pogo pin type sockets might not be an option
- 32 Gbaub PAM-4 presents tougher signal integrity challenges compared to 32 Gbps NRZ
- and it will only get worse in the future:
  - 56 Gbps NRZ
  - 56 Gbaud PAM-4
  - 100 Gbps NRZ

# References


- [1] Jose Moreira, Fabio Pizza, Christian Borelli, Fulvio Corneo, Hubert Werkmann, Sui-Xia, Daniel Lam, Bernhard Roth, “A Pragmatic Approach for At-Speed Characterization and Loopback Correlation at 28 Gbps“,Advantest VOICE 2014
- [2] Heidi Barnes, Jose Moreira, Abraham Islas, Michael Comai, and Francisco Tamayo-Broes, Orlando Bell, Mike Resso, Antonio Ciccomancini and Ming Tsai, Performance at the DUT: Techniques for Evaluating the Performance of an ATE System at the Device Under Test Socket”, DesigCon 2009
- [3] Heidi Barnes, Jose Moreira, Mike Resso and Robert Schaefer,“ Advances in ATE Fixture Performance and Socket Characterization for Multi-Gigabit Applications”, DesignCon 2012.
- [4] Jose Moreira, “Design of a High Bandwidth Interposer for Performance Evaluation of ATE Test Fixtures at the DUT Socket”, IEEE Asian Test Symposium 2012,
- [5] Jose Moreira and Hubert Werkmann, “An Engineers Guide to Automated Testing of High-Speed Interfaces”, Artech House 2010.
- [6] Jose Moreira, Hubert Werkmann, Masahiro Ishida, Bernhard Roth, Volker Filsinger, Sui-Xia Yang, “An ATE Based 32 Gbaud PAM-4 At-Speed Characterization and Testing Solution”, IEEE Asian Test Symposium 2014.
- [7] Jose Moreira, Hubert Werkmann, Volker Filsinger, Bernhard Roth, “At-Speed Testing of 32 Gbaud PAM-4 Interfaces Using Automated Test Equipment”, DesignCon 2015.
- [8] Jose Moreira, Bernhard Roth, Hubert Werkmann, Lars Klapproth, Michael Howieson, Mark Broman, Wend Ouedraogo and Mitchell Lin, “An Active Test Fixture Approach for 40 Gbps and Above At-Speed Testing Using a Standard ATE System”, IEEE Asian Test Symposium 2013.