
SIXTEENTH ANNUAL
BiTS
TM
Burn-in & Test Strategies Workshop
March 15 - 18, 2015
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 8
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Session 8

Morten Jensen
Session Chair

BiTS Workshop 2015 Schedule

Solutions Day

Wednesday March 18 10:30 am

Looking For That Four Leaf Clover

"A Test-Cell-Solution for 81GHz Automotive Radar ICs"

Jason Mroczkowski, Peter Cockburn, & John Shelley - Xcerra Corporation

"Universal Device Interface DUT Solutions for ATE Test"

Bob Bartlett- Advantest Corporation

"Where No Tester Has Gone Before"

Roger Sinsheimer -Teradyne Inc.

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Where No Tester Has Gone Before

Roger Sinsheimer, PE
Teradyne Inc.

2015 BiTS Workshop
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What was the goal of this project?

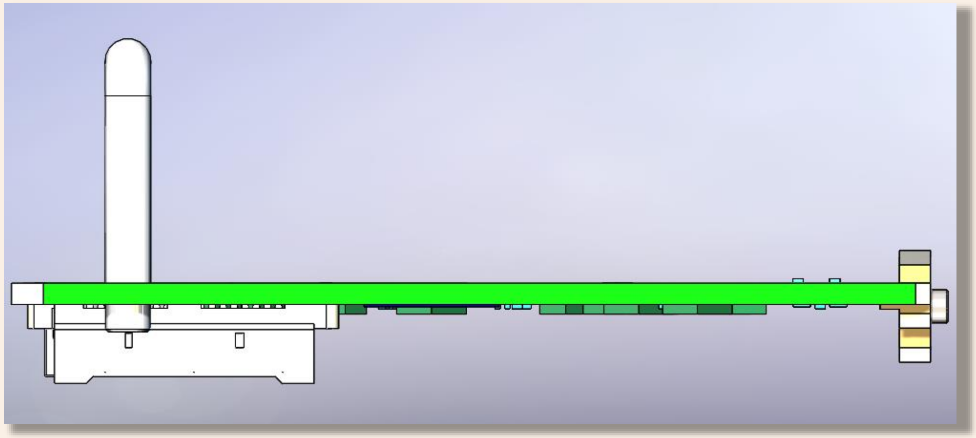
- The speed of optical transceiver devices being tested is ever-increasing
- The volume of ultra-speed optical transceiver devices being tested is also increasing — dramatically
- Test of this emerging class of devices has been performed by hand with rack-and-stack systems or using loop back techniques — e.g. low volume or low confidence
- Can we instead perform high speed device test with ATE and an automated handler?

A critical innovation

- The digital test instruments in ATE do not operate at these speeds
- Teradyne's fastest digital instrument operates at up to 10Gbps — far too slow to test 32Gbps-class devices
- But we can use SERDES technology to close the gap

4:1 / 1:4 SERDES Module

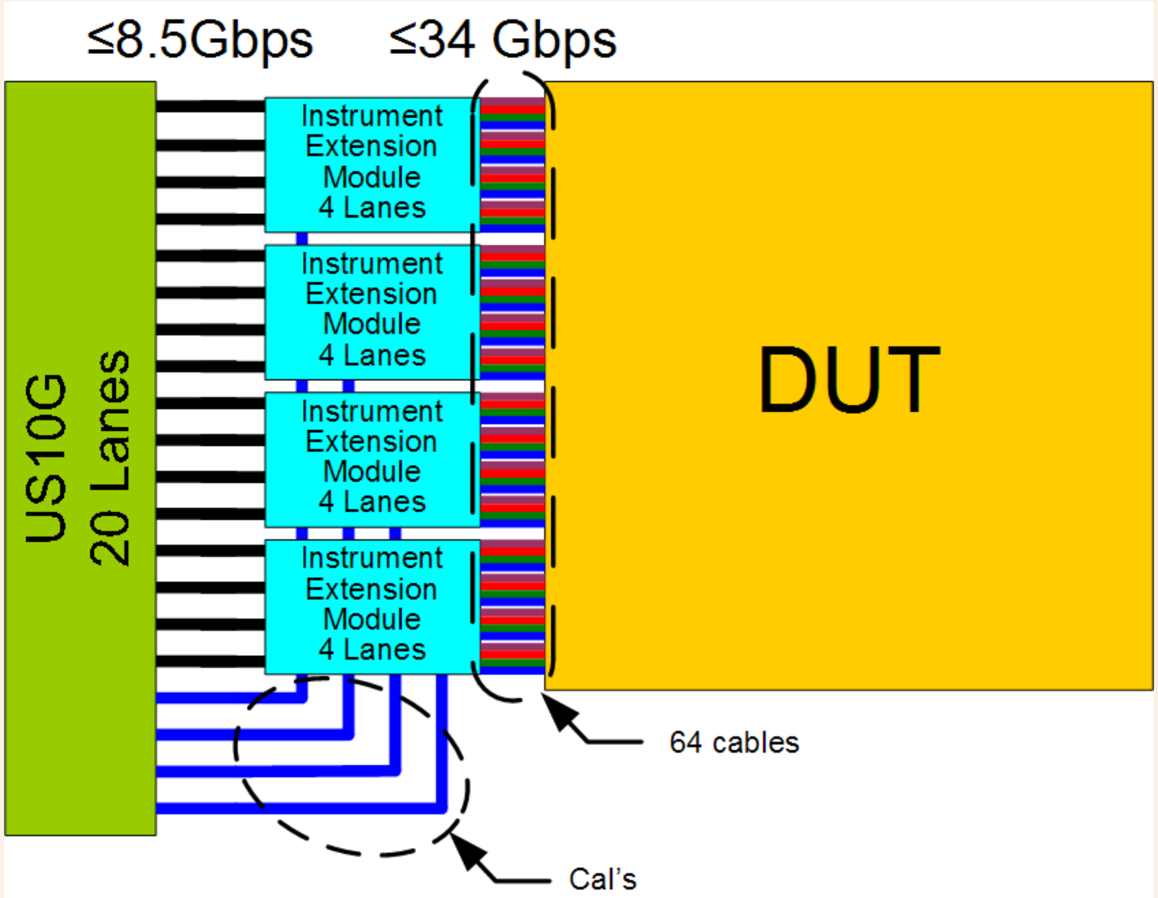
- SERializes four up-to-8.5Gbps streams into a single up-to-34Gbps stream
- DESerializes a single up-to-34Gbps stream into four up-to-8.5Gbps streams



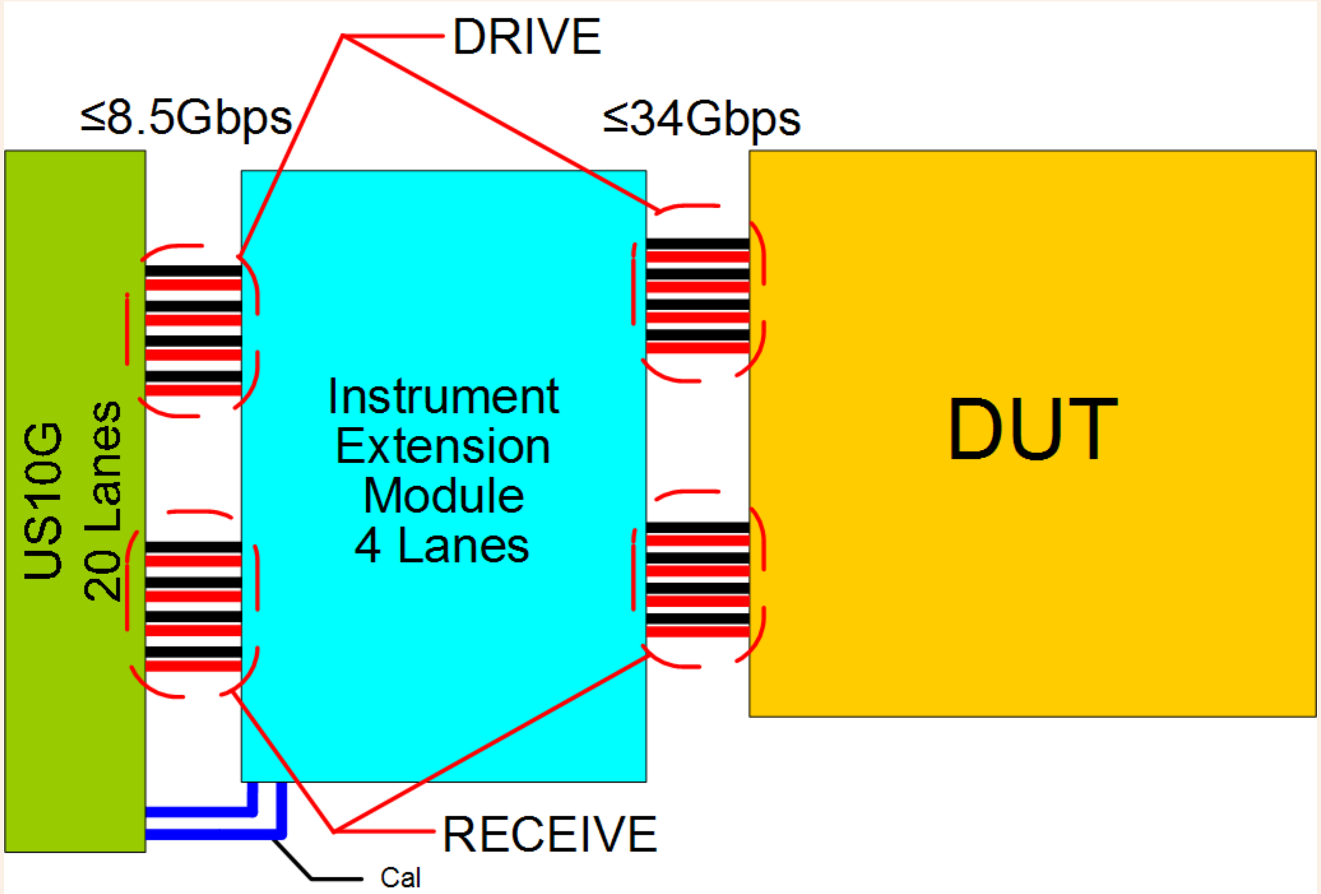
How is this new tool applied?

- With this “Instrument Extension”, one Teradyne high speed digital instrument can support up to 16 Lanes (16 Drive channels to the DUT and 16 Receive channels from the DUT)
- If the DUT has more than 16 Lanes to be tested the balance of the high speed Lanes must be tested using a multi-insertion protocol to achieve coverage of the untested Lanes

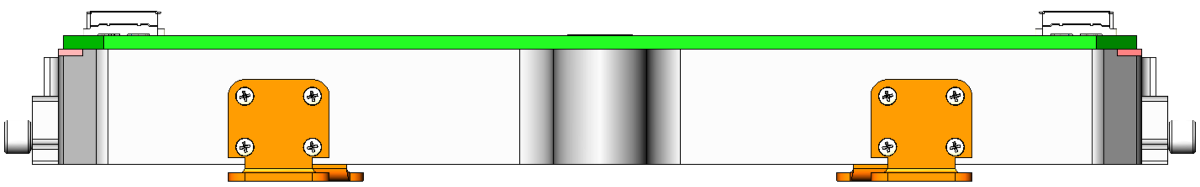
Instrument to / from DUT



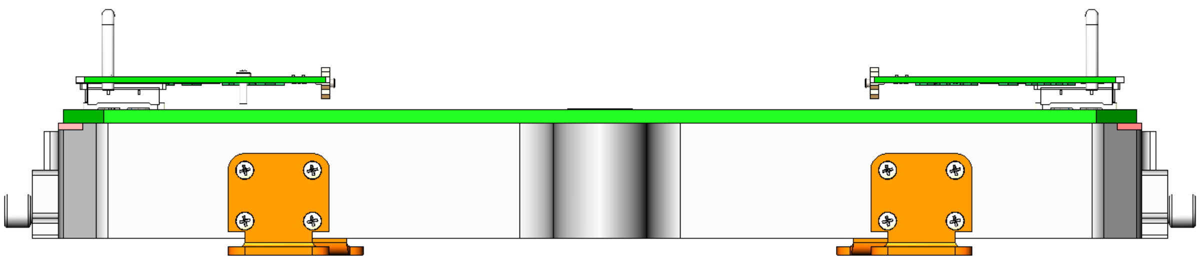
Looking closer . . . .



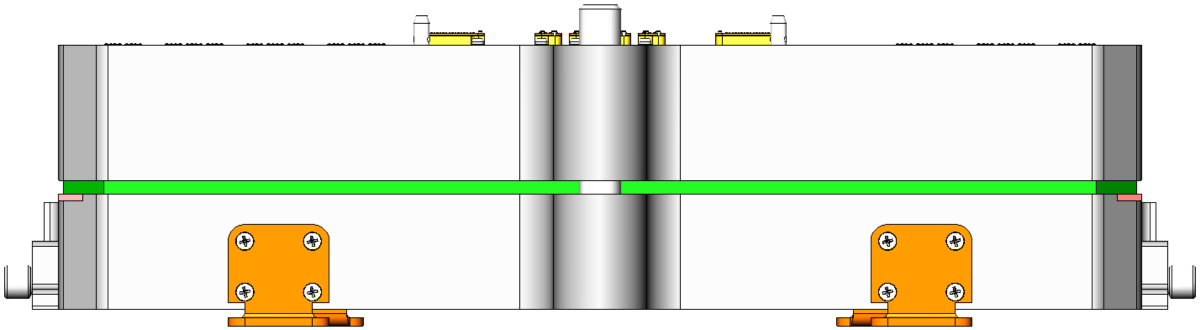
Family Board Assembly



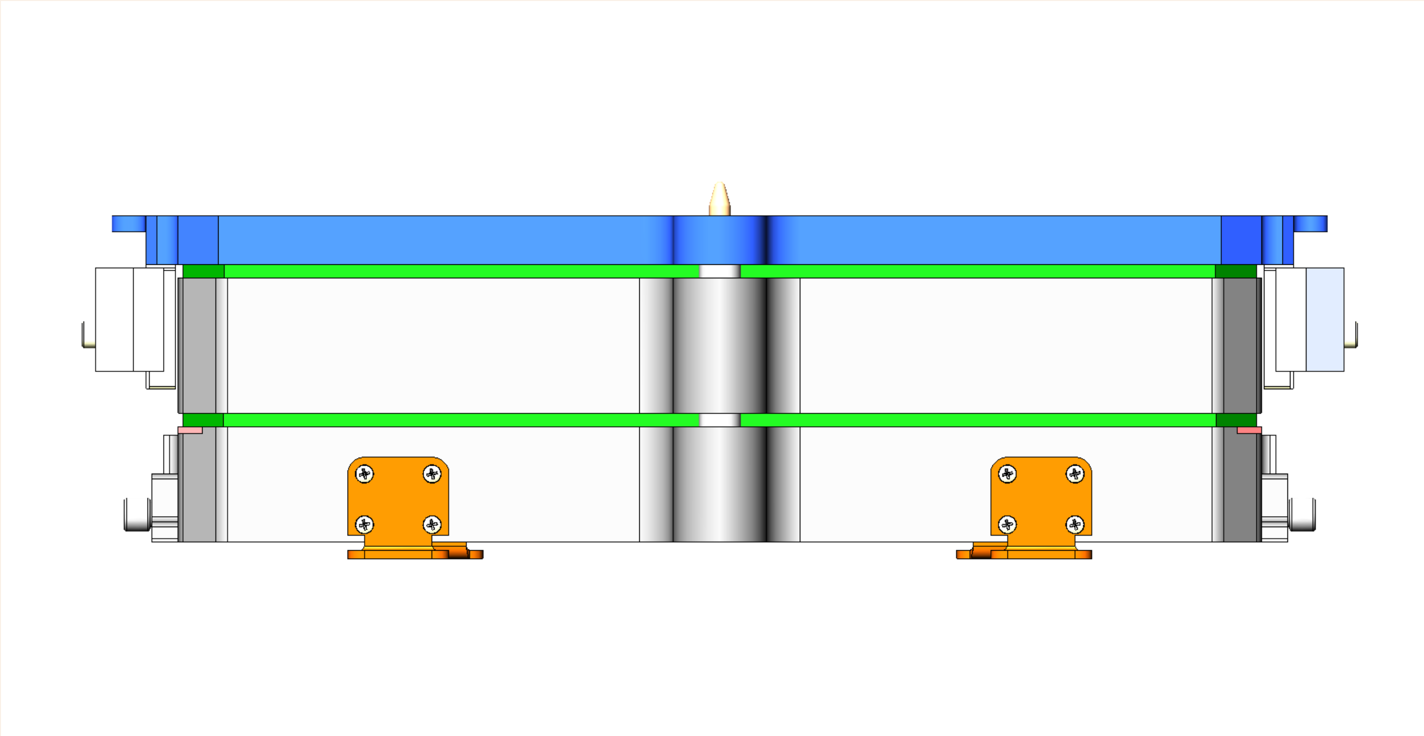
SERDES Modules added



Extender section added



DSA (HIB) Assembly mounted

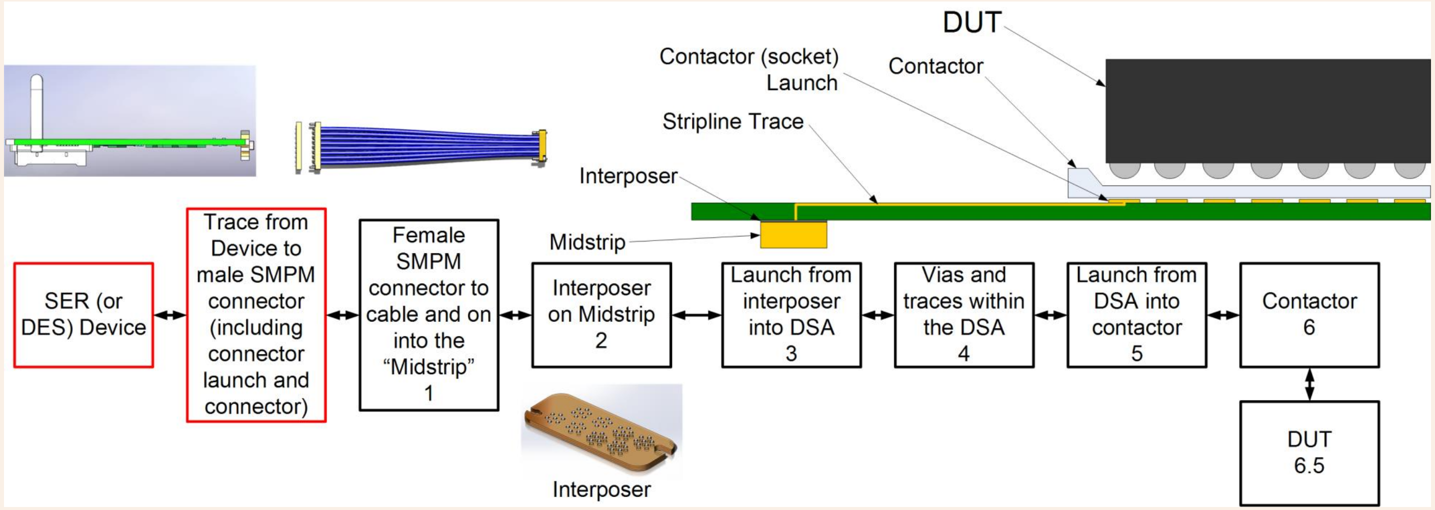


Where No Tester Has Gone Before

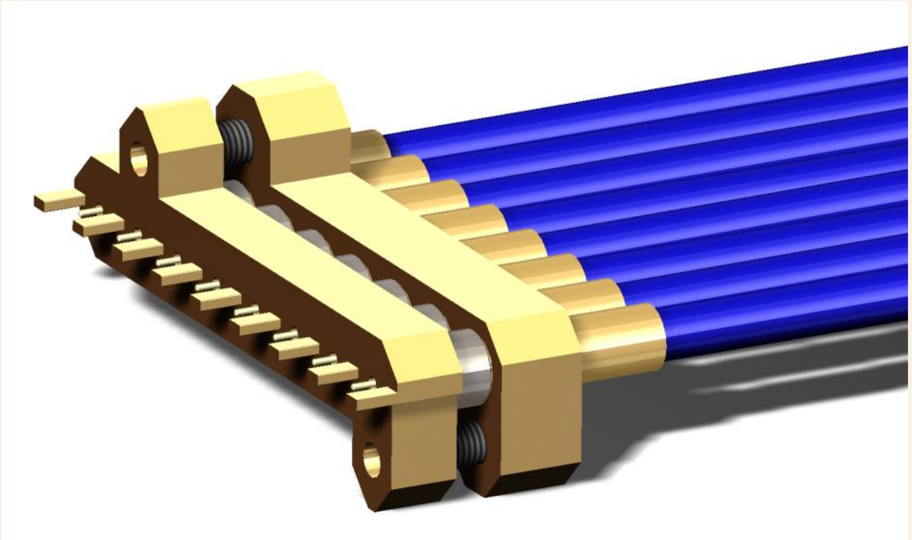
Looking for the weakest link

- With any high speed channel, the greatest mismatch / cause of signal loss / bandwidth limiter is going to be the component or system which most degrades the rise time and causes the eye to collapse
- Given the ultra-speed nature of this project, we looked at each and every component in the channel as a potential failure point

SI Investigation

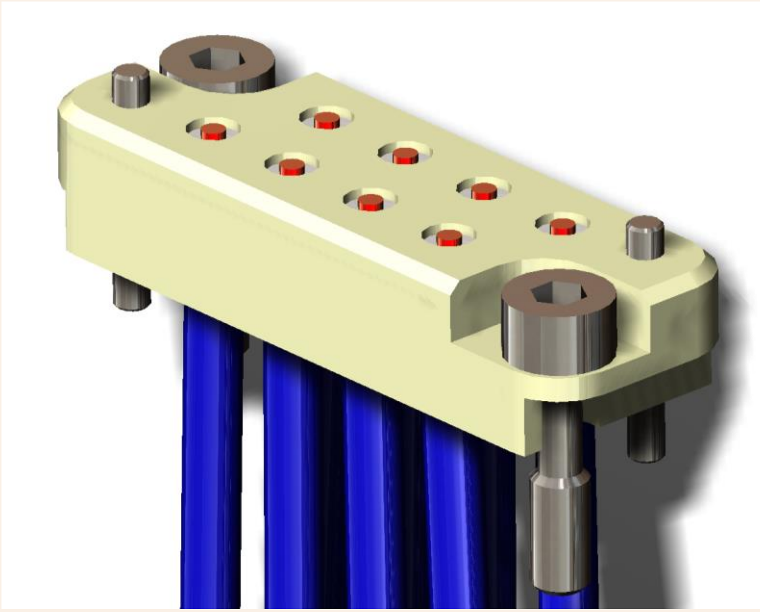


Board-edge connector to cable



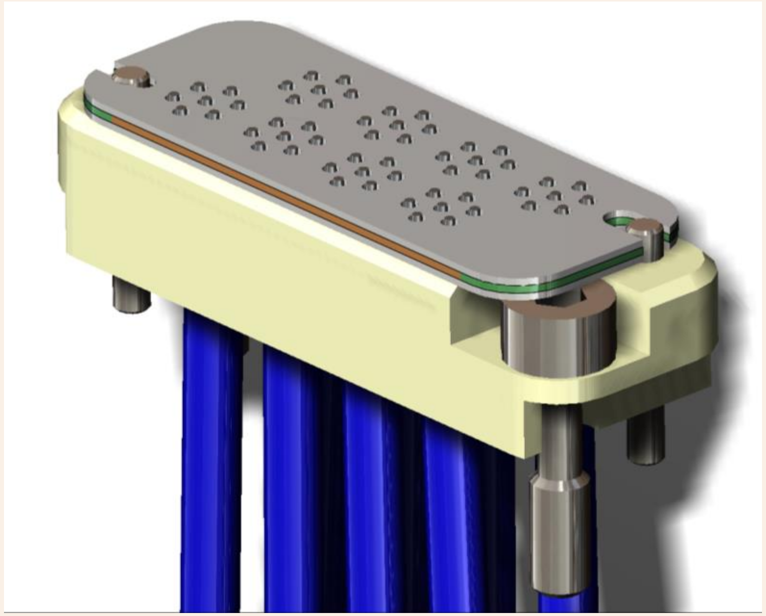
- This one's relatively easy from an SI point-of-view. It's a straightforward SMPM to SMPM interconnect

Cable to Interposer



- The cable terminates in a "Midstrip"
  - The interposer mounts here

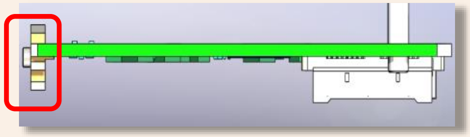
Interposer



- Evaluated several technologies for this critical component

Converting rise time to S21 (channel) bandwidth

- The 20%-80% rise time ($Tr_{(20-80)}$) of the signal between the DUT and the Module Board is 8ps (at the Module Board edge)
  - The rise time when it arrives at the DUT is allowed to degrade to as "slow" as $Tr_{(20-80)}$ 12ps



$$f3dB = 0.22 / Tr_{(20-80)}$$

- For $Tr_{(20-80)}$ = 8ps this equates to a signal channel with an insertion loss of 3dB @ 28GHz
- For $Tr_{(20-80)}$ = 12ps this equates to a channel with an insertion loss of 3dB @ 18GHz

Conservative conversion

- The 0.22 factor is the “nominal” number, the conservative value is 0.27*

$$f3dB = 0.27 / Tr_{(20-80)}$$

- For $Tr_{(20\text{-}80)}$ = 8ps this equates to a target insertion loss of 3dB @ 34GHz
- For $Tr_{(20\text{-}80)}$ = 12 ps using the conservative value we get 3dB @ 23GHz

*The difference between the nominal and conservative numbers is driven by the anticipated form of the signal — the more square-wave like the waveform (the more the waveform is dependent upon higher harmonics) the higher this value needs to be to ensure fidelity.

Converting data rate to channel bandwidth

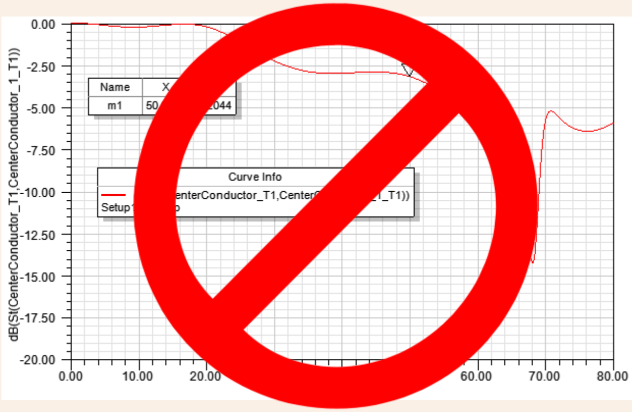
- The "Standard" Rule of Thumb says: "The required bandwidth (3dB of Insertion Loss) of a data channel is 1.5X the data rate", e.g. based upon the third harmonic of the data stream or 3X the Nyquist frequency
- For this program the maximum data rate was 32.8Gb/s, so the required channel bandwidth (I-L 3dB point) must be 49GHz according to this Rule of Thumb
- The "Test" RoT answer (a channel so clean that the waveform of the DUT can easily be seen without channel-induced distortion, e.g. suitable for Test) changes the data rate multiplier factor to 2.5, so the RoT -3dB point becomes . . . 82GHz (!!?!)

Discussion

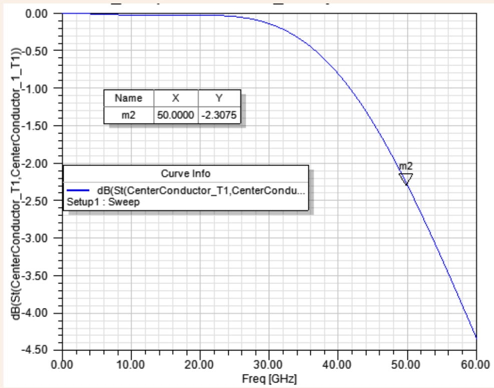
- The data rate Rule of Thumb approach *should only be used when the signal rise time is not known!*
- It is very conservative (see the previous slides) and, *if achievable*, does ensure a sure-fire result!
- As a conservative solution at lower speeds it is a fine (if overkill) approach — at speeds such as those required by this program we cannot achieve the bandwidths required by the Rule of Thumb
- Fortunately we knew the rise time and could ignore the RoT method

Further Discussion

- For any of these mathematically predictive approaches to work the degradation of the S21 curve *must* look like single-pole roll-off:



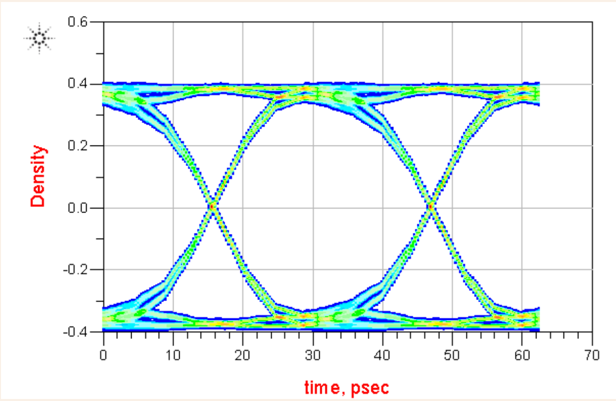
Before Design Optimization



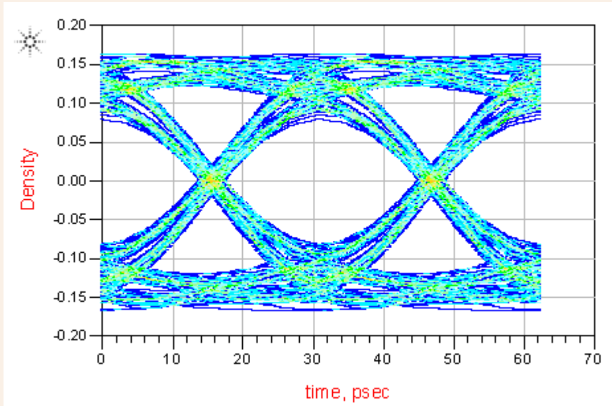
After

Just one more thing . . . .

- Here's an eye diagram @ 32Gbps through a channel with an insertion loss of 3dB @ 28GHz:



Basic



With DDj injection

Conclusion

- We have achieved the previously impossible — testing a meaningful number of channels of 32Gbps class devices using conventional test hardware
- We were able to accomplish this by paying intense attention to all aspects of the design.
- No detail was too small to consider — dimensional tuning, material choices, vendor partner selection are all critical for success