
SIXTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 15 - 18, 2015
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 6
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Session 6
Marc Mössinger
Session Chair

BiTS Workshop 2015 Schedule

Performance Day

Tuesday March 17 1:30 pm

Lord of the Dance

"Electrical circuit model for silicon wafer spring pin probe"
Mohamed Eldessouki - SV Probe

"Kelvin Sockets at Speed"
Gert Hohenwarter - GateWave Northern, Inc.

"Designing Sockets for Ludicrous Speed (80 GHz)"
Don Thompson - R&D Altanova
Jose Moreira - Advantest

"PCB Test Fixture and DUT Socket Challenges for 32 Gbps/GBaud ATE Applications"
Jose Moreira - Advantest
Christian Borelli & Fulvio Corneo - STMicroelectronics

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Electrical circuit model for silicon wafer spring pin probe

Mohamed Eldessouki

SV TCL – An SV Probe Company

2015 BiTS Workshop
March 15 - 18, 2015

Contents

- Motivation and Objective
- Introduction
- Spring Pin Measurements and Simulation
- Spring Pin Modeling and Verification
- Summary and Conclusion

Motivation & Objective

Motivation

WL-CSP and WLP Customers are looking for spring pin circuit model to be able to:

- Simulate and Predict Bandwidth (BW)
- Simulate and Predict Power Plane Input Impedance
- Reduce risk probe hardware not to meet test expectations

Objective

Develop Close Form Accurate Circuit Model

Verify Developed Model Using:

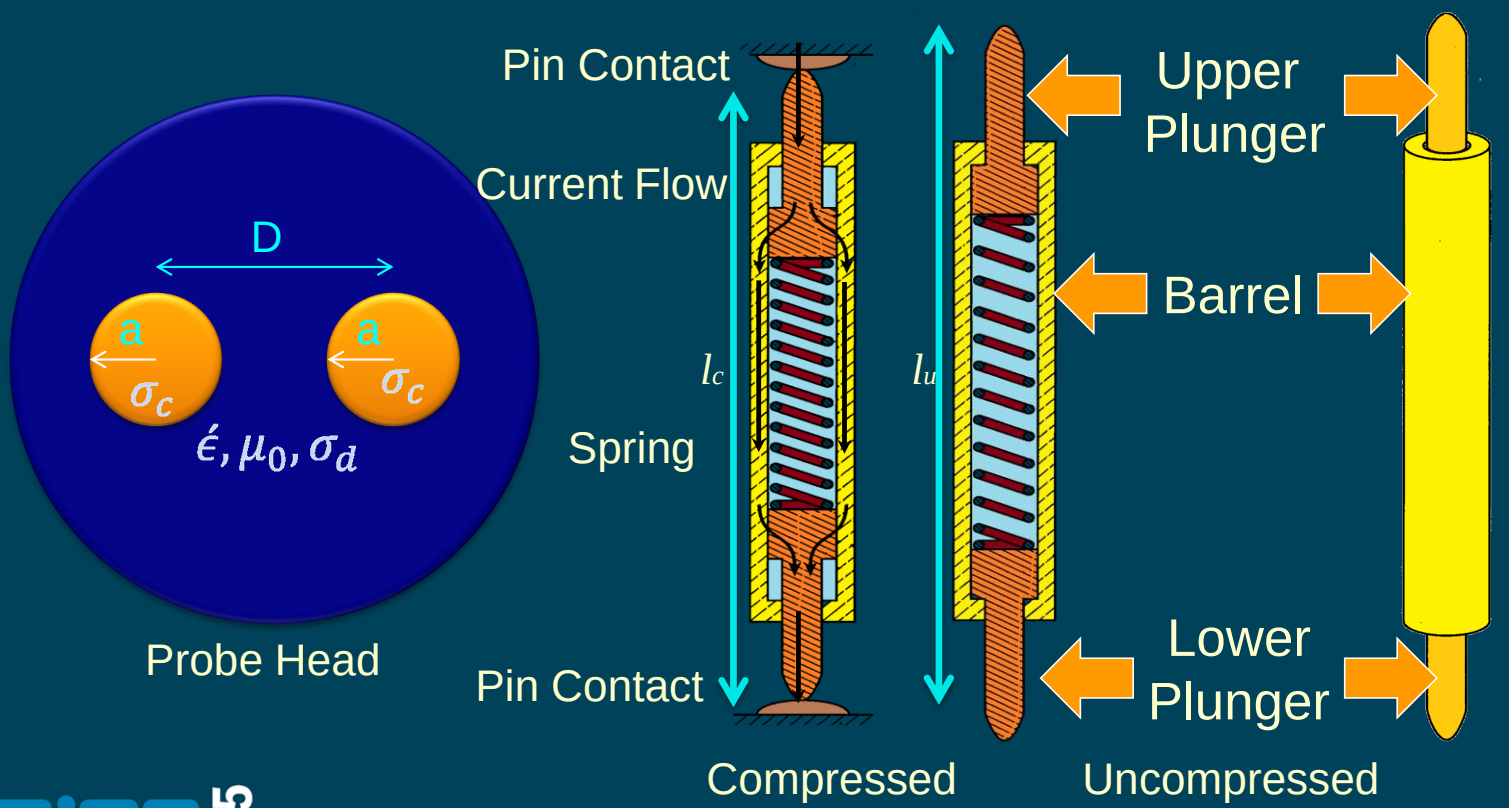
- Measured S-parameters
- Ansoft HFSS Simulation Tool (Field Analysis)

Introduction

- Spring Pin Structure
- Parallel Wire Transmission Line (TL) Model Fundamental Equations
- Proximity and Skin Effect
- Parallel Wire Circuit Model Comparison
- Impedance Discontinuities

Introduction

Spring Pin Structure (Double Plunger)



Introduction

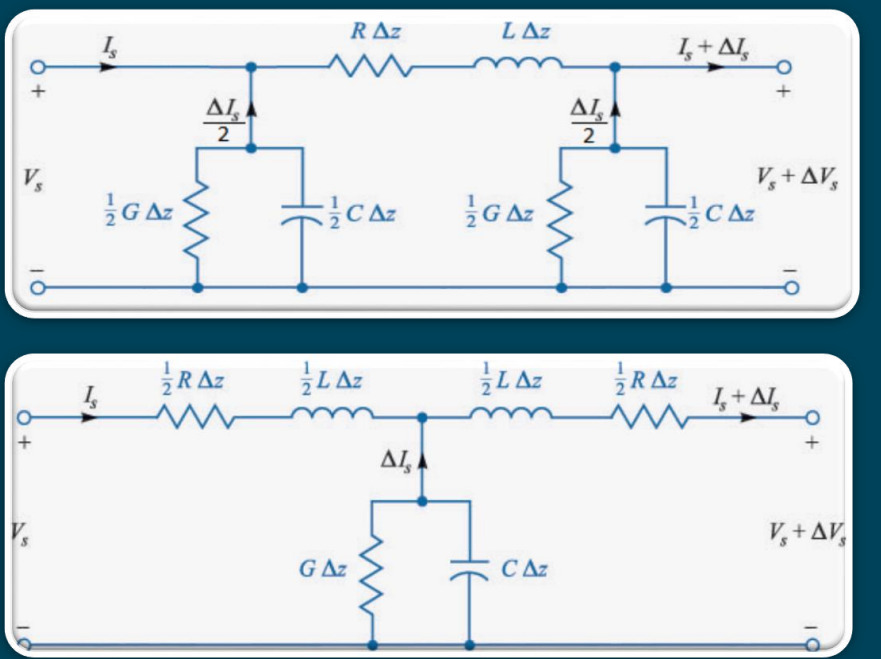
Fundamental Equations

$$L = \frac{\mu}{I_0 I_0^*} \int_s \overline{H}.\overline{H}^* \, dS$$

$$C = \frac{\varepsilon'}{V_0 V_0^*} \int_s \overline{E}.\overline{E}^* \, dS$$

$$R = \frac{R_s}{I_0 I_0^*} \oint_{S_1+S_2} \overline{H}.\overline{H}^* \, dl$$

$$G = \frac{\omega\varepsilon''}{V_0 V_0^*} \int_s \overline{E}.\overline{E}^* \, dS$$



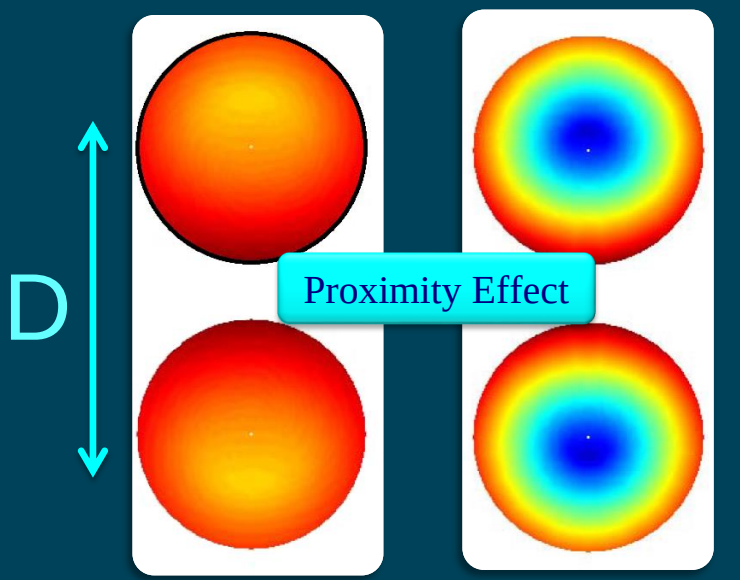
π and T Equivalent Circuit TL Model

Introduction

Proximity and Skin Effect

Current density distribution in parallel wire with small spacing D.

Unbalanced current distribution due to proximity effect.



Introduction

Parallel Wire TL Model Comparison Summary

Model	Advantages (Account for)	Disadvantages
Low Frequency	• Internal and External Inductance • Proximity effect	• No Skin Effect
High Frequency	• Skin Effect	• No Proximity Effect • No Internal Inductance
Wide Band	• Skin Effect • Internal Inductance • Proximity Effect in Inductance Calculation	• No Proximity Effect on Resistance Calculation Only

Introduction

Models Comparison

$$L = \frac{\mu_0}{\pi}\left[\frac{1}{4} + \cosh^{-1}\left(\frac{D}{2a}\right)\right]$$

$$R = \frac{2}{\pi a^2 \sigma_c}$$

Low Frequency

$$L_{ext} = \frac{\mu_0}{\pi}\cosh^{-1}\left(\frac{D}{2a}\right)$$

$$R = \frac{R_s}{\pi a}\frac{D/2a}{\sqrt{(D/2a)^2 - 1}}$$

High Frequency

$$L = \mathrm{Im}(Z)$$

$$R = \mathrm{Re}(Z)$$

Wide Band

Where

$$Z = 2Z_{\mathrm{int}} + j\omega L_{ext}$$

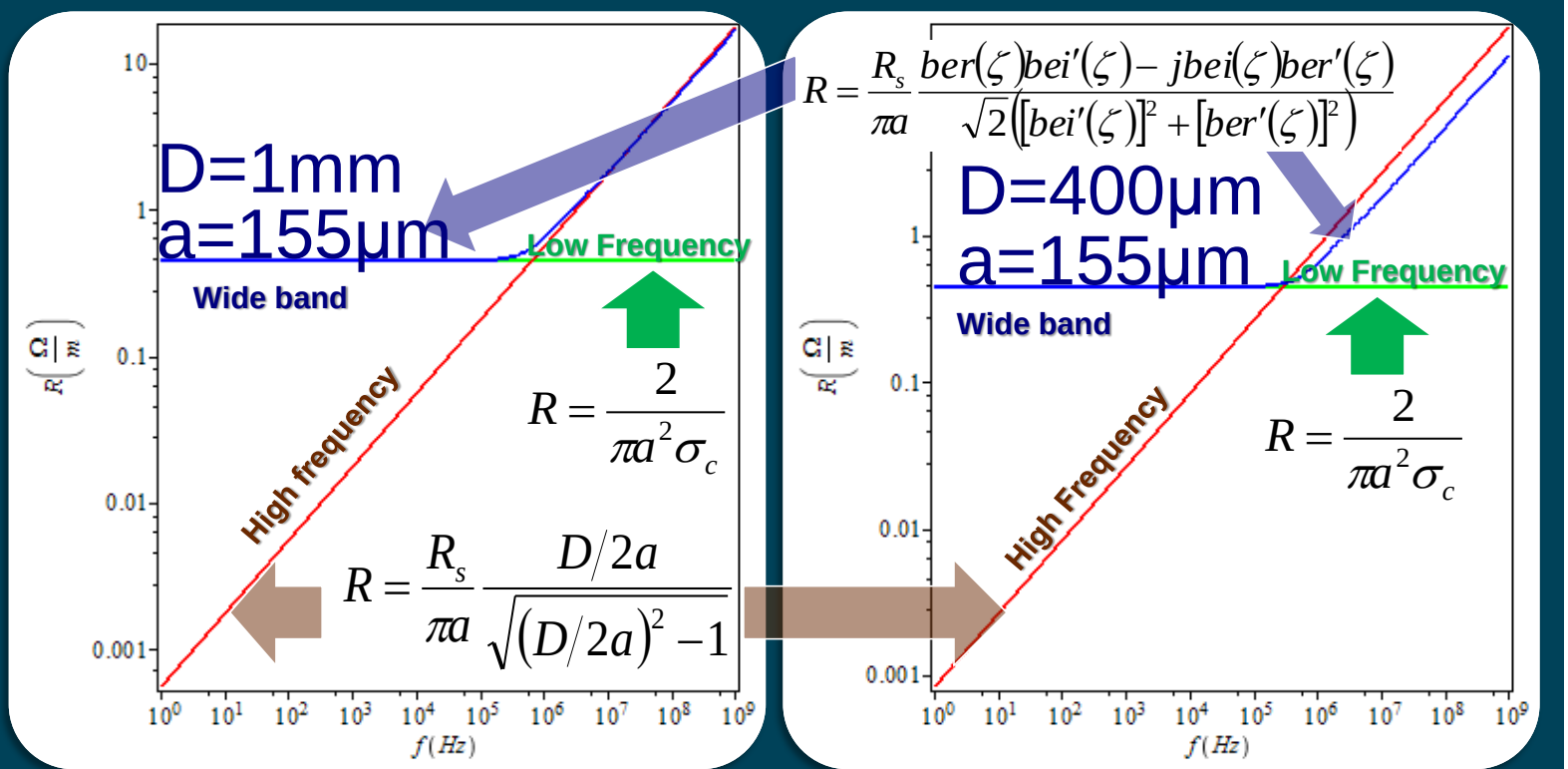
$$Z_{\mathrm{int}} = \frac{R_s}{\sqrt{2}\pi a}\frac{ber(\zeta) + jbei(\zeta)}{bei'(\zeta) - jber'(\zeta)}$$

$$L = \frac{R_s}{\pi a}\frac{ber(\zeta)ber'(\zeta) - jbei(\zeta)bei'(\zeta)}{\sqrt{2}\omega\left([bei'(\zeta)]^2 + [ber'(\zeta)]^2\right)} + \frac{\mu_0}{\pi}\cosh^{-1}\left(\frac{D}{2a}\right)$$

$$R = \frac{R_s}{\pi a}\frac{ber(\zeta)bei'(\zeta) - jbei(\zeta)ber'(\zeta)}{\sqrt{2}\left([bei'(\zeta)]^2 + [ber'(\zeta)]^2\right)}$$

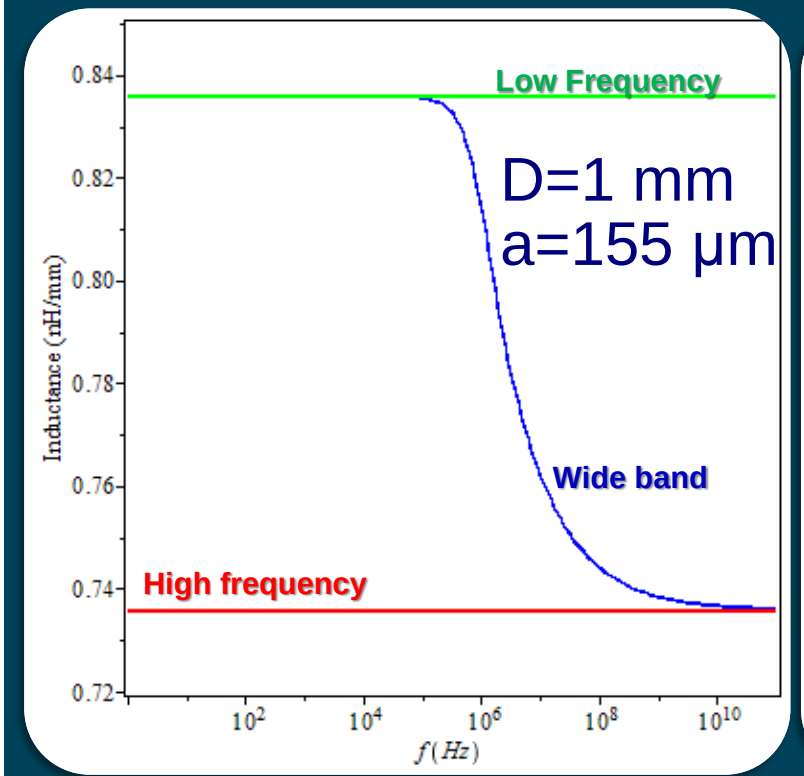
Introduction

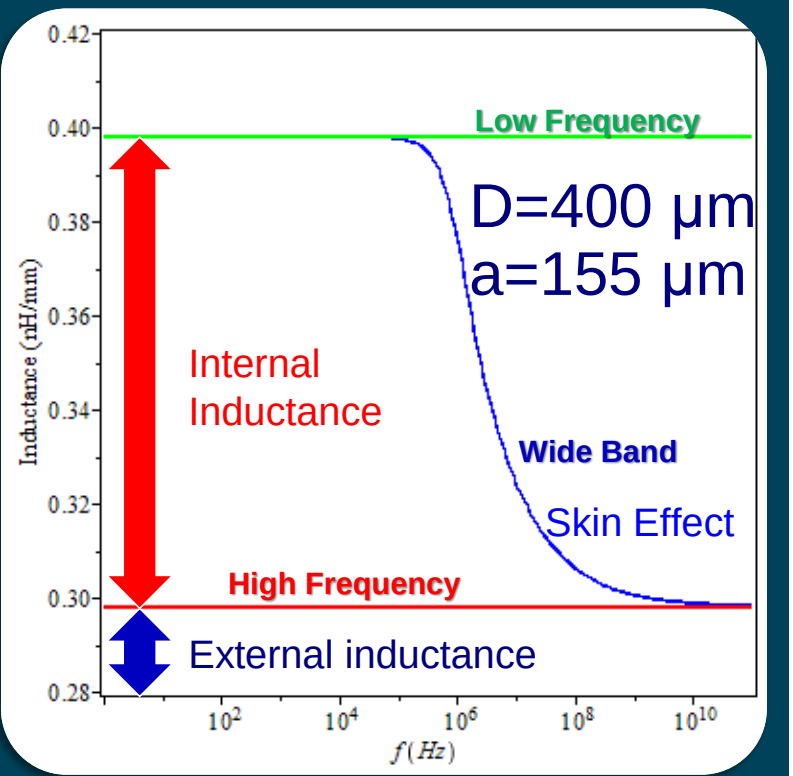
Models Comparison



Introduction

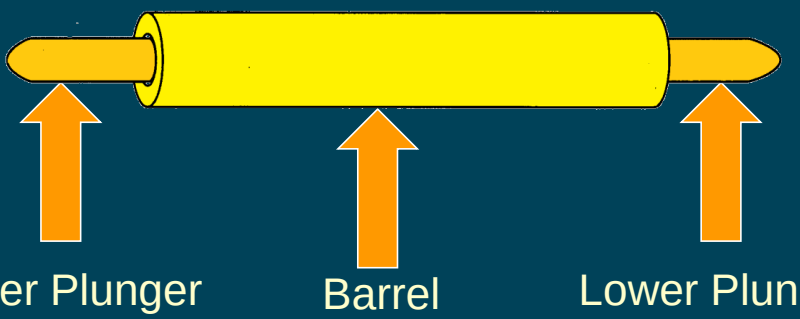
Models Comparison

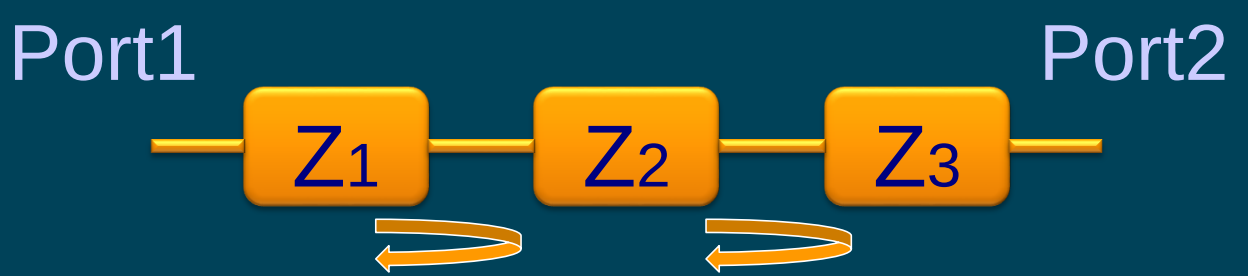




Introduction

Impedance Discontinuity

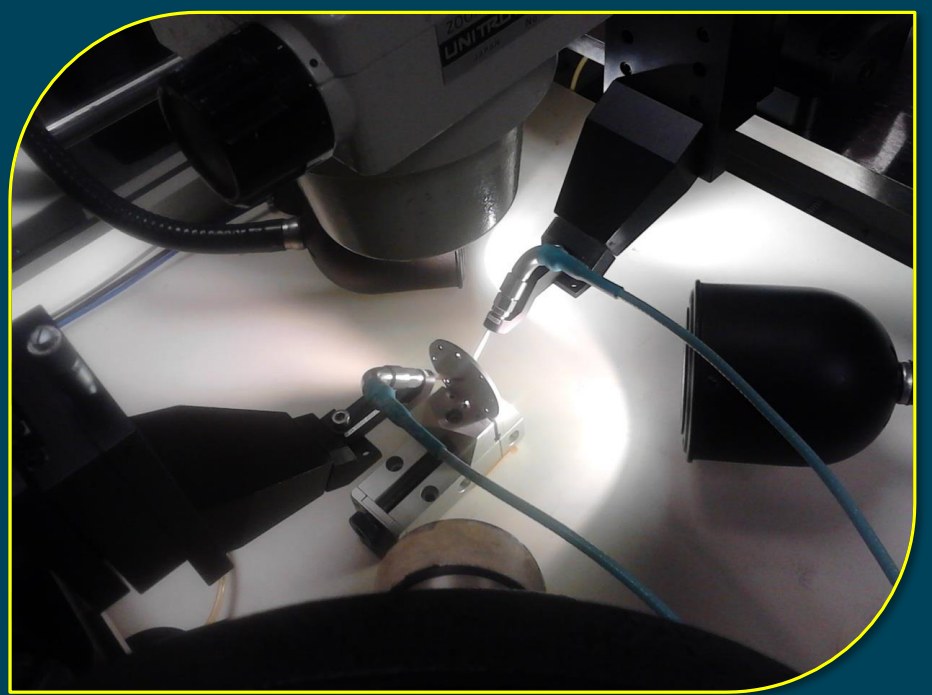




Wave reflections due to impedance mismatch.

Measurements & Simulation

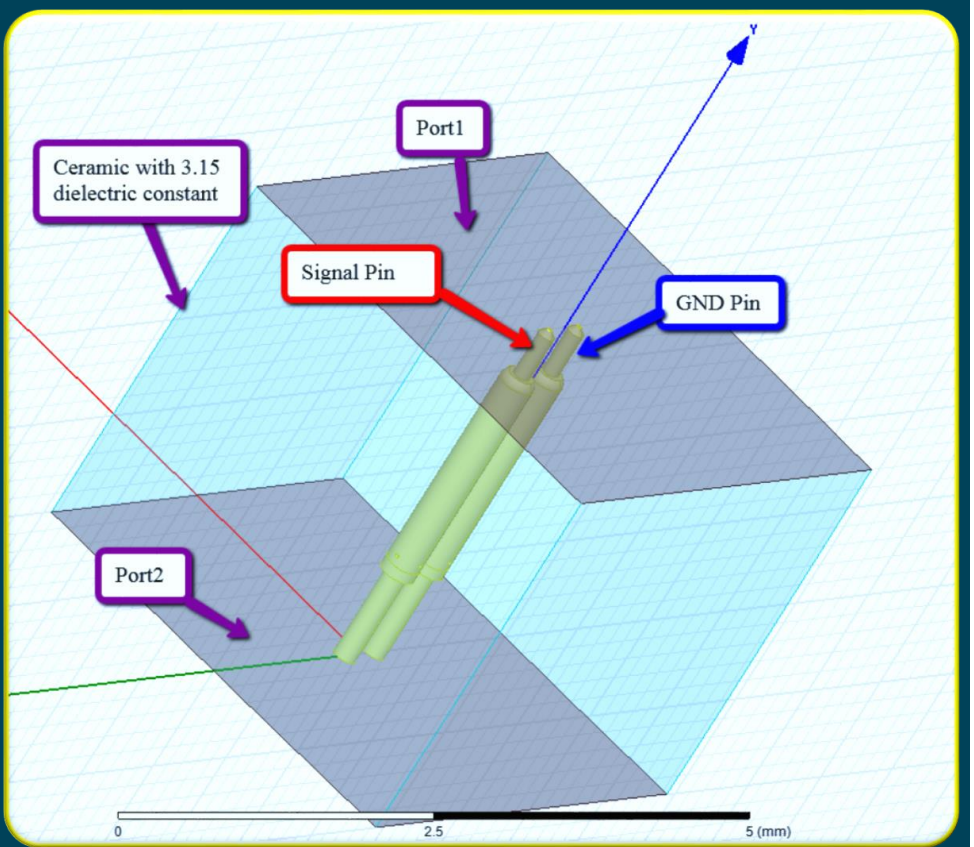
Measurement Setup



Measurements & Simulation

Ansoft HFSS Simulation

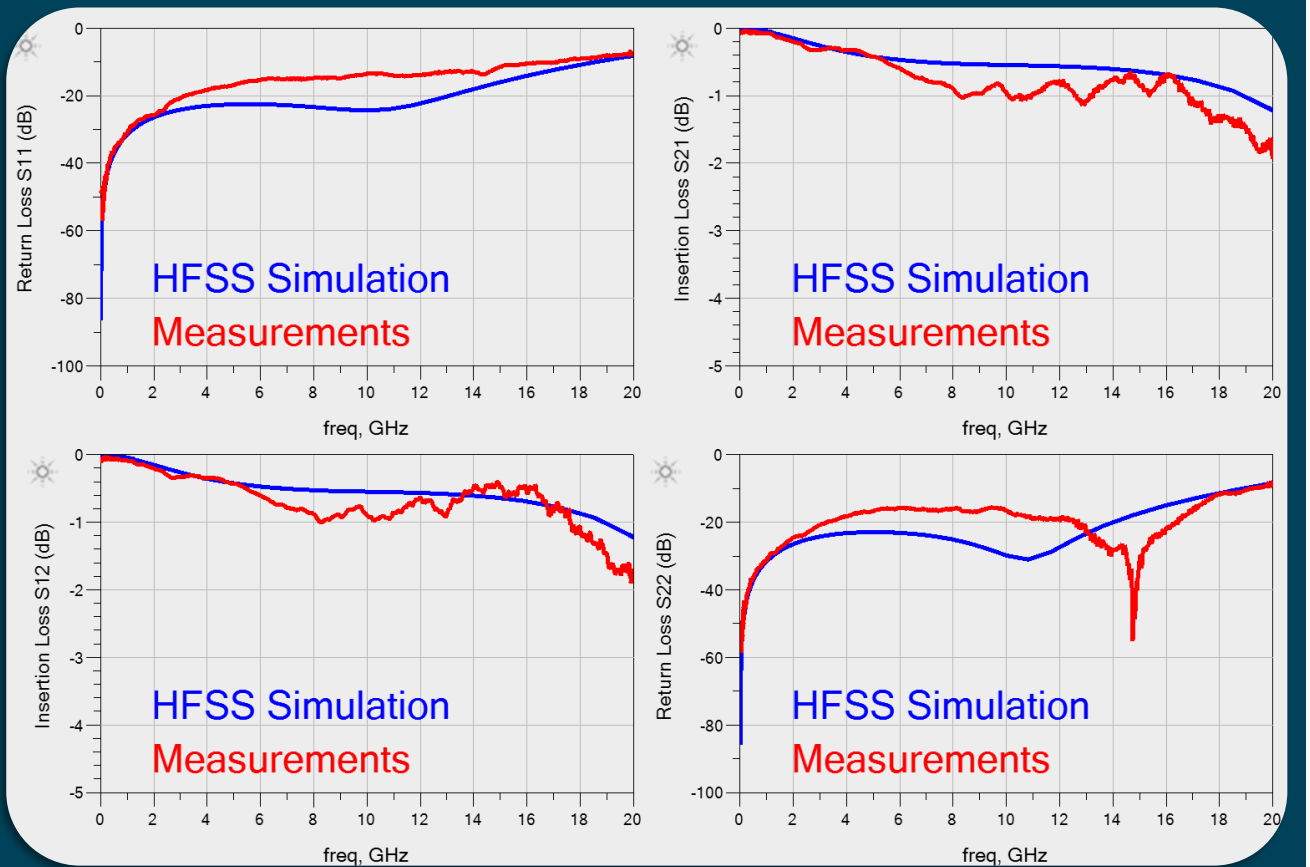
Structure and Boundary conditions.



Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Measurements & Simulation

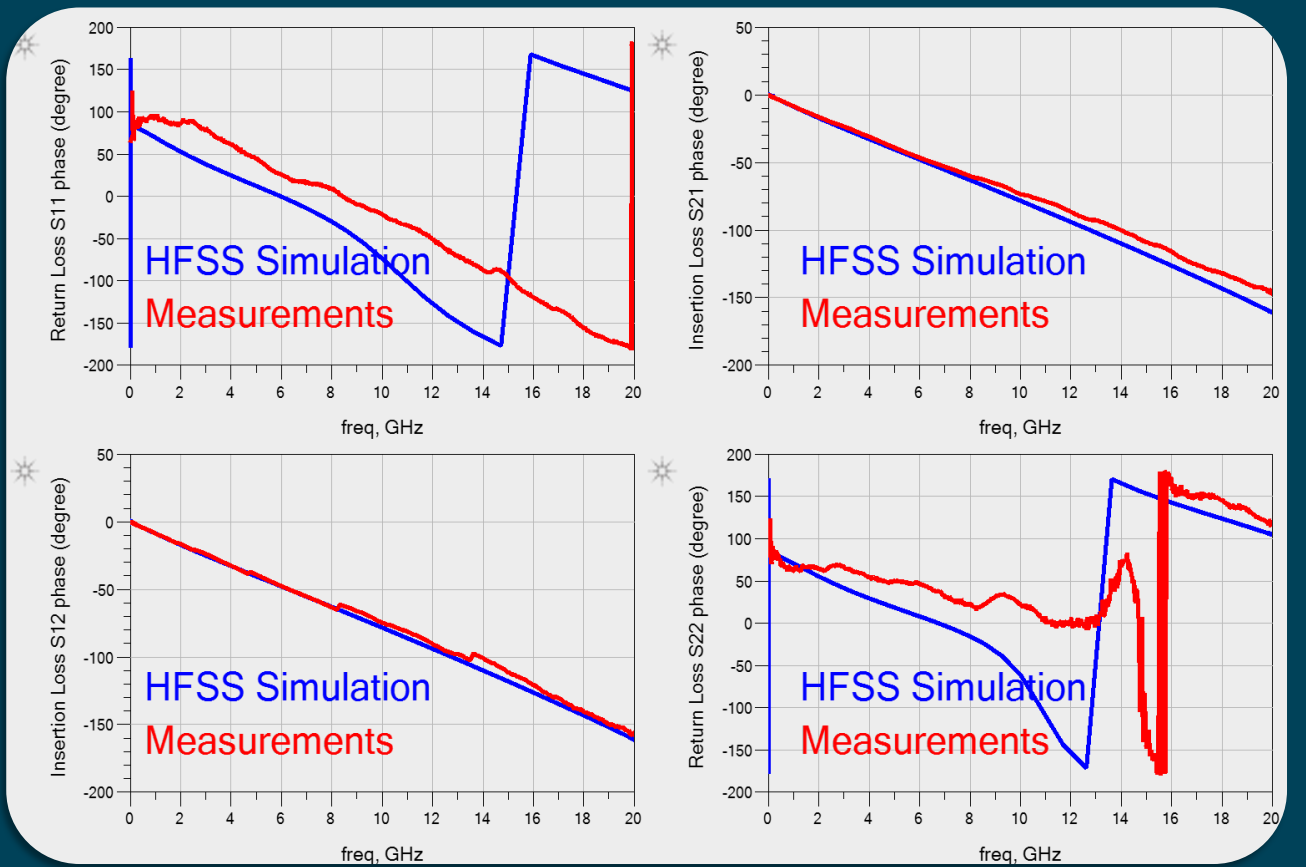
Insertion and Return Loss Magnitude



Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Measurements & Simulation

Insertion and Return Loss Phase

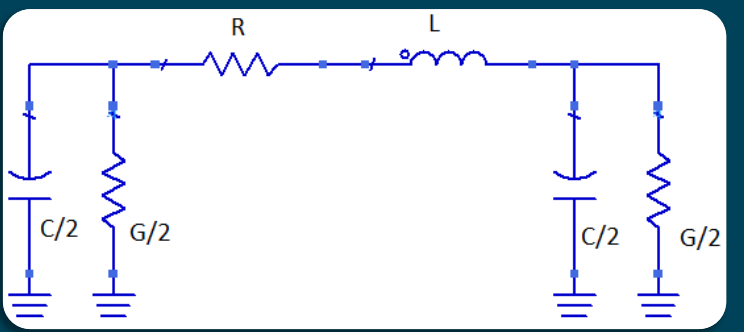


Electrical Circuit Model for Silicon Wafer Spring Pin Probe

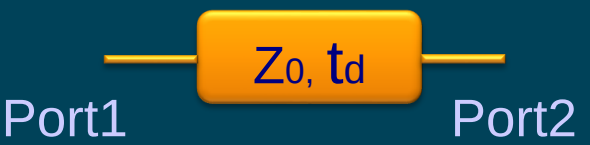
Circuit Model & Model Verification

Circuit Models

Lumped Circuit Model



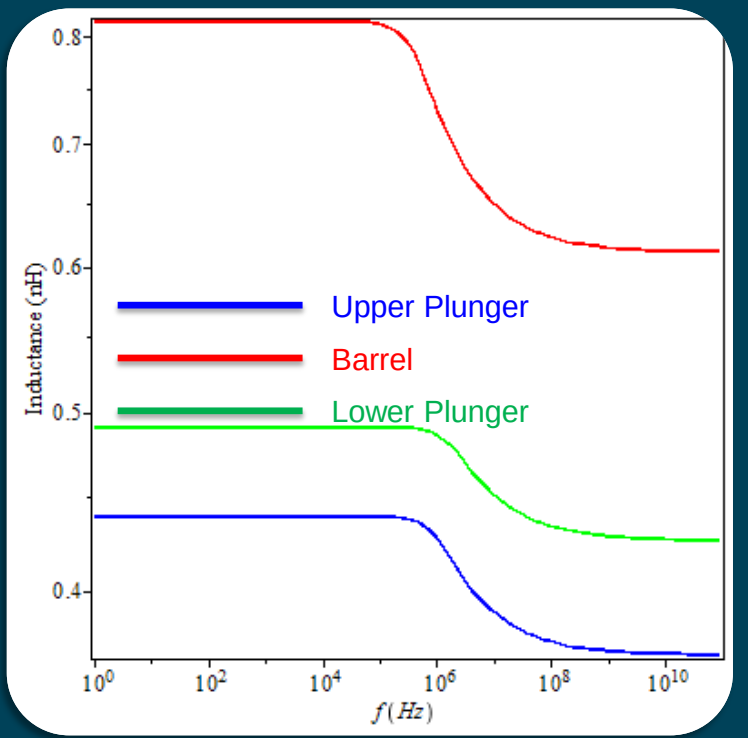
TL Model

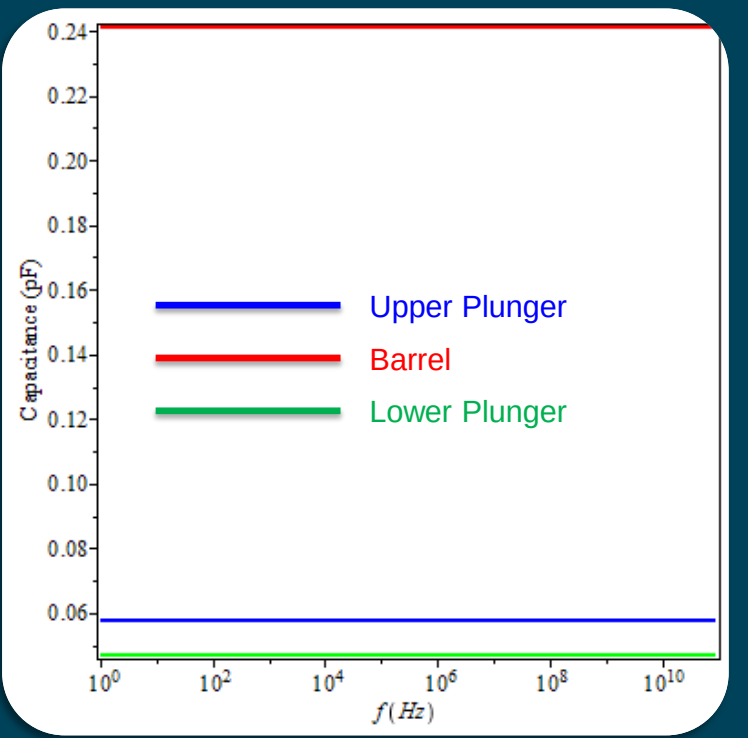


Spring Pin

Circuit Model & Model Verification

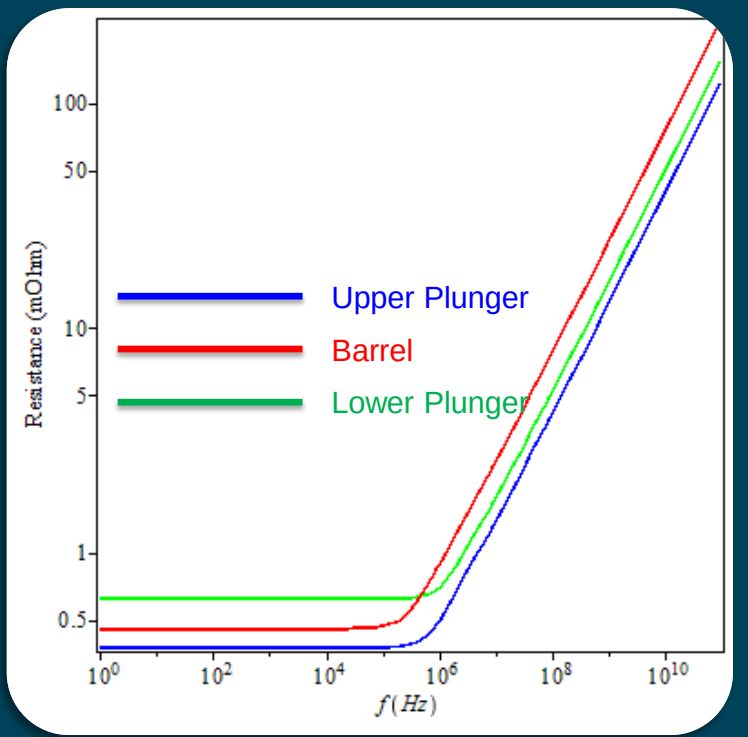
Circuit Model Parameters (Total L & C)

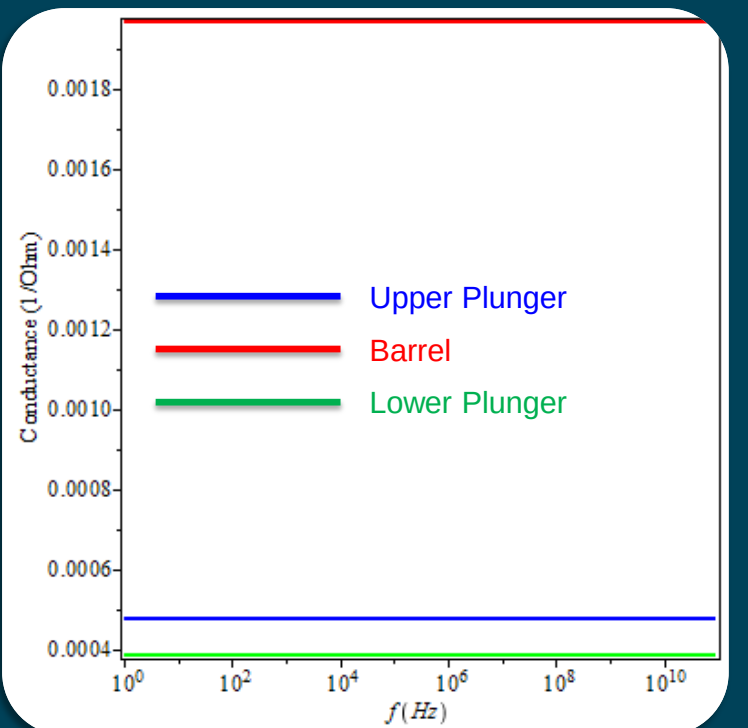




Circuit Model & Model Verification

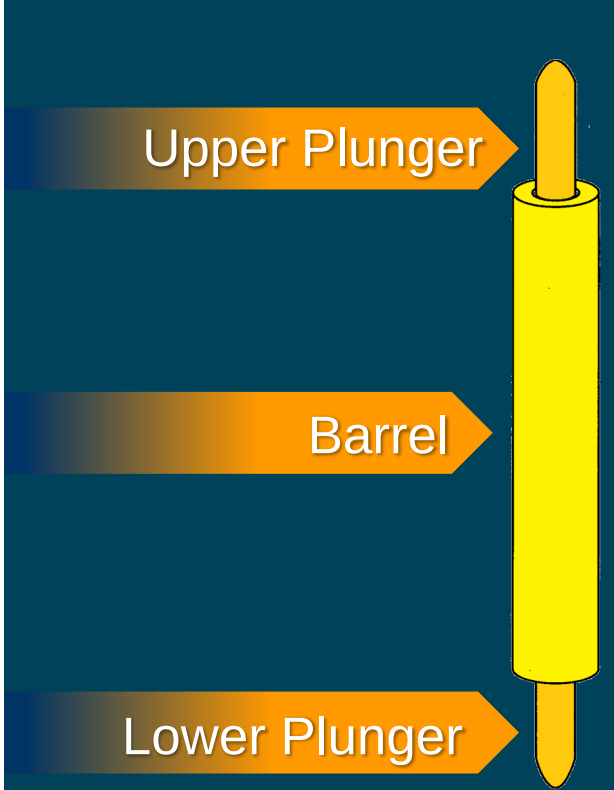
Circuit Model Parameters (total R & G)

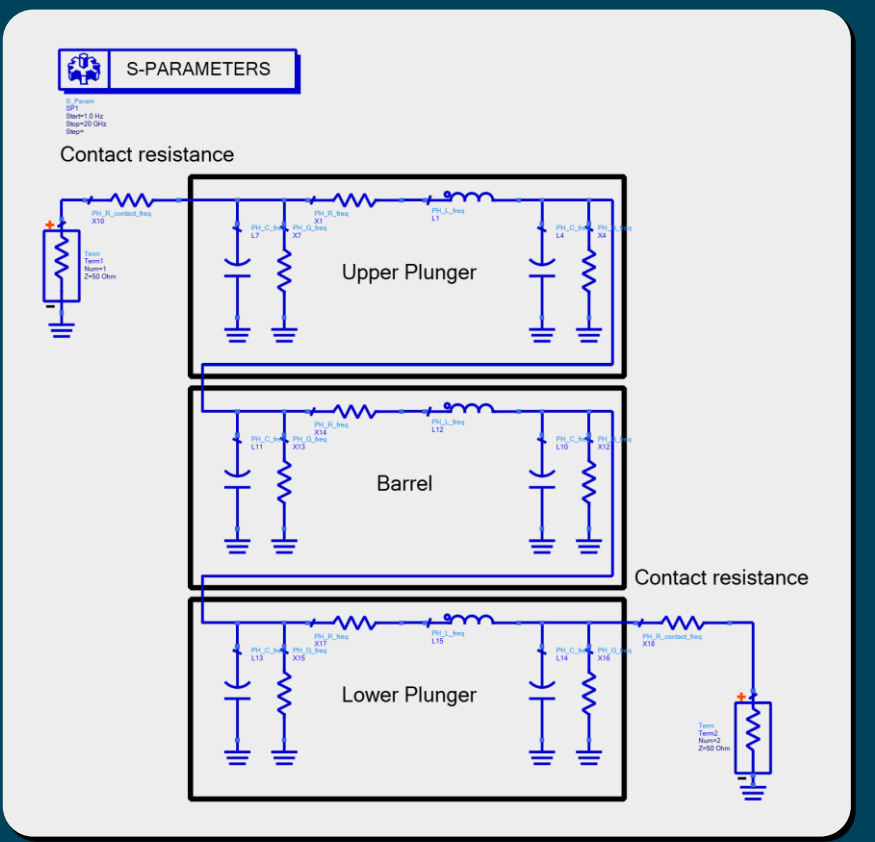




Circuit Model & Model Verification

Lumped Circuit π Model

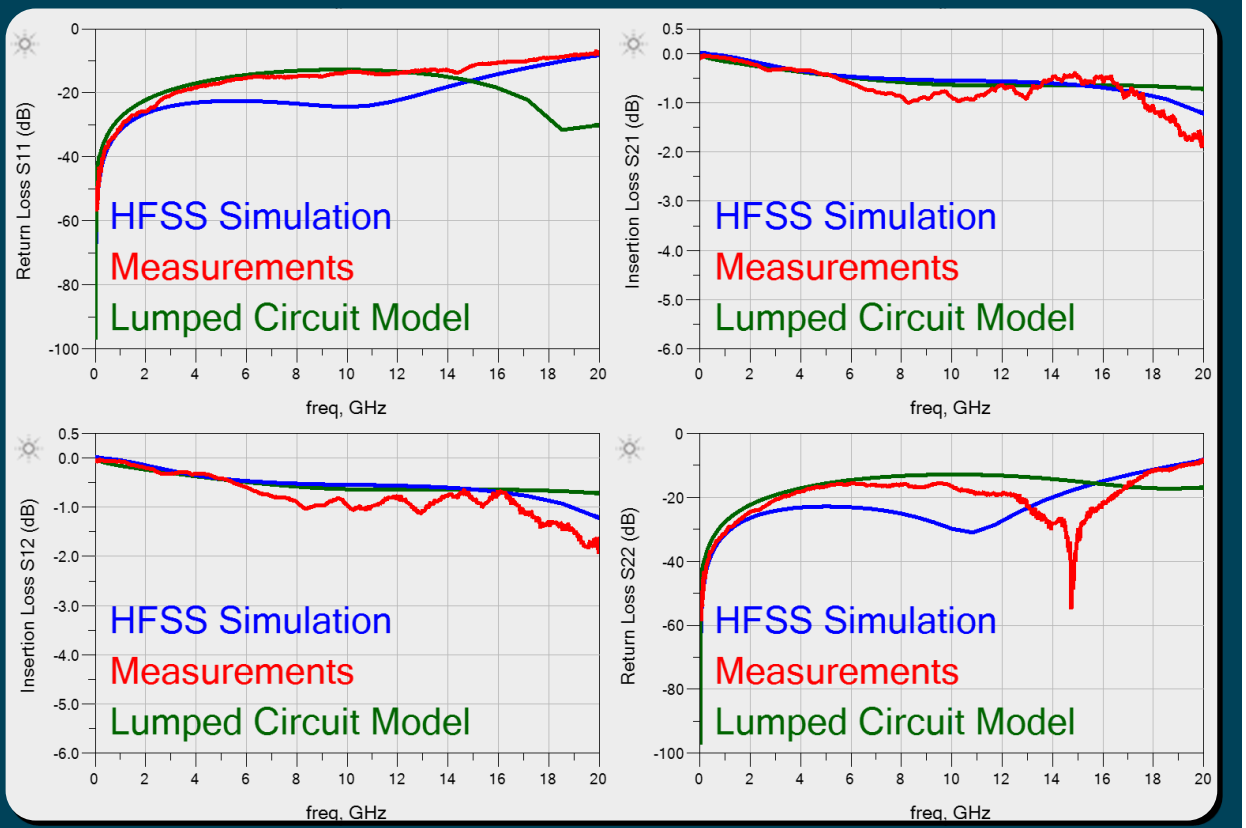




Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Circuit Model & Model Verification

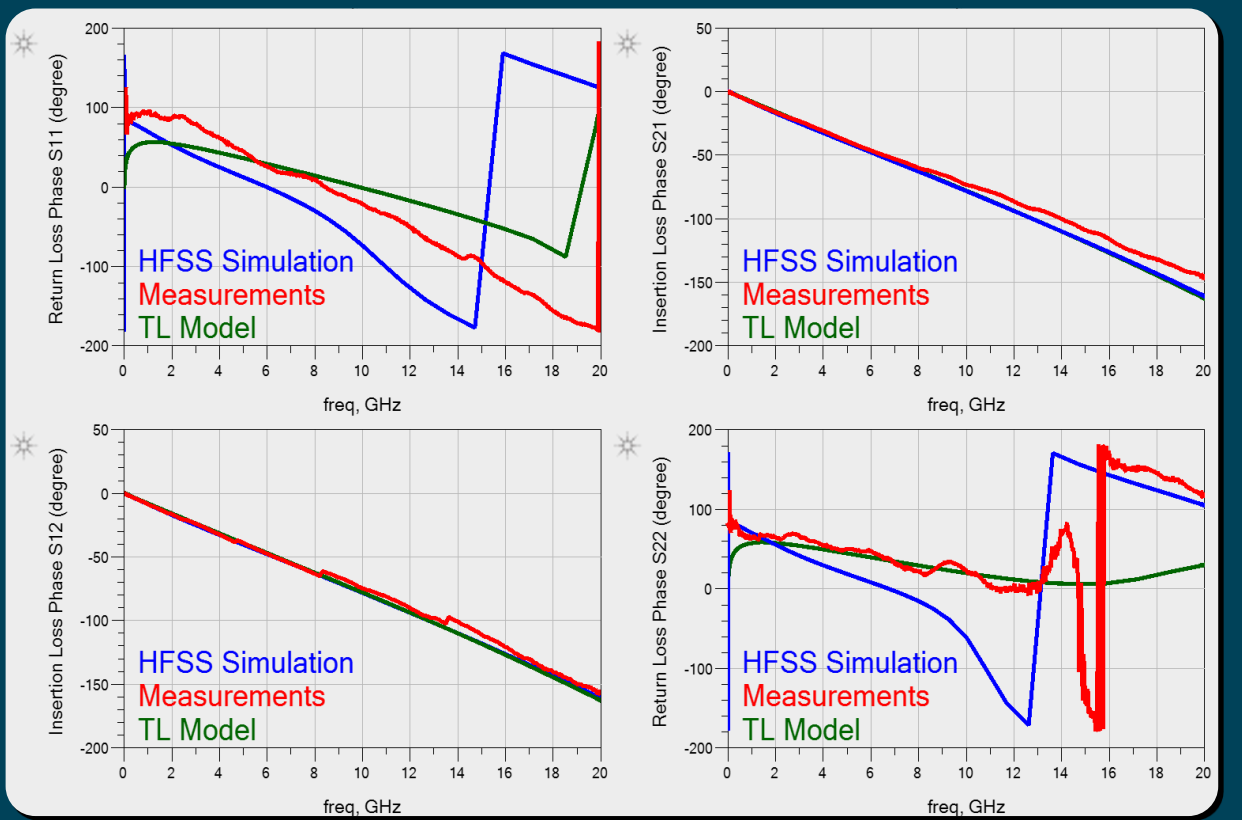
Lumped Circuit π Model



Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Circuit Model & Model Verification

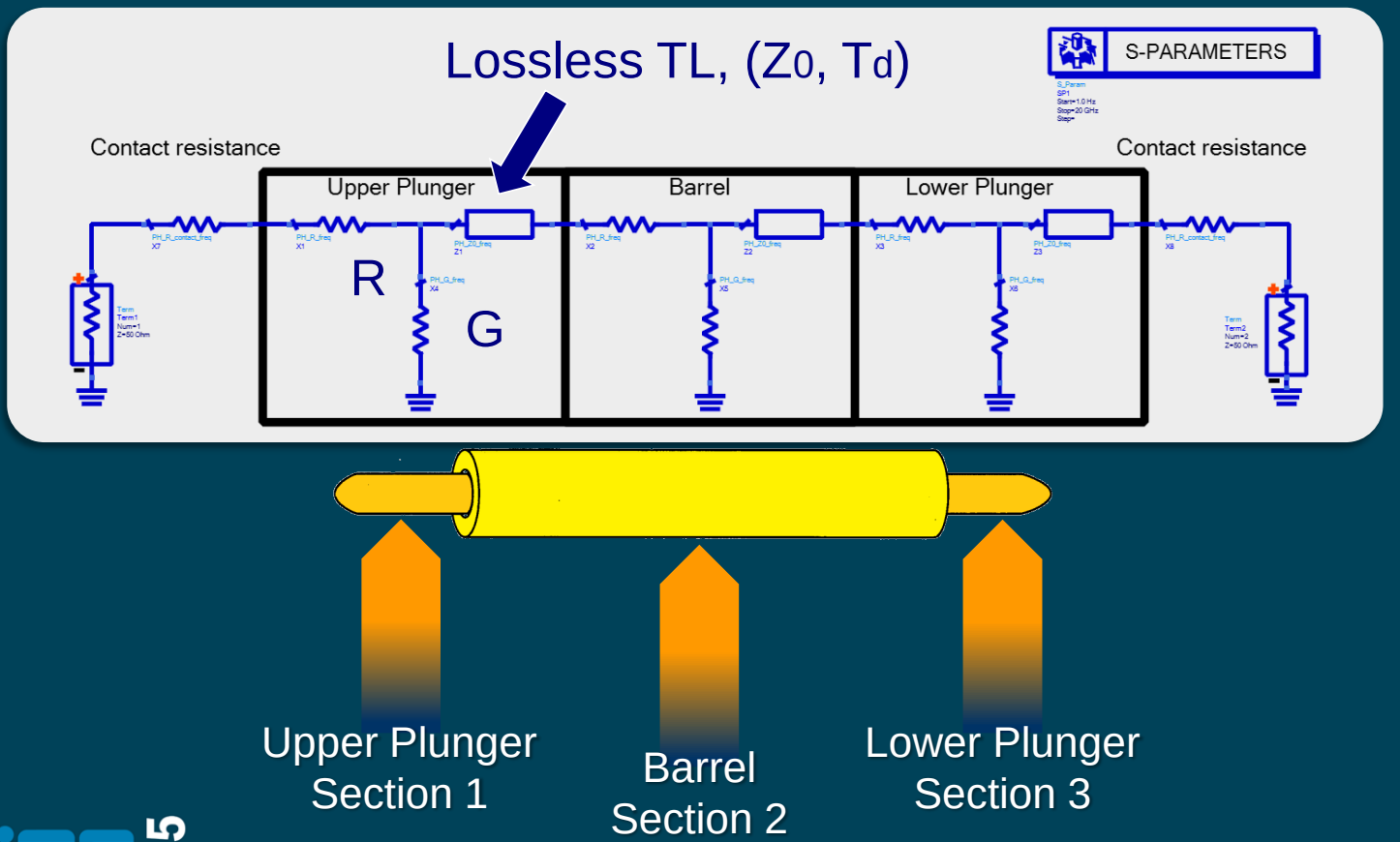
Lumped Circuit π Model



Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Circuit Model & Model Verification

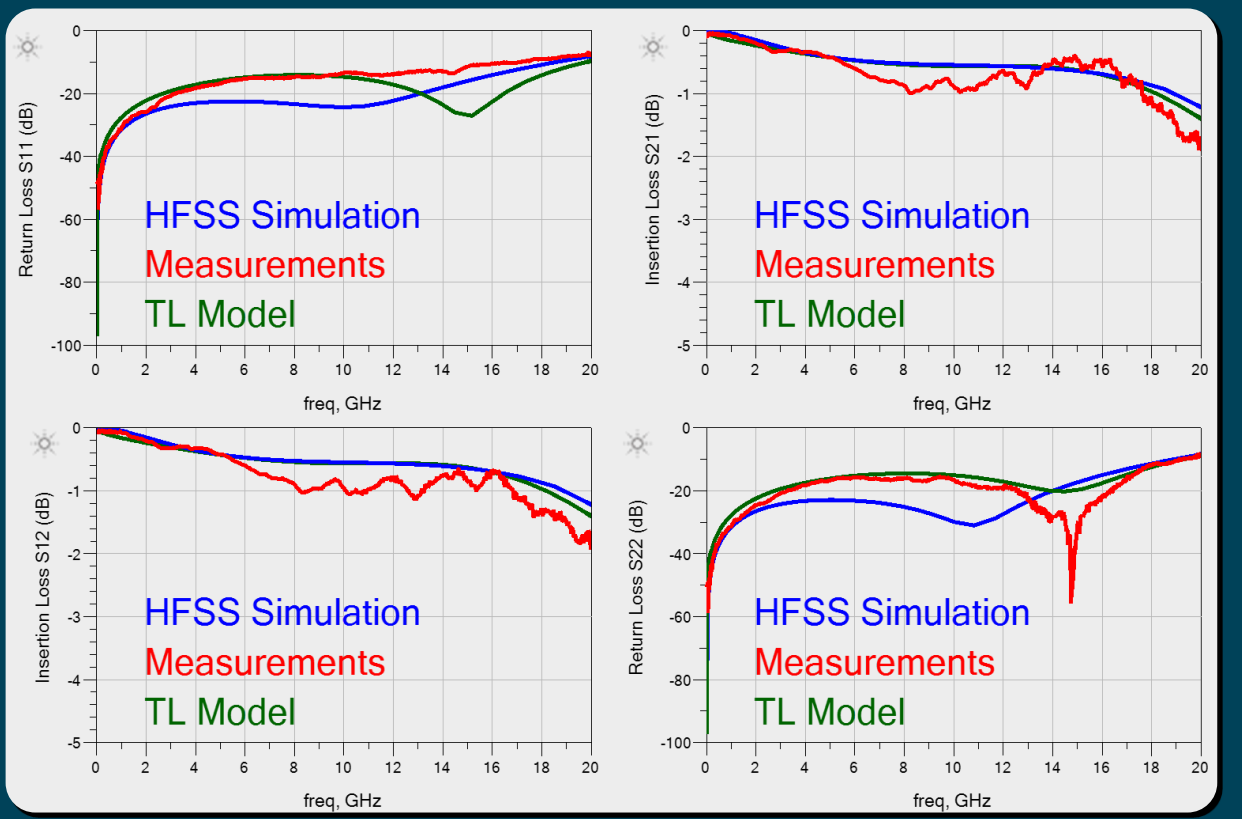
TL Circuit Model



Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Circuit Model & Model Verification

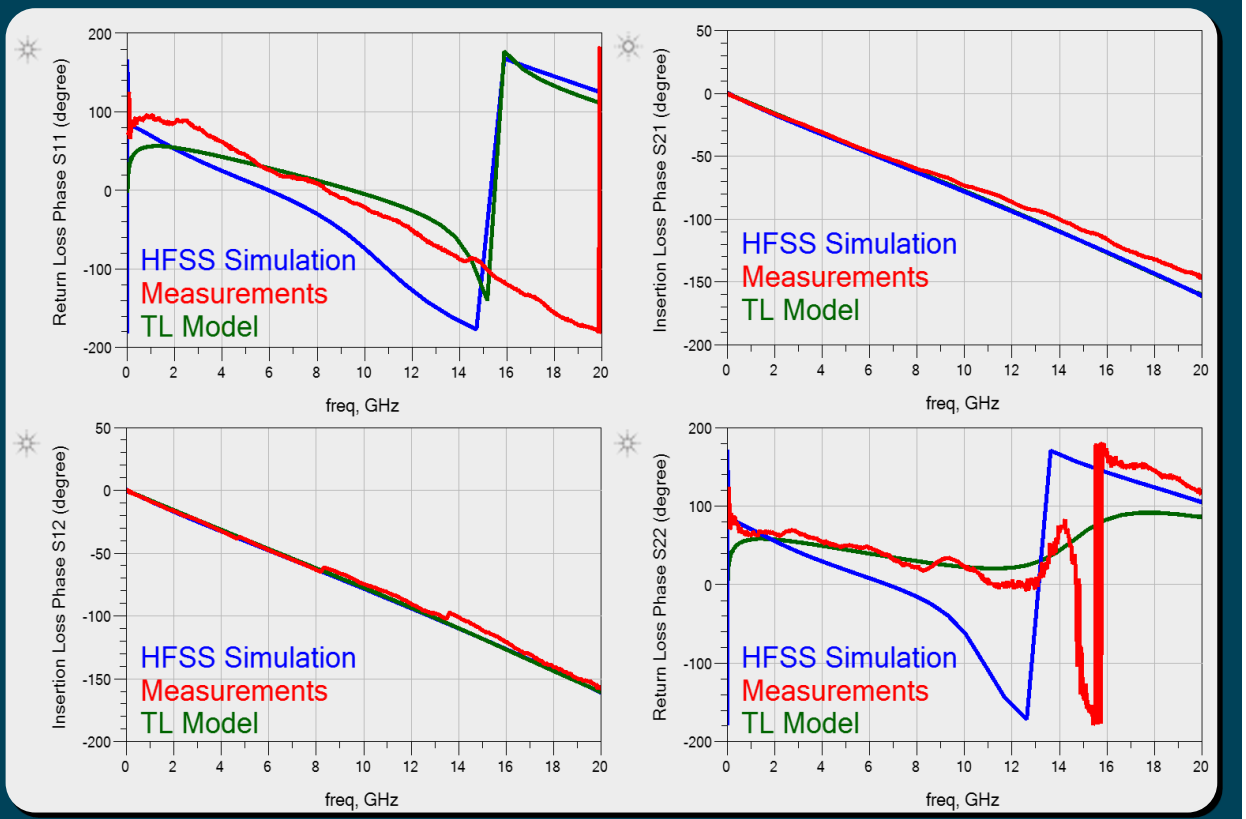
TL Circuit Model



Electrical Circuit Model for Silicon Wafer Spring Pin Probe 24

Circuit Model & Model Verification

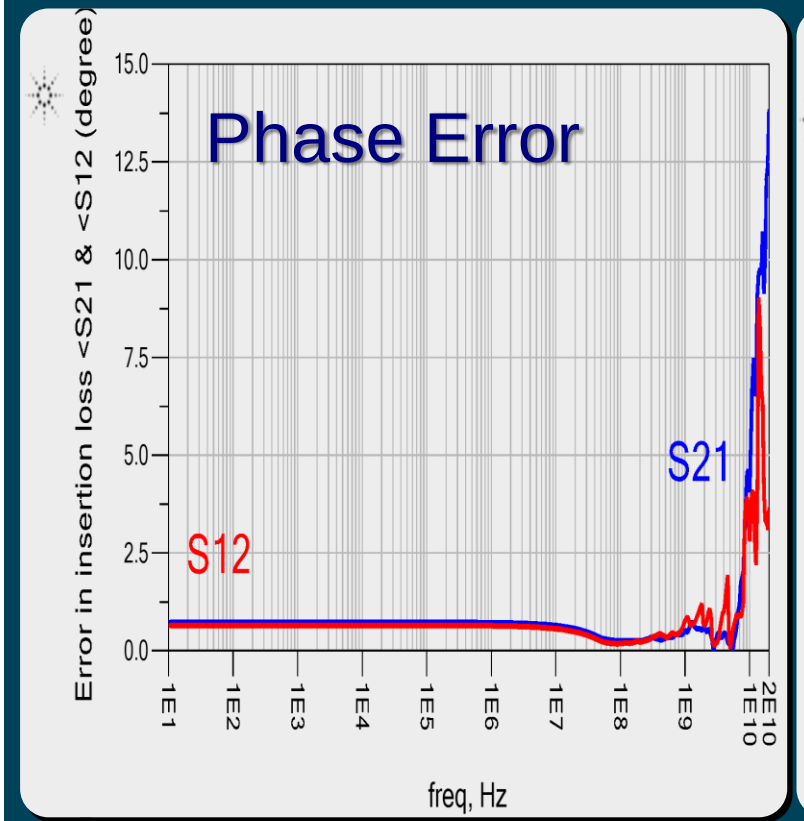
TL Circuit Model

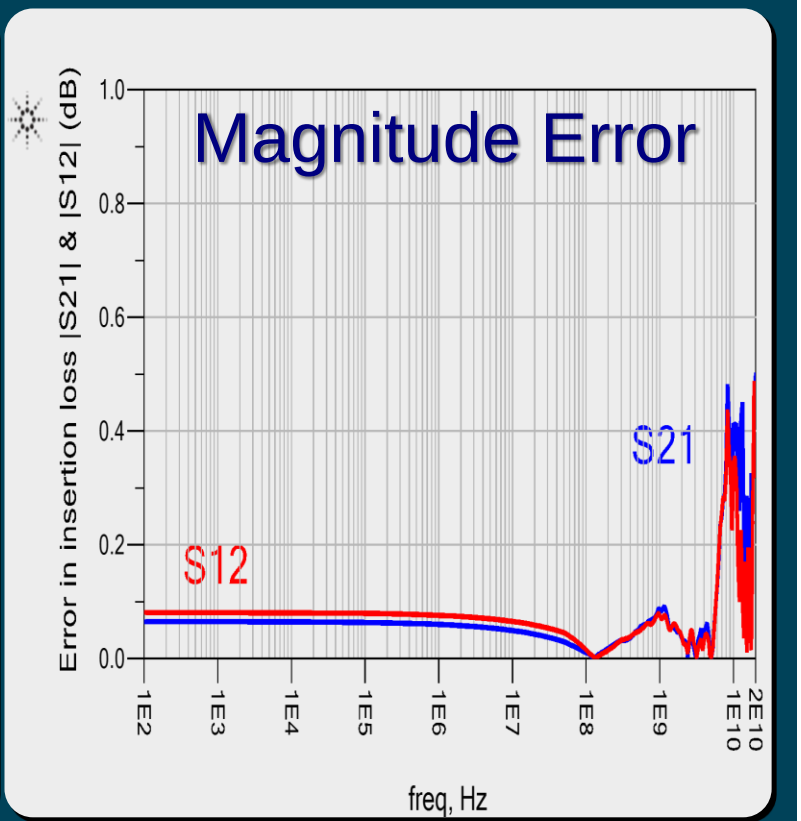


Electrical Circuit Model for Silicon Wafer Spring Pin Probe

Circuit Model & Model Verification

Measurements vs. Model Magnitude & Phase Error





SUMMARY

- Lumped and TL circuit models had been developed using close form Wideband solution.
- Models had been analyzed for 400um probe spacing.
- Models were verified against Spring pin measurements and field analysis simulation results.
- Results show a good match with maximum magnitude error of 0.5dB and phase error of 12 degree at high frequency

CONCLUSION

- Using a closed form model, minimize simulation time and cost.
- Closed form model can be used for quick product feasibility
- Model can be integrated with other probe card components to obtain a full performance prior to manufacturing to minimize risks and Design optimization time delays.
- TL model provides better results compared with lumped circuit model, where distribution effect takes place.

References

- Utkarsh R. Patel, Bjrn Gustavsen, and Piero Triverioyz, “An Equivalent Surface Current Approach for the Computation of the Series Impedance of Power Cables with Inclusion of Skin and Proximity Effects”, IEEE TRANSACTIONS ON POWER DELIVERY, 15 August 2013
- C. R. Paul, Analysis of Multiconductor Transmission Lines, 2nd ed., Wiley, 2007.
- M. M. Al-Asadi, A. P. Duffy, A. J. Willis, K. Hodge, and T. M. Benson, “A Simple Formula For Calculating The Frequency-dependent Resistance Of A Round Wire”, MICROWAVE AND OPTICAL TECHNOLOGY LETTERS, Vol. 19, No. 2, October 5 1998
- Pagnetti, A., Xemard, A., Paladian, F., and Nucci Evaluation of the impact of proximity effect in the calculation of the internal impedance of cylindrical conductors, URSI 2011, Aug. 2011.