
SIXTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 15 - 18, 2015
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Session 3
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Session 3
Valts Treibergs
Session Chair

BiTS Workshop 2015 Schedule

Frontiers Day

Monday March 16 4:30 pm

Wafer Level Pots of Gold

"Coplanarity Analysis of WLCSP Spring Probe Head"

Jiachun (Frank) Zhou , Daniel DelVecchio , & Cody Jacob - Smiths Connectors

"Pushing the envelope in DFM (Design for Manufacturing) for 0.2 mm Pitch WLCSP Socket"

Paul Gunn, Muhammad Syafiq, & Takuto Yoshida - Test Tooling Solutions Group

"Space Transformer PCB For Testing 200 µm WLCSP"

Khaled Elmadbouly - Smiths Connectors

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Space Transformer PCB For Testing 200 µm WLCSP

Khaled Elmadbouly

Smiths Connectors

2015 BiTS Workshop
March 15 - 18, 2015

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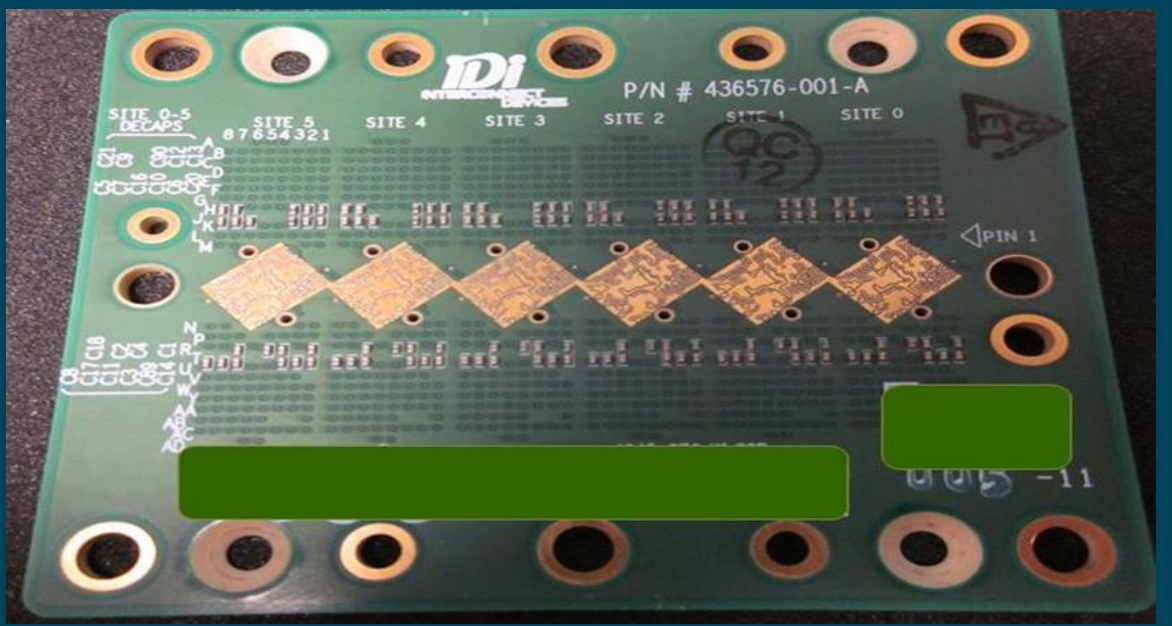
- What is the Space Transformer PCB
- How it gets used in the Probe Head
- Comparing Probe Head with Load Board vs. Traditional Probe Card
- Comparing PCB with MLC and MLO
- The Challenges of PCB
- Test and Validation
- Summary

What is the Space Transformer PCB

Standard pitch extender PCB to fan out the 200um DUT pins to 0.7mm pitch or larger for standard load board fabrication process

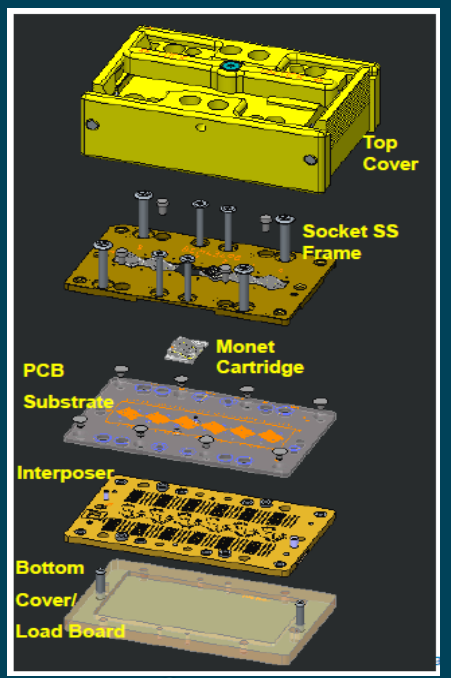


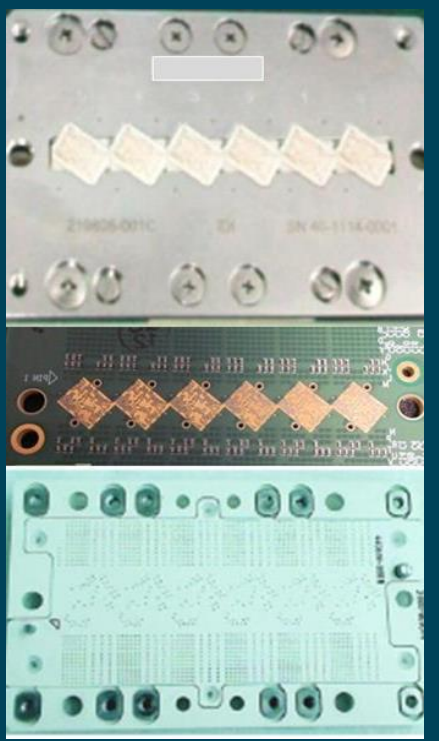
Space Transformer PCB For Testing 200 µm WLCSP

How it Gets Used in the Probe Head

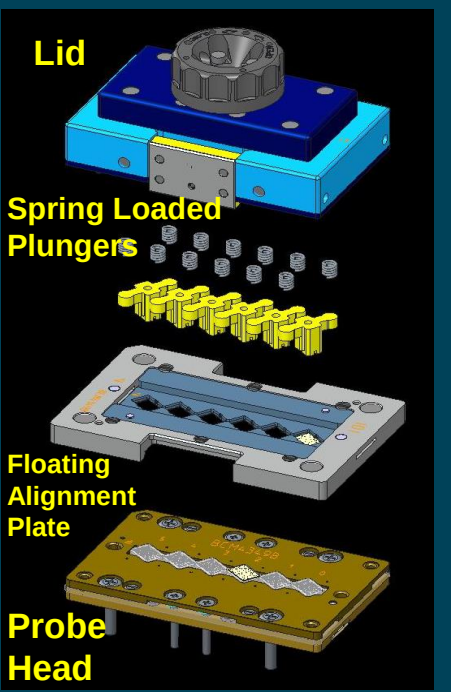
Space transformer connects the Monet 200um probe head to load board through a low profile spring probe interposer

For Probing Wafer





For Final Package Test



Space Transformer PCB For Testing 200 µm WLCSP

Comparing Probe Head with Load Board vs. Traditional Probe Card

Parameter	Load Board with Probe Head smiths connectors Proprietary Design	Traditional Design Probe Card
Application	Probe wafer and final packages	Probe wafer only
Multi-Sites Limitation	No limit (up to max tester resources)	Size restriction for tooling
Maintenance	• Field service repairable • When a probe is damaged, the cartridge for a broken site can be replaced for quick PH recovery	• Non field service repairable • When a probe is damaged, the entire PH is down and need to be replaced
Cost Of Ownership	PH can be refurbished when probes reach end of life	PH will be retired when probes reach end of life
High Speed Signal Integrity	Acceptable	Acceptable
High Power Delivery	Superior	Acceptable

Comparing PCB with MLC and MLO

Parameter	Standard PCB smiths connectors Proprietary Design	MLO (Multi-layer Organic) Thin/ Thick Film Substrate	MLC Multi-Layers Ceramic
Flatness	Acceptable	Need Improvement	Best
Thermal Performance	Acceptable	Need Improvement	Best
Rigidity	Acceptable	Need Improvement	Best
High Power Delivery	Acceptable	Need Improvement	Acceptable
Hole's True Position to Pads	Acceptable	Acceptable	Poor
16-Layers Average Thickness	Acceptable 1.3 to 1.6mm range	Acceptable	Too Thick 3 to 5mm
Via Resistance	Acceptable	Acceptable	High Resistance
High Speed Signal Integrity	Acceptable Up to 6Ghz	Acceptable	Poor

The Challenges of PCB

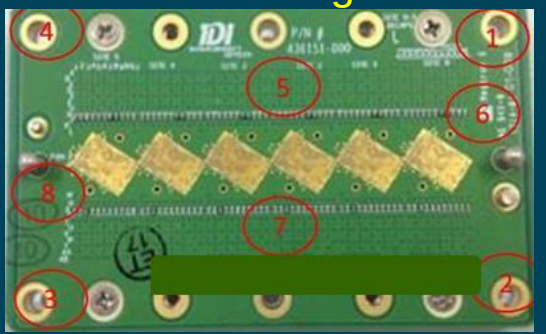
The success of the probe head relies heavily on the success of the space transformer PCB

- PCB flatness will have big effect on tip to tip coplanarity of the probe head (first to last touch)
- Alignment hole true position accuracy is very critical for pin to pad alignment
- RF signals need special routing

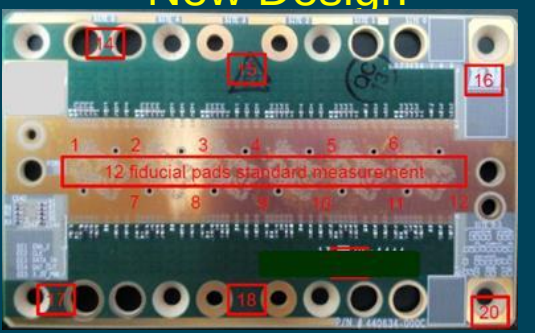
PCB Flatness

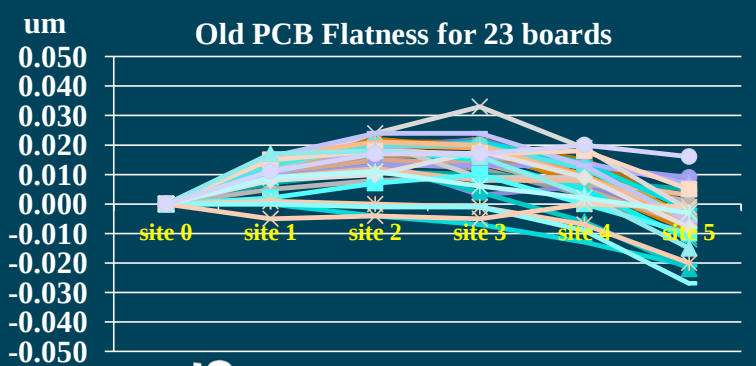
- The old design PCB had a flatness issue in the same direction of the bowing induced by the spring probe interposer preload.
- The new design PCB with controlled thieving and solder mask improved flatness by 10um and is now in the opposite direction of interposer bowing and preload

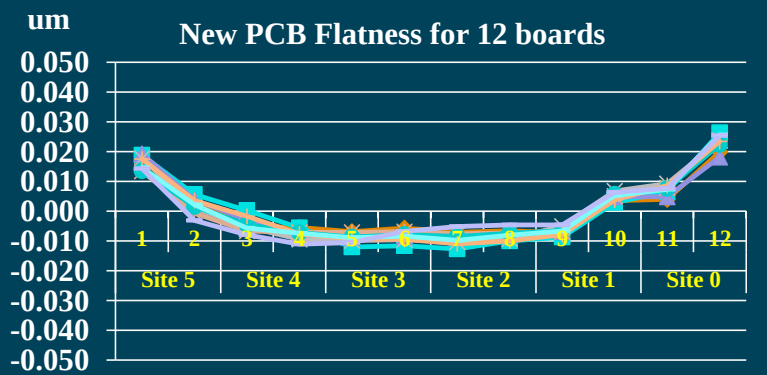
Old Design



New Design







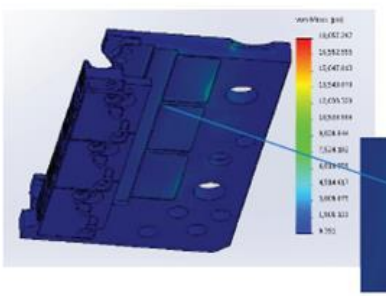
Space Transformer PCB For Testing .2mm WLCSP

Probe Head Flatness

The new SS frame structure and the improved PCB flatness design contributed significantly to reduce the bowing by 30um

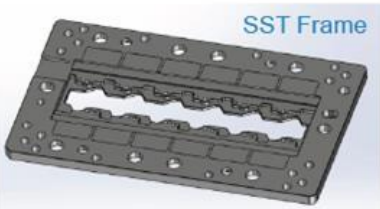
Analysis & Results (623-0249-13)

smiths connectors



Stress:

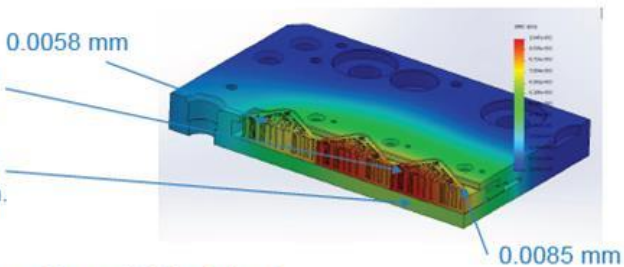
The maximum stress is 18.1 kpsi for 249-13 pin and 24.1 kpsi for 249-02 pin for which yields the safety factor of (31.2/18.1=) 1.7 and (31.2/24.1=) 1.3.



Deformation:

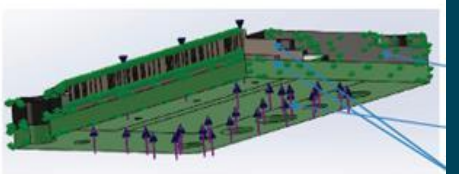
The maximum deformation of Monet cartridge is 0.0103 mm

The maximum deformation of interposer board is 0.0070 mm.



(The vonMises stress criteria is used to predict the failure)

Boundary Conditions



Ceramic Peek; SST; PCB R5775

Bolted - Fixed Support

Symmetry (Quarter model is used)

Pre-Load: Monet/PCB-101972-000; Total: 2430

Test-Force: PCB-623-0249-02/13; Total 1521

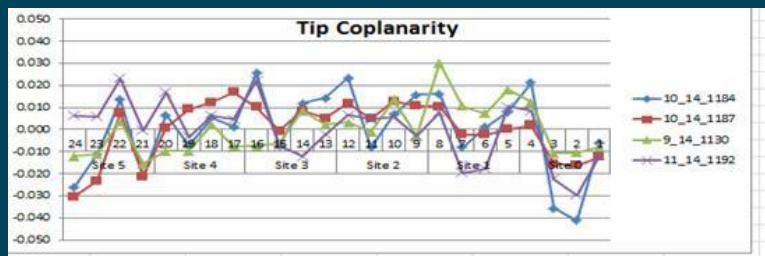
Spring Connector (not shown)

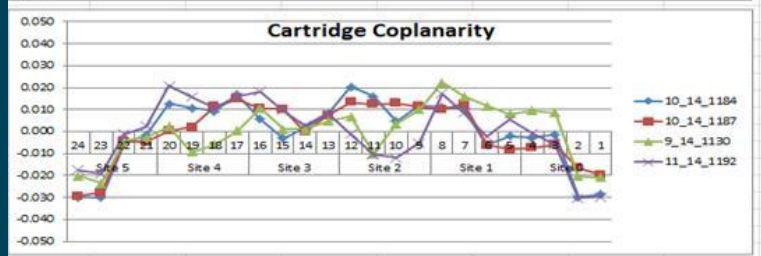
Gap/Contact

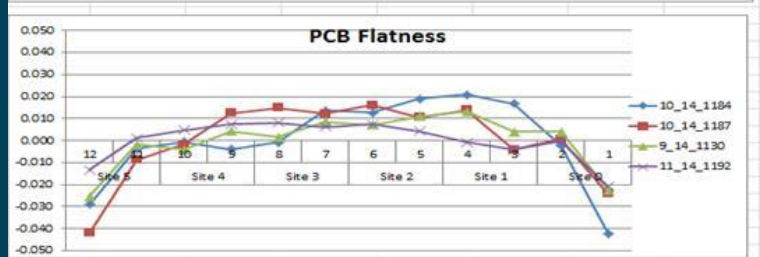
Probe Head & PCB Flatness

The overall PH coplanarity and the bowing was reduced by 30um after improving the structure of the PH frame and PCB flatness.

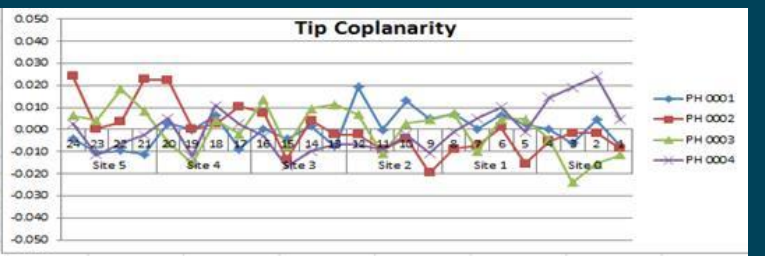
4 PH using the Old PCB design

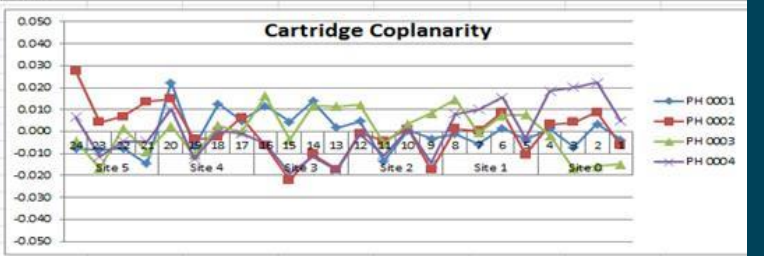


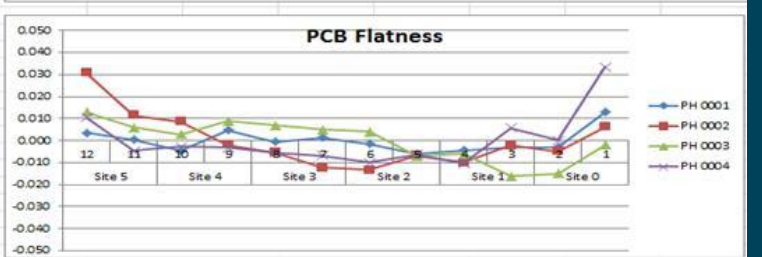




Same PH using the New PCB design

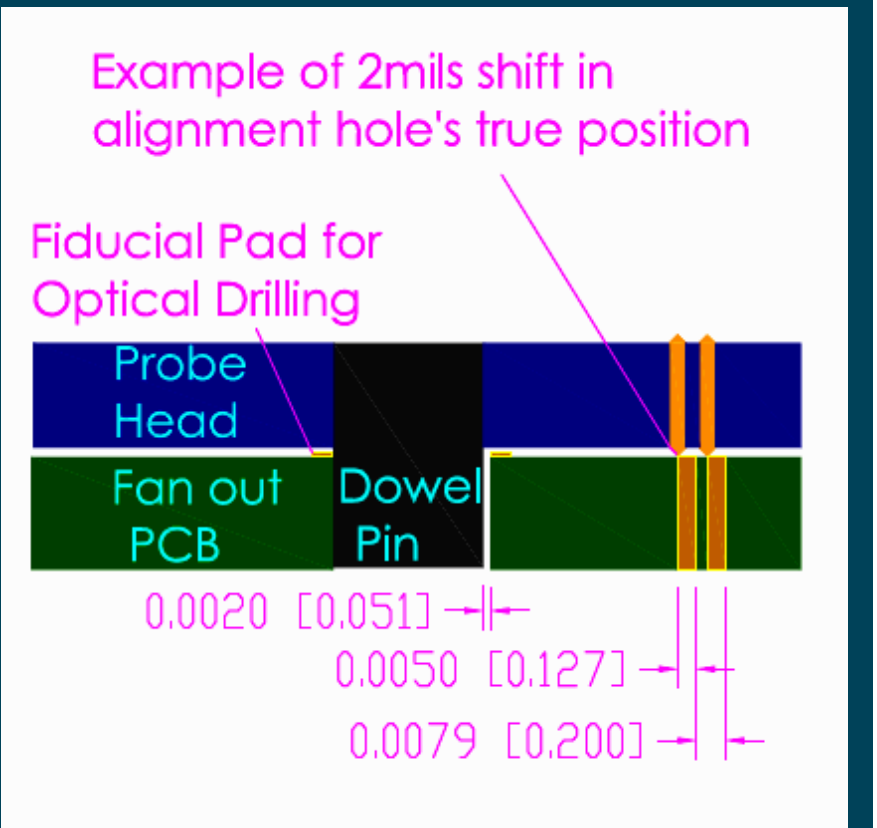






Alignment Hole True Position

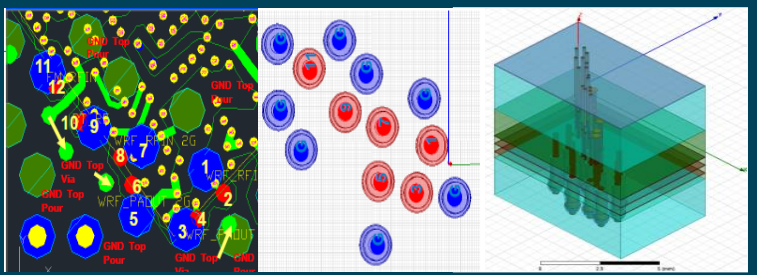
Placing fiducial pads around alignment holes in PCB with true position of +/-0.001" is a standard practice for POP interposer PCB, however for these 200um WLCSP PCB, the target pad is too small, therefore we developed additional fiducial pads to achieve precision PH optical alignment



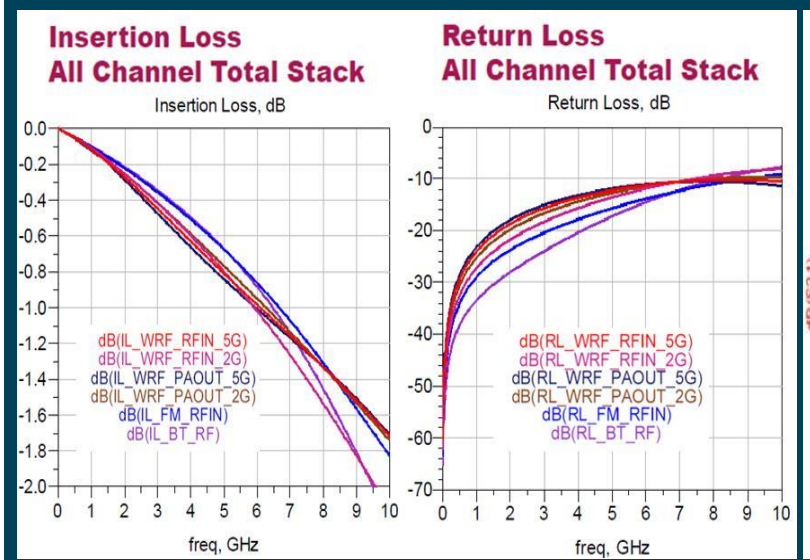
RF Signal Routing

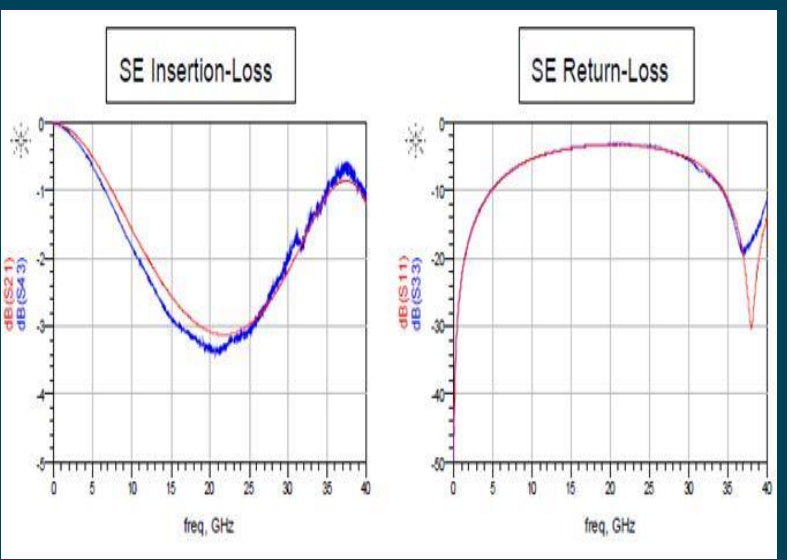
Developed special routing for RF signal to meet 6GHz speed requirement.

This routing was simulated then verified by actual measurement not only for the PCB but also for the entire Probe Head



Simulation vs Actual Measurements: IL: -1 dB, 6.8GHz; RL: -10dB, 6.0GHz





Test and Validation

Design and set up 4-wire Kelvin Cres board to measure leakage and 100% Cres for every space transformer PCB and probe head

Space Transformer PCB For Testing 200 µm WLCSP

Test and Validation

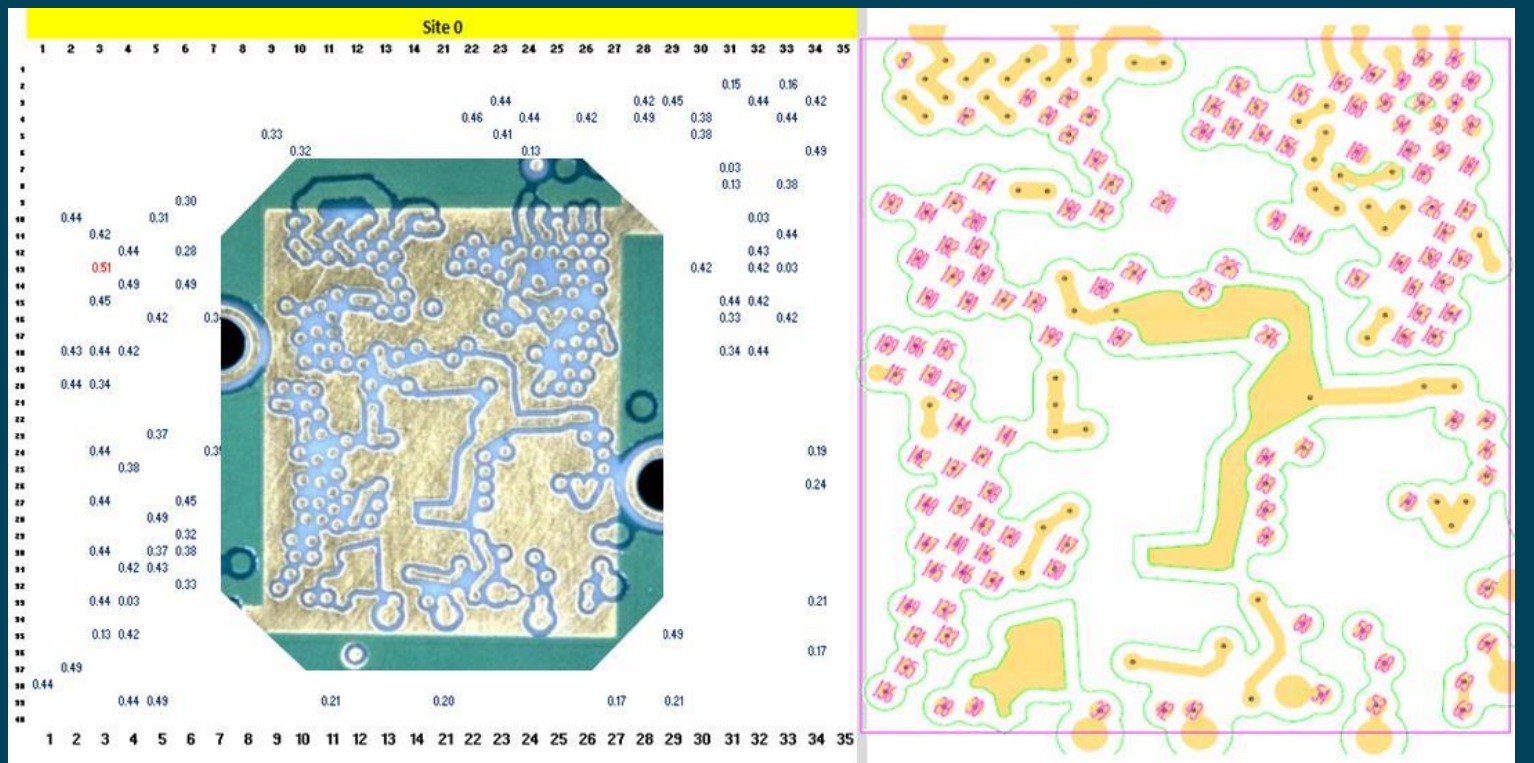
Example of Cres report for each probe head

WLCSP- 395 - 0.2mm 6-Sites Cres Report PH_SN 40-0814-1142 08/05/2014						SN# 1123			SN# 1165			SN# 1142			SN# 1151			SN# 1143			SN# 1146		
RF Avrg Cres					0.257	0.236	0.234	0.234	0.273	0.273	0.235	0.297	0.311	0.282	0.230	0.226	0.258	0.262	0.287	0.260	0.217	0.230	0.208
RF STD DEV					0.069	0.047	0.052	0.046	0.071	0.057	0.063	0.071	0.089	0.084	0.060	0.065	0.123	0.073	0.074	0.066	0.047	0.052	0.033
Signal Avrg Cres					0.433	0.449	0.453	0.429	0.419	0.438	0.412	0.454	0.464	0.447	0.408	0.418	0.404	0.435	0.451	0.431	0.414	0.430	0.405
Signal STD DEV					0.094	0.079	0.098	0.080	0.074	0.068	0.068	0.107	0.105	0.107	0.112	0.115	0.114	0.095	0.098	0.097	0.072	0.074	0.074
Socket Cres Criteria's					Avrg Cres	Max Cres	High Cres Pins	Site 0			Site 1			Site 2			Site 3			Site 4			Site 5		
Qty.	0.8mm Pin Name	Type	Net Name	0.2mm Bumps Number	0.500	1.000	35	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3
1	1	RF01	PCIE_TDN0	5	0.298	0.428		0.235	0.250	0.255	0.239	0.234	0.258	0.337	0.428	0.280	0.355	0.334	0.353	0.270	0.373	0.262	0.349	0.289	0.263
2	2	RF02	PCIE_TDP0	6	0.236	0.357		0.232	0.256	0.237	0.274	0.287	0.281	0.221	0.357	0.235	0.201	0.195	0.194	0.233	0.297	0.216	0.172	0.193	0.171
3	3	RF03	PCIE_RDP0	8	0.245	0.337		0.268	0.290	0.337	0.244	0.166	0.195	0.289	0.326	0.267	0.206	0.117	0.208	0.240	0.330	0.330	0.201	0.215	0.182
4	4	RF04	PCIE_RDN0	9	0.247	0.323		0.265	0.299	0.229	0.204	0.283	0.231	0.307	0.323	0.265	0.182	0.253	0.178	0.302	0.279	0.296	0.194	0.178	0.169
5	5	RF05	USB3_TDP	21	0.251	0.318		0.273	0.316	0.233	0.218	0.271	0.155	0.211	0.301	0.312	0.318	0.316	0.293	0.201	0.231	0.185	0.266	0.215	0.205
6	6	RF06	USB3_TDN	22	0.259	0.371		0.219	0.212	0.214	0.352	0.364	0.317	0.325	0.371	0.297	0.203	0.171	0.194	0.250	0.252	0.244	0.223	0.213	0.235
69	E06	AC	BT_REG_ON	320	0.357	0.447		0.377	0.385	0.328	0.342	0.361	0.339	0.426	0.410	0.393	0.284	0.313	0.303	0.415	0.447	0.377	0.291	0.360	0.270
70	E07	AC	GPIO_13	182	0.390	0.510		0.429	0.360	0.461	0.375	0.417	0.382	0.352	0.352	0.326	0.324	0.362	0.339	0.473	0.510	0.478	0.345	0.367	0.372
72	E09	AC	RF_SW_CTRL_12	184	0.392	0.474		0.410	0.393	0.365	0.395	0.382	0.370	0.406	0.404	0.407	0.354	0.358	0.337	0.379	0.388	0.364	0.474	0.448	0.426
73	E10	AC	RF_SW_CTRL_8	181	0.352	0.433		0.343	0.353	0.345	0.310	0.433	0.320	0.340	0.384	0.304	0.379	0.372	0.359	0.373	0.427	0.392	0.311	0.285	0.302
74	E11	AC	RF_SW_CTRL_4	86	0.350	0.439		0.387	0.392	0.439	0.385	0.318	0.377	0.370	0.370	0.363	0.307	0.369	0.325	0.302	0.279	0.313	0.339	0.343	0.318
75	F02	AC	PACKAGEOPTION_2	131	0.363	0.511		0.325	0.341	0.293	0.305	0.364	0.381	0.351	0.418	0.328	0.267	0.344	0.344	0.489	0.511	0.463	0.324	0.366	0.324
77	F06	AC	GPIO_2	220	0.411	0.540		0.512	0.540	0.430	0.384	0.441	0.401	0.319	0.325	0.385	0.429	0.377	0.398	0.402	0.413	0.437	0.426	0.414	0.362
78	F08	AC	GPIO_12	199	0.320	0.479		0.334	0.343	0.337	0.268	0.325	0.263	0.306	0.343	0.273	0.252	0.250	0.247	0.430	0.479	0.449	0.268	0.324	0.268
130	PS15	PS15	P15_PCIEUSB_AVDD1P2		0.053	0.112		0.055	0.072	0.037	0.020	0.037	0.041	0.012	0.112	0.093	0.073	0.044	0.047	0.045	0.037	0.089	0.056	0.052	0.038
131	PS16	PS16	P16_USB2_AVDD33		0.208	0.379		0.189	0.211	0.141	0.093	0.177	0.112	0.274	0.218	0.231	0.379	0.321	0.303	0.161	0.205	0.168	0.189	0.191	0.175
134	PS19	PS19	P19_VDDIO		0.054	0.103		0.090	0.036	0.014	0.091	0.089	0.016	0.072	0.024	0.100	0.037	0.012	0.103	0.060	0.066	0.059	0.024	0.018	0.058
135	PS20	PS20	P20_WRF_SYNTH_VDD3P3		0.206	0.316		0.273	0.267	0.242	0.162	0.178	0.202	0.227	0.316	0.267	0.176	0.167	0.141	0.159	0.160	0.214	0.179	0.183	0.190
136	PS21	PS21	P21_AVDD3P3		0.121	0.176		0.087	0.103	0.126	0.079	0.127	0.089	0.111	0.139	0.175	0.107	0.176	0.157	0.100	0.140	0.126	0.082	0.136	0.123
137	PS22	PS22	P22_VDDIO_RF		0.100	0.169		0.110	0.085	0.091	0.090	0.045	0.130	0.067	0.066	0.103	0.153	0.050	0.086	0.165	0.169	0.106	0.082	0.113	0.087
140	PS25	PS25	P25_BT_VDDC		0.053	0.114		0.042	0.056	0.040	0.039	0.046	0.041	0.047	0.114	0.069	0.057	0.044	0.038	0.035	0.030	0.078	0.051	0.055	0.075
141	PS04	PS04	WRF_XTAL_VDD1P2_SEN	254	0.217	0.314		0.240	0.314	0.185	0.206	0.221	0.177	0.229	0.225	0.220	0.241	0.146	0.156	0.224	0.242	0.235	0.223	0.218	0.209
142	PS08	PS08	VOUT_LNLDO_SENSE	351	0.248	0.324		0.311	0.281	0.269	0.207	0.233	0.256	0.322	0.324	0.310	0.198	0.235	0.150	0.240	0.262	0.237	0.214	0.193	0.227
143	PS09	PS09	VOUT_BT LDO 2P5_SENSE	362	0.271	0.486		0.433	0.486	0.315	0.234	0.244	0.221	0.319	0.341	0.263	0.199	0.233	0.203	0.206	0.186	0.233	0.246	0.259	0.256
154	GND1		X1_GND_754		0.016	0.029		0.000	0.029	0.020															

Cres Report | Leakage Report | 395_0.2mm Pin Map | Cres_Socket_Measurements | LKG_Socket_Measurem

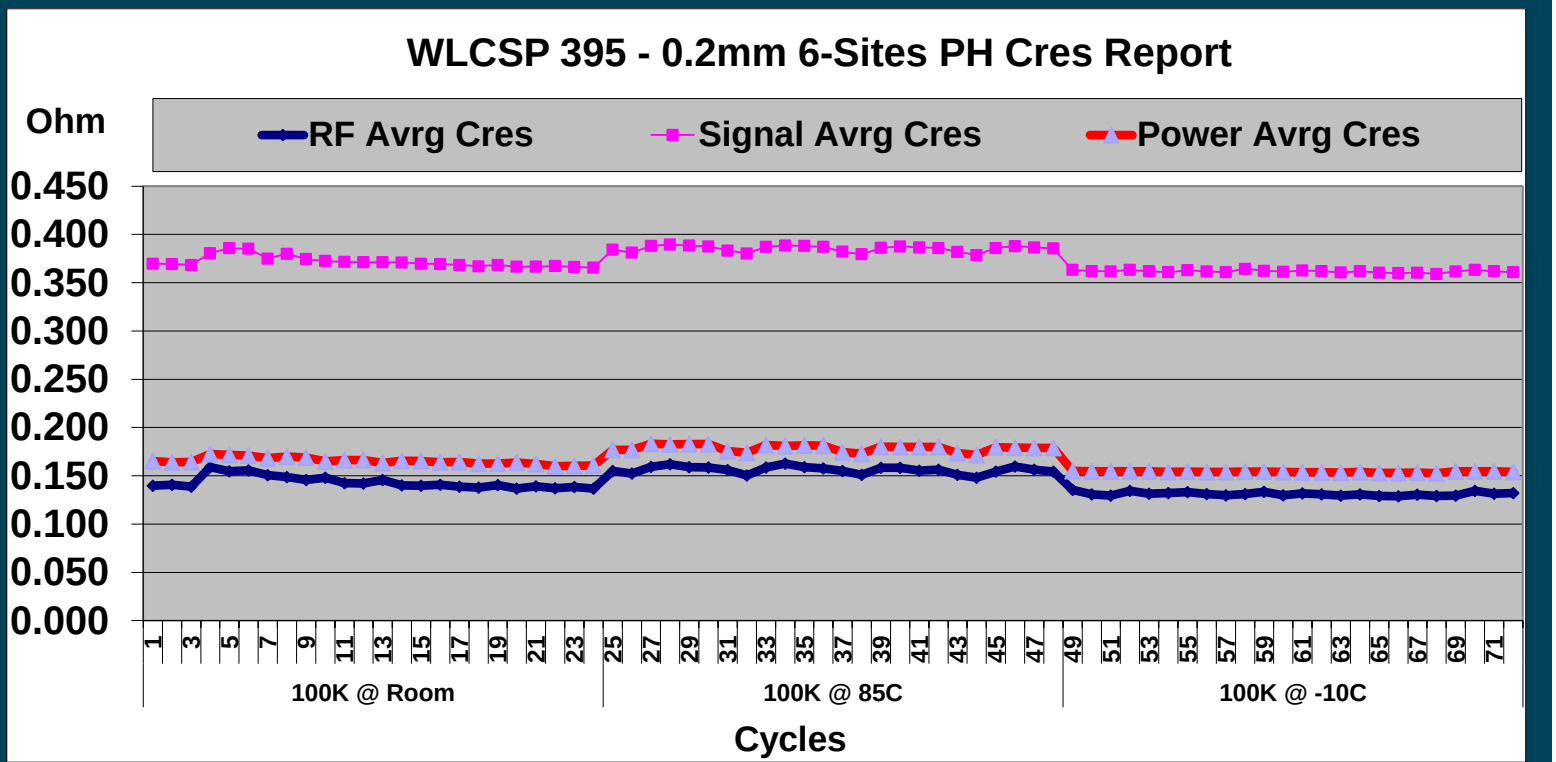
Test and Validation

Example of a device pin map showing the Cres measurement of the exact location of each bump, to check any failing via, pad or pin



Test and Validation

Example of first article PH validation to verify the space transformer PCB and the PH can withstand the 300K cycles at room temp, 85C and -10C



Summary

- Over the past several years, development of this type of fan out PCB that gets integrated into PoP test sockets has been very successful, and more recently has been adapted to probe heads for multi-site ≥200um WLCSP
- The design standards of this space transformer PCB have been developed in such a way as to ensure precision alignment in HVM environment and in consideration of PCB fabrication, yield, and tolerances
- Overall performance is very satisfactory while there is still room for improvement, moving forward for the next generation Probe Head.