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Session 3

Valts Treibergs

Session Chair

**BiTS Workshop 2015 Schedule** 

# Frontiers Day

Monday March 16 4:30 pm

#### **Wafer Level Pots of Gold**

"Coplanarity Analysis of WLCSP Spring Probe Head"

Jiachun (Frank) Zhou, Daniel DelVecchio, & Cody Jacob - Smiths Connectors

"Pushing the envelope in DFM (Design for Manufacturing) for 0.2 mm
Pitch WLCSP Socket"

Paul Gunn, Muhammad Syafiq, & Takuto Yoshida - Test Tooling Solutions Group

"Space Transformer PCB For Testing 200 μm WLCSP"

Khaled Elmadbouly - Smiths Connectors



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# Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket

Paul Gunn, Muhammad Syafiq, Takuto Yoshida **Test Tooling Solutions Group** 



2015 BiTS Workshop March 15 - 18, 2015

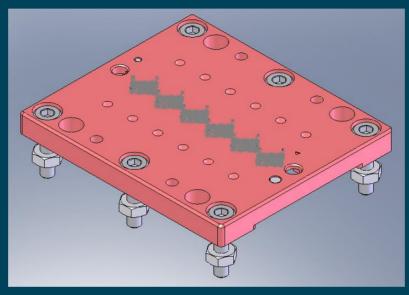


#### **Contents**

- Socket 1 Design
- Improved Socket 2 Design
- First FEA Simulation for Socket 2
- FEA Simulation Improvement
- Compare FEA Simulation and Actual Measurement
- Improved Socket 3 Design
- Conclusion



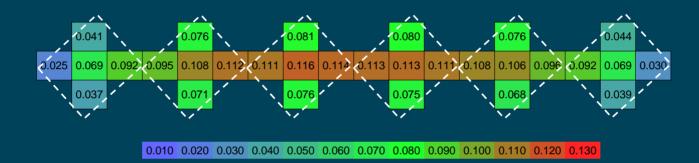
## **Socket 1 Design**



- Total 1656 pins for 6 devices
- 1 Top Plate (TP) Design
- Socket side 6x M3 screws to keep TP coplanar at pin areas
- Without FEA



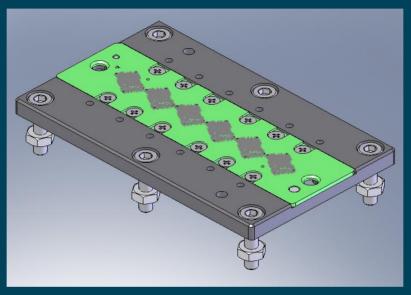
# **Socket 1 Coplanarity Measurement**



- Target 0.050mm for coplanarity
- Max. 0.116mm coplanarity from measurement
- Warpage trend shows at center area
- TP hardness is not enough
- Tight screws is far from pin areas
- FEA is required for next design



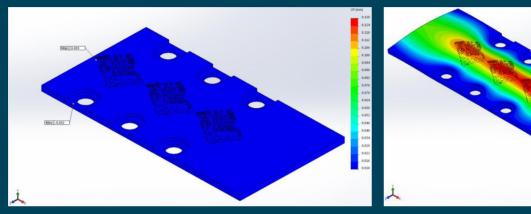
## **Improved Socket 2 Design**



- Total 2370 pins for 6 devices
- **Improvements** 
  - Stainless Steel Holder & Ceramic Peek TP
  - 12x TP screws closer to pin area
  - Design with FEA simulation



## First FEA Simulation for Socket 2



**Nominal Case** 

**Worst Case** 

Items	Nominal Case	Worst Case
Coplanarity of TP [mm]	0.011	0.158

- Coplanarity values are different in nominal and worst case
- We estimated actual coplanarity close to nominal case



## **Socket 2 Coplanarity Measurement**



0.010 0.020 0.030 0.040 0.050 0.060 0.070 0.080 0.090 0.100 0.110 0.120 0.130

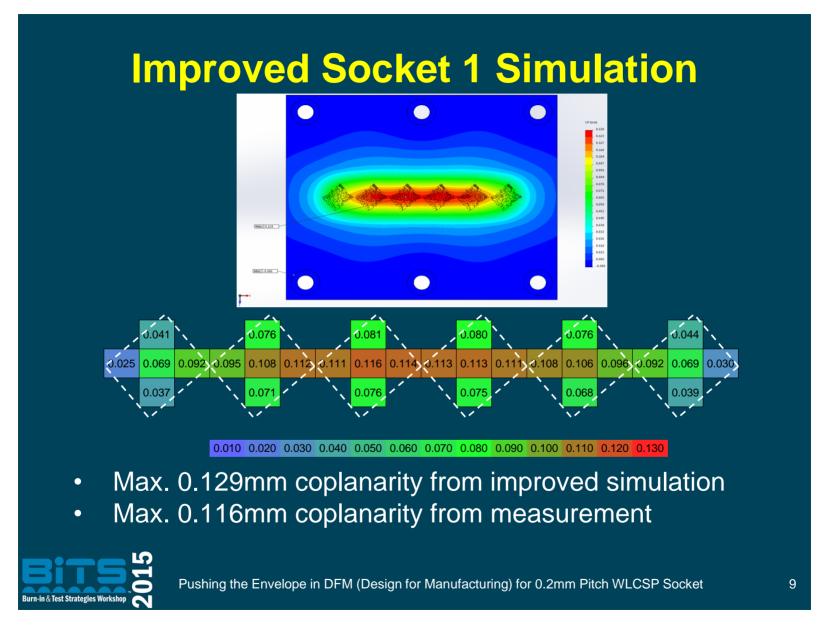
- Target 0.050mm for coplanarity
- Max. 0.125mm coplanarity from measurement
- Coplanarity measurement close to worst case
- Need to improve the FEA

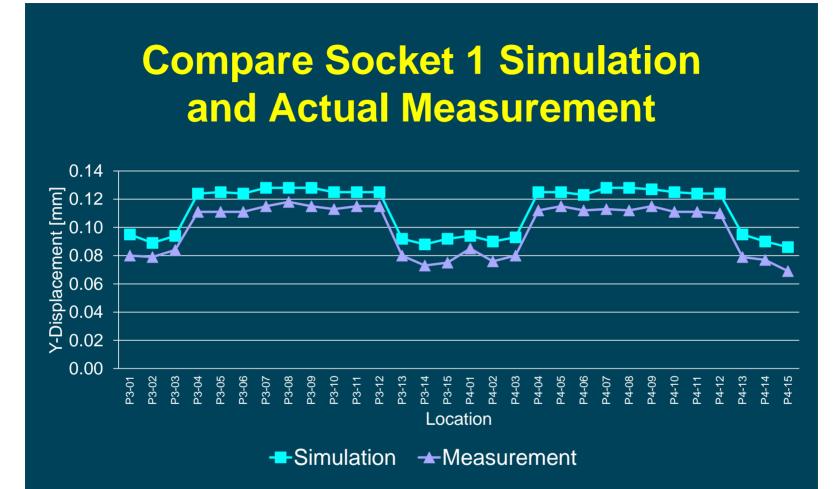


## **FEA Simulation Improvement**

- Implement elastic membrane technique
  - To predict deformation
  - To predict stress values
- Elastic membrane technique provides
  - More stiffness reliability
  - More robust design
- Refer to Prabakaran and Pal, Finite Element Analysis using Elastic Membrane Technique for Test Socket Design Optimization (BiTS, 2008)



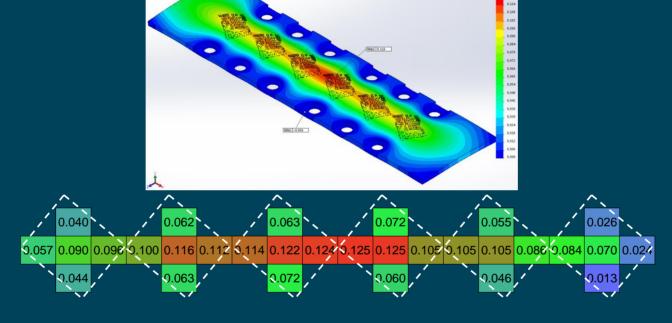




Coplanarity error rate is 20% or less



# **Improved Socket 2 Simulation**



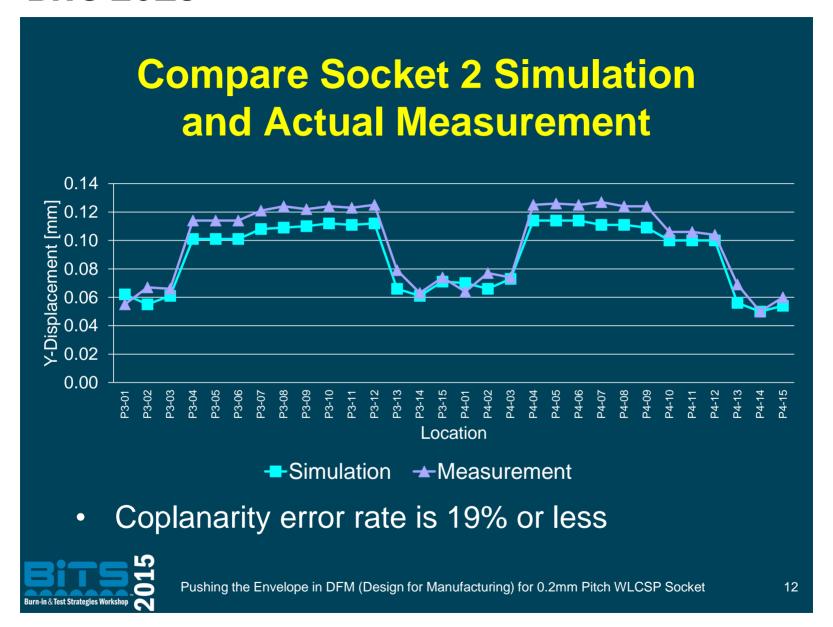
0.010 0.020 0.030 0.040 0.050 0.060 0.070 0.080 0.090 0.100 0.110 0.120 0.130

- Max. 0.116mm coplanarity from improved simulation
- Max. 0.125mm coplanarity from measurement

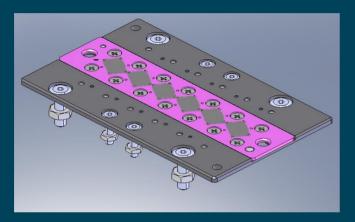


Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket

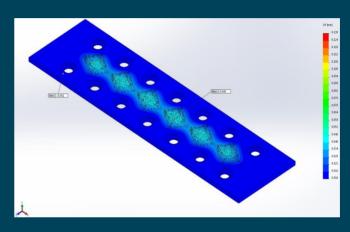
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# **Improved Socket 3 Design**



Socket Design



Improved Simulation

- Total 2430 pins for 6 devices
- Target 0.050mm for coplanarity
- Max. 0.046mm coplanarity from improved simulation



Pushing the Envelope in DFM (Design for Manufacturing) for 0.2mm Pitch WLCSP Socket

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Wafer Level Pots of Gold - Wafer Level Chip Scale Packaging (WLCSP)

## Conclusion

- FEA simulation using Elastic Membrane technique proves good DFM relationship between design to actual socket
- FEA provides more robust design and stiffness to enhance product reliability



Wafer Level Pots of Gold - Wafer Level Chip Scale Packaging (WLCSP)

## Reference

Prabakaran and Pal, 2008, Finite Element Analysis using Elastic Membrane Technique for Test Socket Design Optimization, Burn-In and Test Socket Workshop, Hot Topics Session

