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BiTS

Burn-in & Test Strategies Workshop™

March 15 - 18, 2015

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Session 2

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Session 2

Mike Noel
Session Chair

BiTS Workshop 2015 Schedule

Frontiers Day

Monday March 16 1:30 pm

Spanning the Socket Rainbow

"Contacting Solutions for High Power Bare Die Testing (IGBT MOS-FET and Diodes)"

Markus Wagner - Cohu SEG

"Comparison of Different Methods in Determining Current Carrying Capacity of Semiconductor Test Contacts"

Valts Treibergs - Xcerra Corporation

"Are New Temperature Test Strategies Needed? Meeting Performance and Cost Requirements of Today's Applications"

Andreas Nagy - Xcerra Corporation

"Extreme Temperature and High Current Testing Challenges of Automotive Devices"

Praveen kumar Ramamoorthy & Murad Hudda - Infineon Technologies
Dan Maccoux & Muhamad Izzat bin Roslee - JF Microtechnology

BiTS 2015 Burn-in & Test Strategies Workshop

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BiTS Burn-in & Test Strategies Workshop 2015

Contacting solutions for high power KGD testing (IGBTs, MOS-FETS and Diodes)

Markus Wagner
Cohu ITS

2015 BiTS Workshop
March 15 - 18, 2015

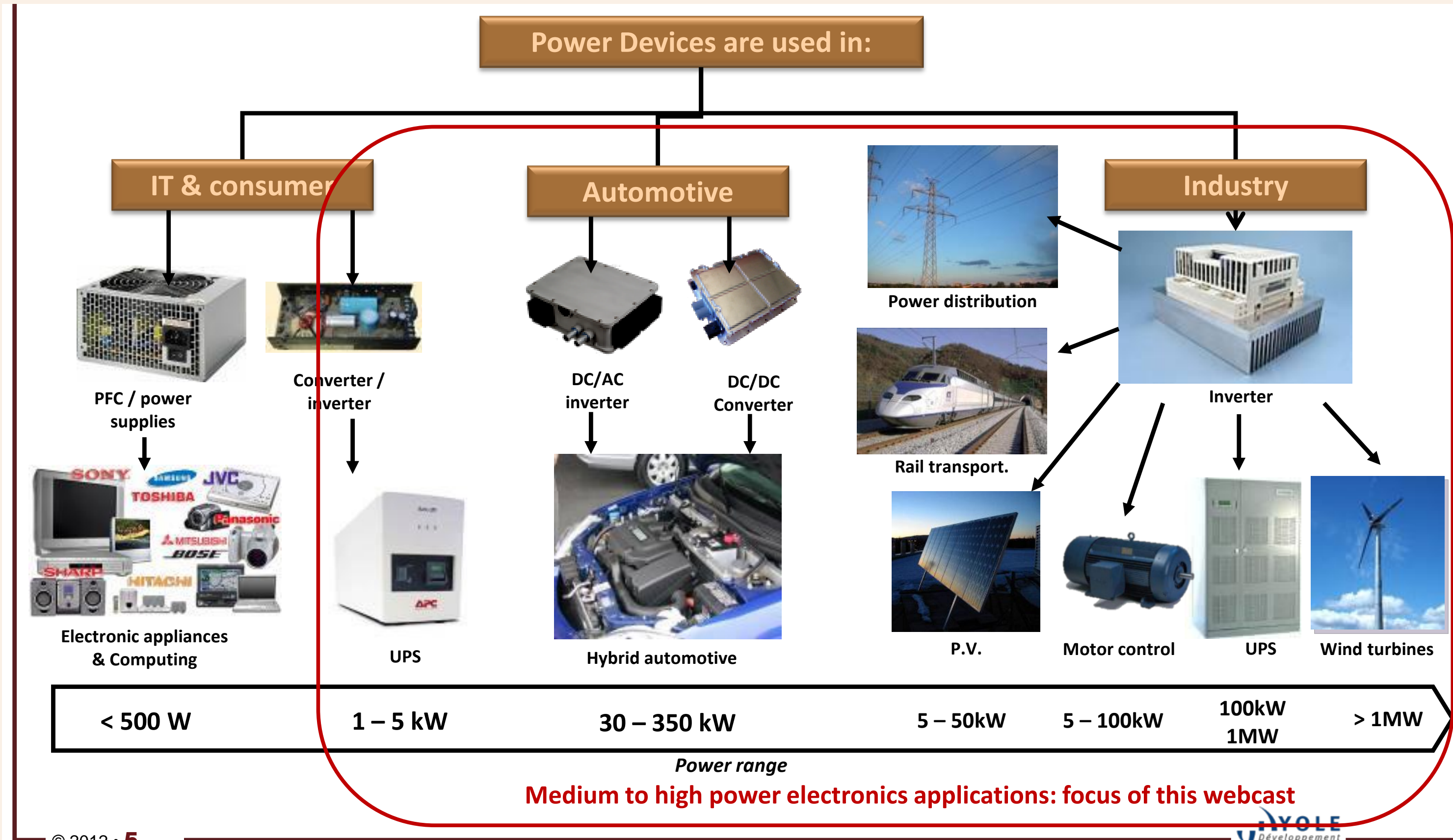
Contents

- Industry trends
- Issues to solve
- Requirements
- Solutions
  - Spring probes (type, coatings and probe layout)
  - Cantilever springs (type, coatings and layout)
  - Yield booster
- System solution
- Summary and outlook

Industry Trends

- Power KGD/bare dies are basic building blocks of power modules
- Applications are IT and consumer, as well as automotive, industrial and renewable energy applications such as solar inverters and wind applications
- Technical trends: constantly increasing current density and voltage

Industry Trends

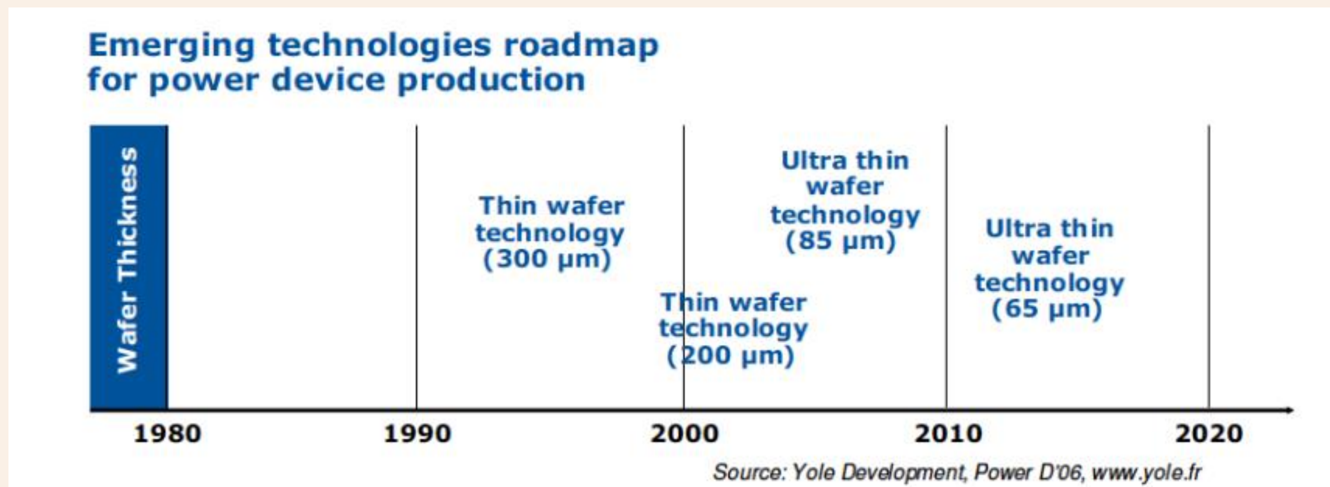


Industry trends

- What is driving KGDs?
- High costs are associated with uncontrolled defects that are not discovered until final test.
- The cost of rework or scrap can completely overwhelm the benefits of using direct die-attach in the first place.

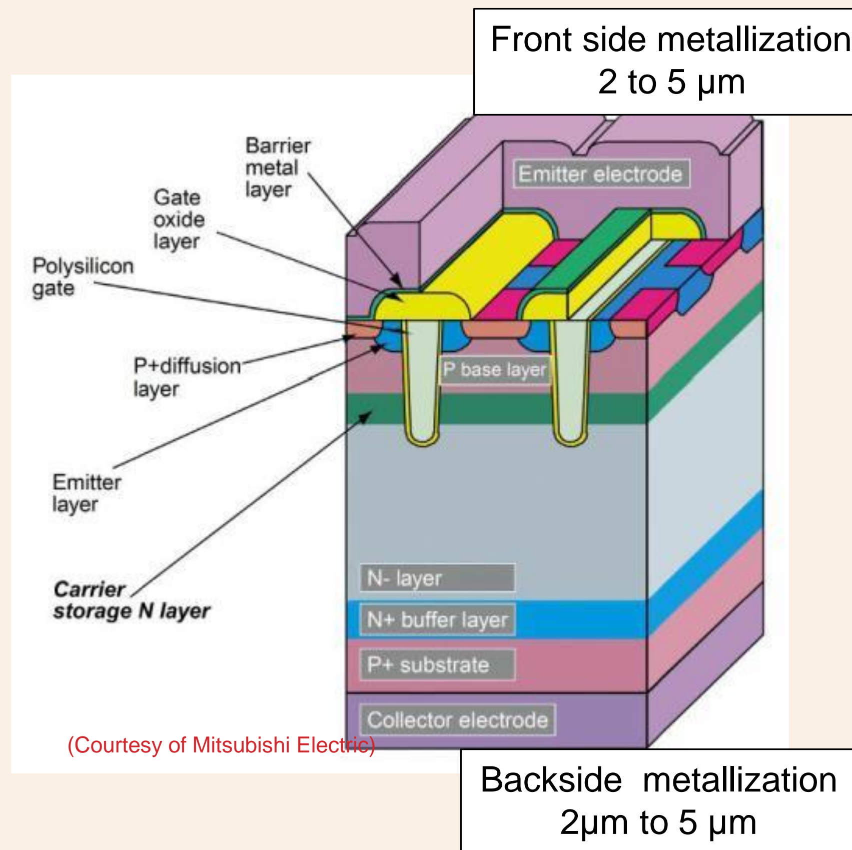
Issues – thin dies

- 100 µm and thinner – desirable for heat dissipation and packaging
- Uneven contacting forces can bend or break dies under test



Issues – thin metallization

Front side metallization
2 to 5 µm



(Courtesy of Mitsubishi Electric)

Backside metallization
2µm to 5 µm

Issues – thin metallization

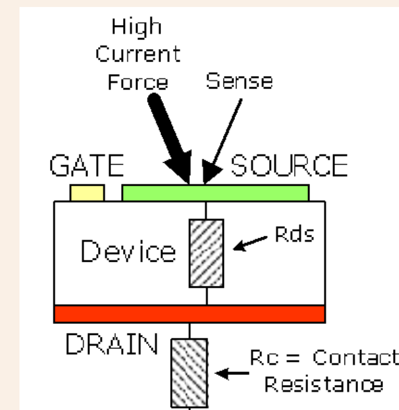
- Bare die metallization
  - Different metallization topology of bare dies and molded devices
  - Most metallization are PVD sputtered surfaces with a total thickness of 2 µm to 5 µm

Coatings	IGBT	MOS-FET	Diode	Molded package
Backside metallization	• Ti - NiV – Ag • Ti - AuSn	• Ti - NiV – Ag • Ti - AuSn	• Ti/Ni/Ag or CrNiAg for wire bonding • Ni/Au or Ti/Ni/Ag for soldering	n.a.
Front side metallization	• AlCu (5 µm) • CuXx	AlCu (5 µm)	• Ti/Al, Ti/Ni/Al or Pure Al or Al (1%Si) for wire bonding • Ni/Au or Ti/Ni/Ag or CrNiAg for soldering	Lead/pad coating: Pure tin (7-15 µm) or NiPdAu (30-100 nm)
Passivation		nitride (only on edge structure)		n.a.

Issues - Measuring Rds(on)

- Power MOSFET development is confronted with the conflicting demands of providing increasing efficiency and power ratings, while using shrinking process geometries. Therefore the device Rds(on) values are constantly driven down

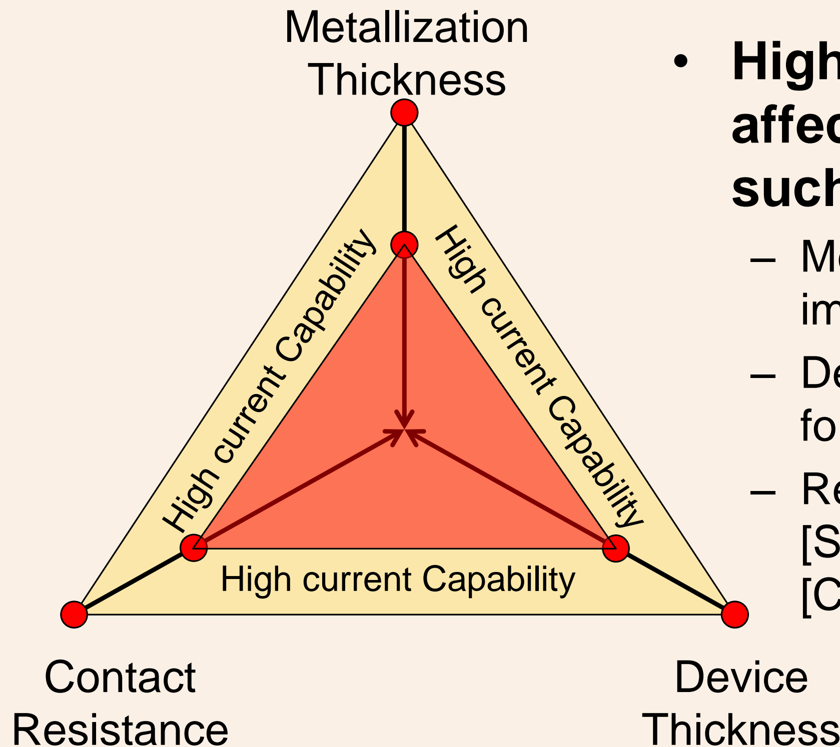
- Rds(on) is a key parameter for power MOSFET KGD sorting
- Kelvin contactors to measure Rds(on) < 10 mΩ



Requirements – contacting

Test parameters	IGBT	MOS-FET	Diode
Max. current	100 A	250 A $_{Drain}$	400 A
Max. voltage range	1200 V (1700 V, 5th generation)	650 V $_{Drain\ to\ Source}$ 1700 V for SIC	1600 V
Min. device thickness	120 µm	70 µm	100 µm
Metallization thickness	2 to 10 µm	2 to 10 µm	2 to 10 µm
Min. resistance	< 10 mΩ	< 10 mΩ	< 10 mΩ
Subsequent processes	MCP/MCM/…	MCP/MCM/….	MCP/MCM/….

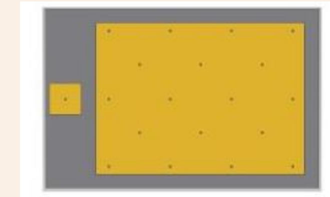
Requirements – high test current

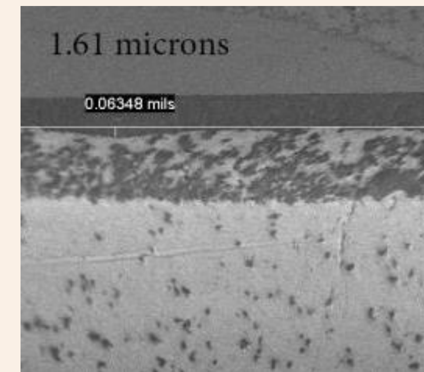


- **High current capability is affected by several factors such as:**
  - Metallization thickness→ max. imprint depth
  - Device thickness → max. contact force
  - Resistance R = R_T [Trace] + R_S [Surface contamination] + R_C [Constriction resistance]

Requirements – metallization protection

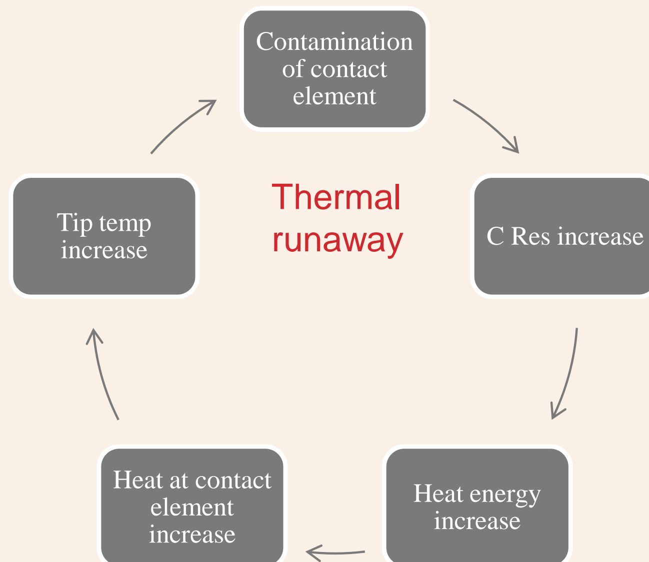
- To avoid injuring the underlying layers, only a very small imprint depth is allowed
- Imprint depth = 0.4 times metallization thickness →~2µm
- Homogeneity and repeatability of imprint depth is achieved by:
  - Same low contact force for each probe
  - Identical contact tip geometry for each probe
  - Tight co-planarity of all contact probes (<10 µm)
  - Planar support for the die under test (<5 µm)
  - Controlled plunger stroke:
    - Defined deceleration with no vibration
    - Smooth touchdown to penetrate oxide layer
    - High positioning accuracy

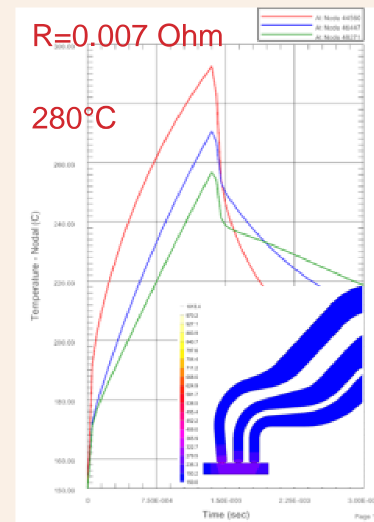


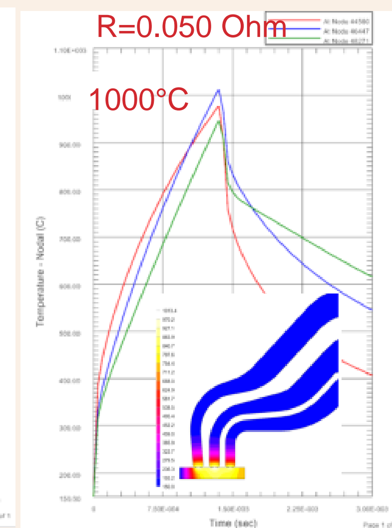


Requirements – low Cres

- In General
  - lowering the on-state resistances of a power devices improves its performance. Therefore Rds(on) is a key parameter for power-device manufacturers

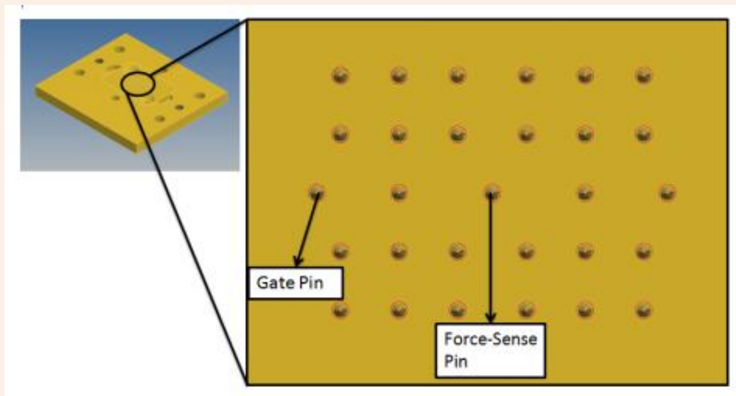






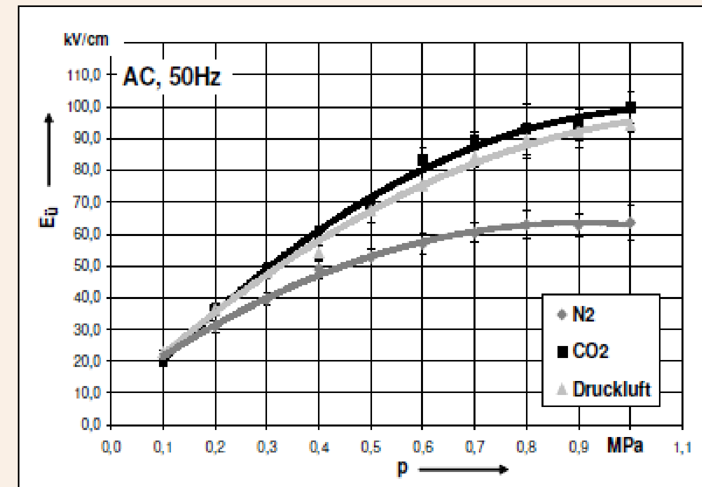
Solution – low Cres

- Minimal contact resistance achieved by:
  - Self cleaning of contact elements (scrub)
  - Appropriate contact material and coating to avoid contamination
  - Automatic cleaning procedures between lots
  - Distribution of current over multiple contact elements plus increased contact area
  - Good heat dissipation - Thermal absorption
  - Non-oxidizing environment during contacting - Yield booster



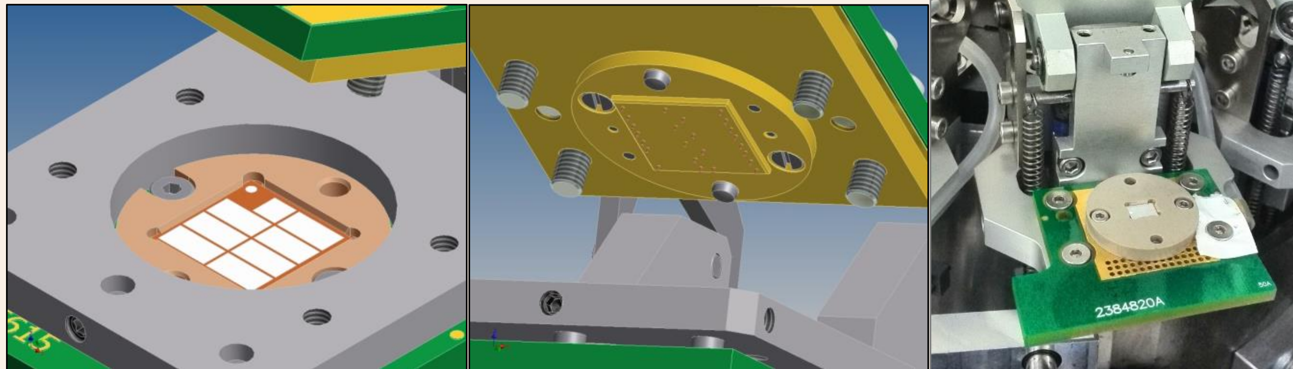
Solution – High voltage breakdown

- High voltage tests are required to measure the device leakage behavior
- Design requirements to prevent voltage breakdowns:
  - Materials with high dielectrically strength
  - Pressurized test environment with N_2, CO_2 or air
  - Special design for contactor parts to avoid:
    - Corona effect →
      - Rounded tip shape
    - Inner partial discharge →
      - Homogeneous materials
      - Vacuum potting
    - Surface discharge →
      - Clean environment,
      - Controlled humidity



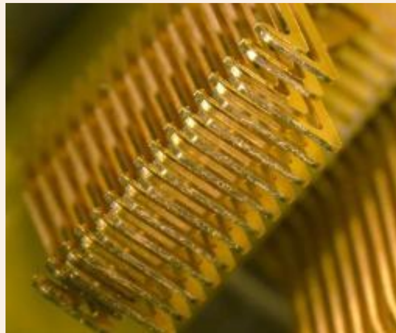
Solutions – spring probes

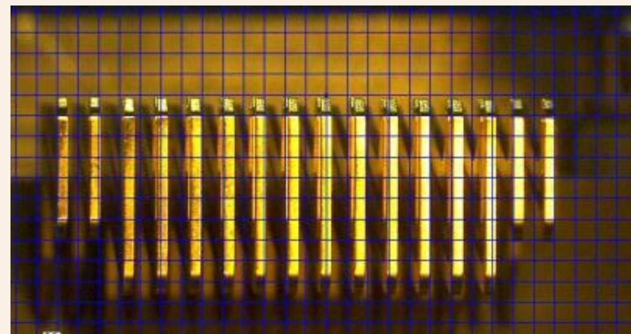
- Characteristics spring probes:
  - Probe life time ~0.3 k – 0.6 k insertions
  - Inexpensive standard buying
  - Typical continuous current capacity ~2-3 Ampere/pin
  - No relative movement – scrub
  - current path can vary between pins



Solutions – Cantilever contact

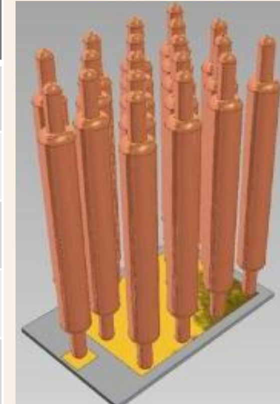
- Characteristics of cantilever springs:
  - High co-planarity of all contact elements is achieved through preload and with high precision manufacturing for probes and sockets
  - Defined current path with high current density through a "one piece" contact element
  - Very low contact force to avoid metallization damage and to penetrate oxide layer (defined relative movement – scrub)
  - Self cleaning through optimized tip geometry and scrub

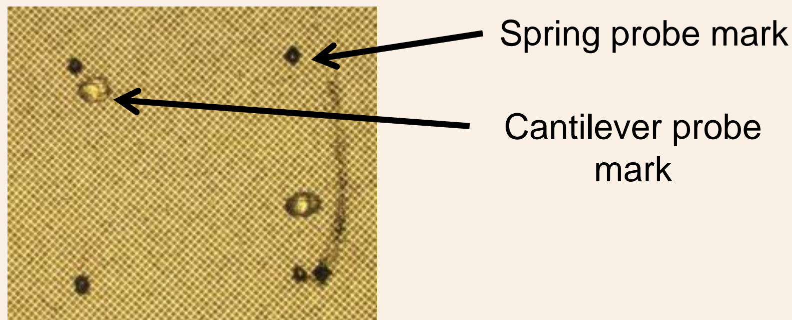




Solutions - Cantilever vs. spring probe

Test parameters	Spring probe	cantilever
Contact area	0.002 mm² @ 0.05dia	0.005 mm²
Force	0.3N	0.2N
Imprint depth	1.5 µm	1.5 µm
Contact pressure	150 N/mm²	40 N/mm²
Current density @ 4A	2500 N/mm²	800 A/mm²



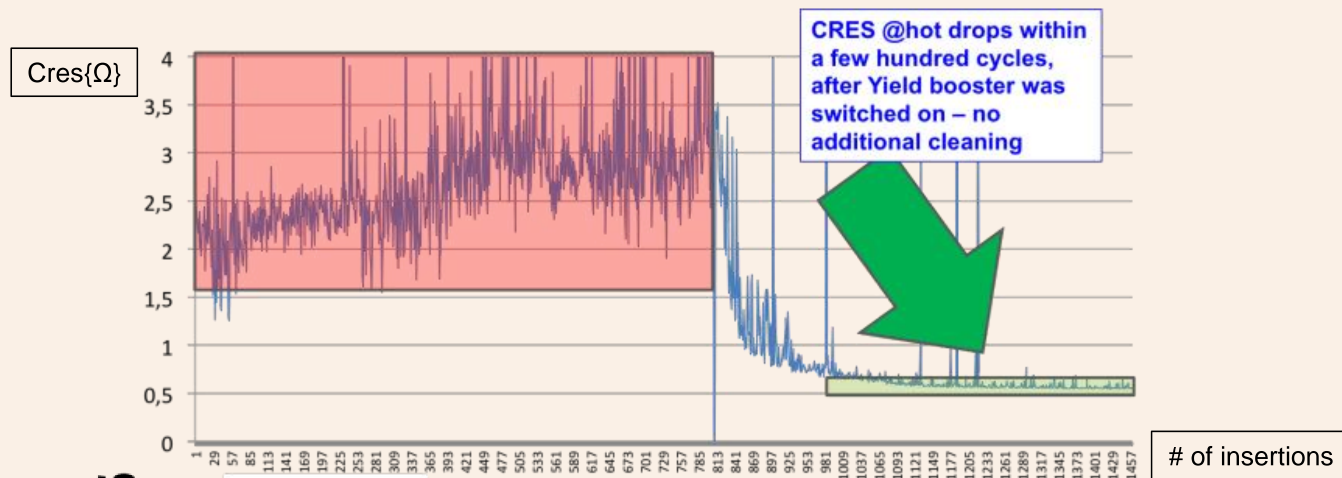


Conclusion: due to a larger contact area and a lower contact pressure, cantilever contact element causes less mechanical and thermal stress

Solutions - Yield booster

- Yield booster, maintaining low Cres

  purging the contact/test area with inert gas @ hot
  - Stabilizes Cres at a low level over 100k+ insertions
  - Increases cleaning frequency to > 100k insertions
  - Reduces surface wear of contact spring tips by factor 2
  - Results in higher live time + better yield + less downtime

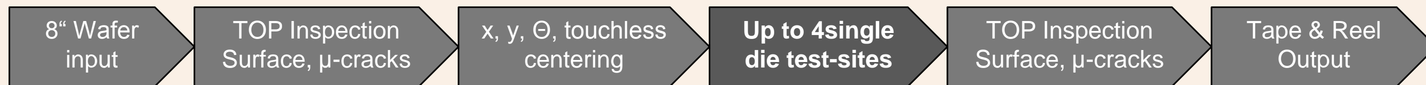


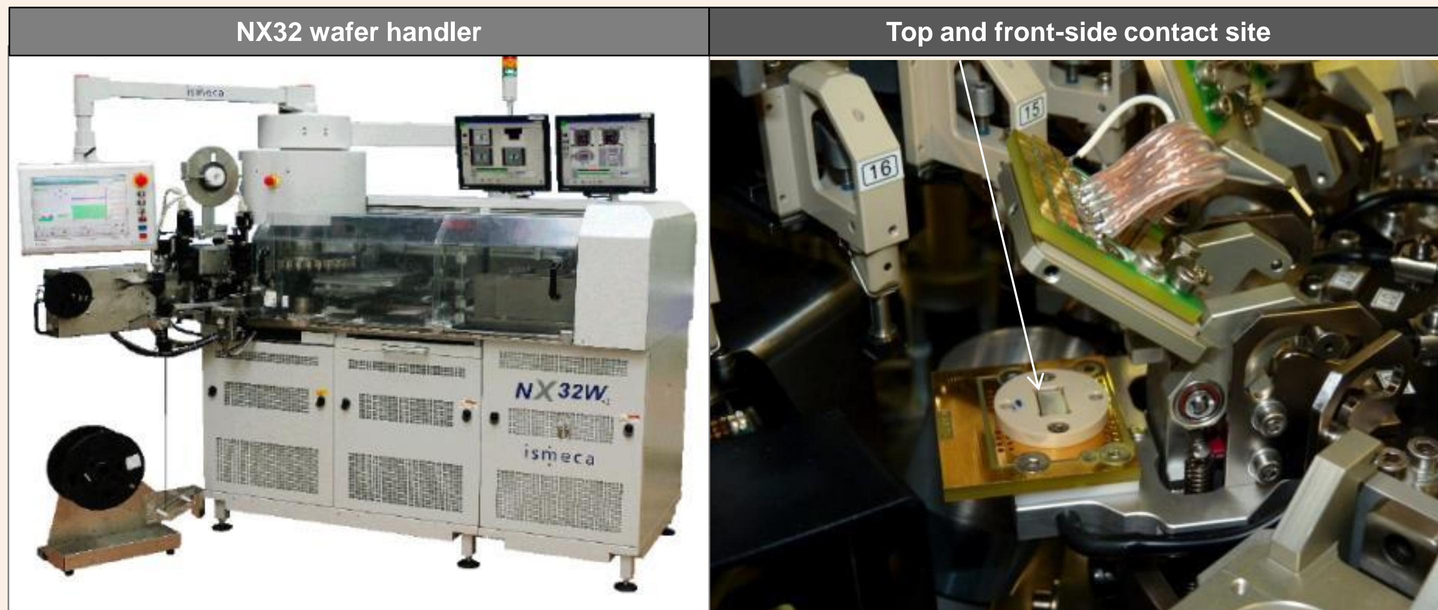
Solution - summary

parameter	Yield boost	cantilever	Spring probes
High current capability	green	green	yellow
High Voltage test capability	green	yellow	yellow
Contamination of contact elements	green	yellow	yellow
Cres	green	green	yellow
Homogenous force distribution	n/a	green	yellow
Imprint position accuracy	n/a	green	green
Imprint depth	green	green	green

A combination of yield booster and cantilever probes delivers a high yield, low maintenance contacting solution for High Power KGDs

Solution – typical handling system





Summary

- Benefits of bare die level testing
  - Less complex and faster module-level testing
  - Higher module yield and less rework costs
- Differences in KGD versus molded package testing
  - Different metallization materials, even for back and front side
  - Very Sensitive to imprint depth and position
  - Contradicting requirement of a low force shallow imprint and a high current carrying capability
  - Downstream processes e.g. wire bonding, flip chip or soldering influence the type of die metallization and contacting
  - Need for new contactor materials, coatings and tip geometries