SIXTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop™

March 15 - 18, 2015

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Session 1

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Session 1

Marc Mössinger
Session Chair

BiTS Workshop 2015 Schedule

Frontiers Day

Monday March 16 10:30 am

Putting MEMS to the Test

"'Taking MEMS Test and Calibration to the Next Level' - An Integrated Platform Approach Driving Further MEMS Growth“

John Rychcik - Xcerra Corporation

"The Target for Consumer MEMS Testing Should Be Under 1 Cent Level"

Vesa Henttonen - Afore Oy

"MEMS IC Manufacturing Test Cost Effective Strategies"

Wendy Chen & Andrei Berar - KYEC

"BURst Pressure (BURP) Stress Test for MEMS Pressure Sensors"

Peter Jones & Ray Sessego - Freescale Semiconductor

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The target for consumer MEMS testing should be under 1 cent level

Vesa Henttonen
Afore Oy

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UNIT PRICE EROSION

- MEMS is the fastest growing part of the semiconductor field showing double digit growth numbers despite sinking unit prices.
- The most of the growth comes from Consumer electronics such as mobile phones and in the near future from different kind of wearables.
- PRICE DILUTION! $25 -> $2.5 -> $0.25 ->???
- Must have an effect to testing too

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MEMS TESTING CHALLENGES

- Yet, every sensor has to be tested, with the real physical stimulus
- Many of the test methods origin from the "old days"
  - What has happened to COT?
- Market demands for more economical ways to test
  - COT/cost price > 30% is intolerable
  - 1 cent COT is a common target. Why not less!

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MEMS TESTING CHALLENGES

- Miniaturization of sensors, new package technologies
  - WLP, CSP
  - Complicated handling
  - Chipping
  - Alignment

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WAYS TO CUT THE COT

Most of the COT depends on investment cost and capacity of the test system. The ways to cut the COT must concern those issues:

1. **Increase the throughput – more parallelism**
2. **Shorten the process – savings in other machinery**
3. **Optimize the system for MEMS – optimal tester**

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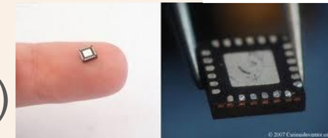
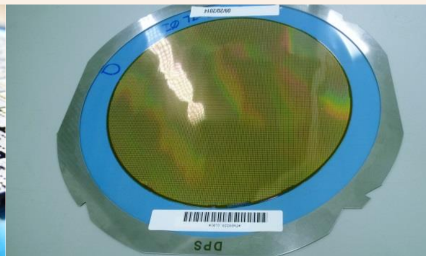
1. CAPACITY INCREASE

MORE PARALLELISM. The bigger the number of sensors under test simultaneously, the bigger is the capacity. Simple?

– Double parallelism = Double capacity. May not be true.
– Handling of single components, lot of pick&place
– Strip testing, benefits and cons
– **Yes,** in **Wafer level testing** (not only for wafers)





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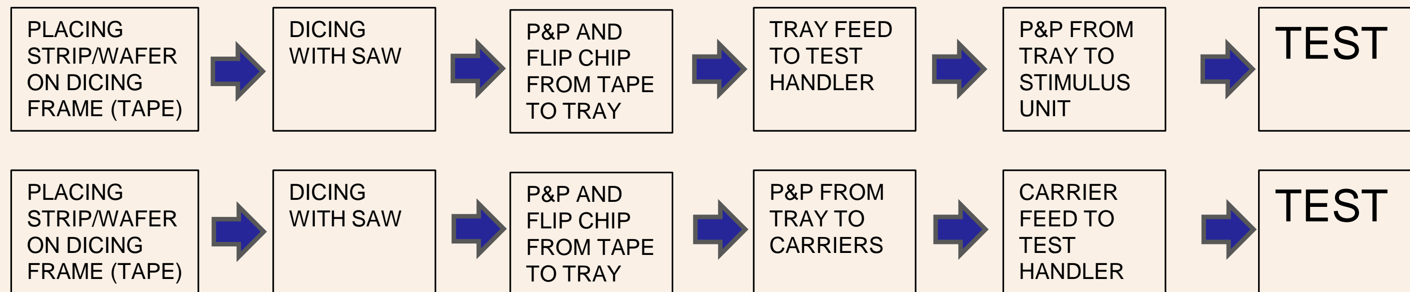
2. SHORTEN THE PROCESS

Typical current process:



Process with wafer level test handler:

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2. SHORTEN THE PROCESS

If the savings from other machinery are bigger than the investment cost of **Wafer Level Test Handler**, can we talk about **NEGATIVE COT**?

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2. SHORTEN THE PROCESS

Process with wafer level test system has major economic and process versatility gains:

1. Loading of thousands of sensors to the test handler at time
2. Short test to test time -> only step of the prober
3. Short product change time -> only the change of probe card
4. Small size of the sensors is not an issue.
5. No P&P processes -> better yield
6. Easy re-test possibility
7. With WLP/CSP, is the final testing the only testing?

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3. OPTIMIZE FOR MEMS

- MEMS sensors are nowadays typically digital. The testing normally means only communication via SPI/I2C and measurement of current consumption.
- The industry still uses Testers which are meant for more complex testing like testing of SOC ICs or processors.
  - Overkills?
  - Share of total investment may be unnecessary big
  - Big size (takes expensive floor space)
  - "Deep integration" to the handler is not possible -> long measuring cables which may wear out quickly and don't give the best measuring conditions.

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3. OPTIMIZE FOR MEMS

- Optimal tester for MEMS:
  - Can be easily optimized for the test requirements
  - Economical
  - Light weight and compact size enables "Deep integration" to the handler
    - Short, static cables. Better signal quality.
    - Tolerates the mechanical stresses due to handler movements
    - Better stimulus, no turning range limitations

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3. OPTIMIZE FOR MEMS

EXAMPLES OF ”DEEP INTEGRATION”

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CONCLUSIONS

- WAFER LEVEL TEST HANDLER:
  - Capable also for final testing
  - Capable also for testing conventional package types
  - Meets the challenges of sensor miniaturization
  - Yields high capacity
  - Shortens the process
  - Combined with optimal tester forms an economical solution
  - Gains the lowest COT

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CONCLUSIONS

COST OF TEST < 1 cent
Case: 3-axis accelerometer

Price (total solution)	**1 000 000**	USD	Full test cell (handler + tester + probe card)
Labour cost	**20 000**	USD	Annual operator cost (24/7)
Cost of use	**20 000**	USD	Consumables, energy
Operation cost/hour	**5**	USD/h	8000 h/year
Test Capacity	**140 000**	UPH	With Zero Test Time
Test Capacity	**13 000**	UPH	Real test capacity*
Cost of test	**0.04**	Cents	No CAPEX included
	0.25	Cents	CAPEX (5 years depriciation)
	0.15	Cents	CAPEX (10 years depriciation)

* UPH achieved with 5 turn testing/calibration and 32 accelerometers parallel

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