SIXTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop™

March 15 - 18, 2015

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Tutorial

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How to Make a High Frequency Transparent Socket

Heidi Barnes
Keysight Technologies

2015 BiTS Workshop
March 15 - 18, 2015

Workshop Agenda

➡ Noon to 1:30 pm ○ Channel Simulations with Sockets

- Signal Integrity Basics

1:30 to 2:45 pm ○ SI Challenges with BGA Sockets

- Differential Signaling and Mode Conversion
- NEXT and FEXT coupling

2:45 to 3:15 pm Break

3:15 to 4:30 pm ○ Measurements

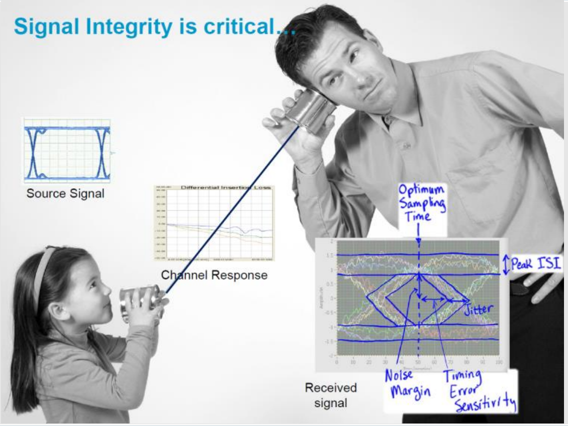
- Fixture characterization and de-embedding

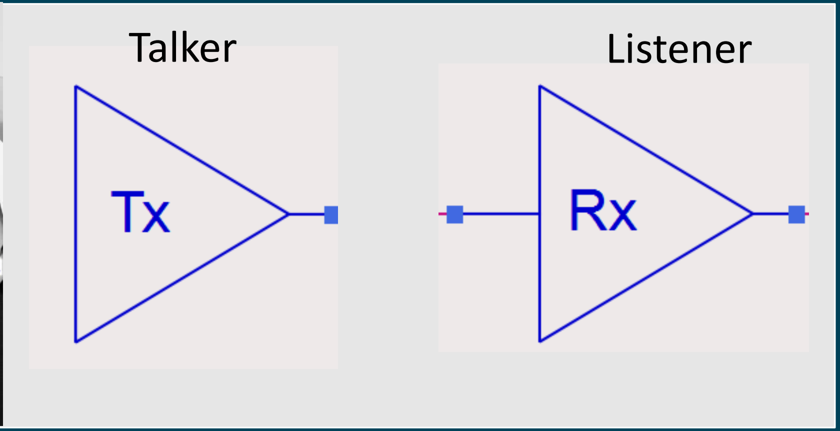
4:30 to 6:00 pm ○ Deconstructed Models

- Calibrated simulations
- The Transparent Socket

Each section includes a ~20 minute Hands-On Lab

Signal Integrity

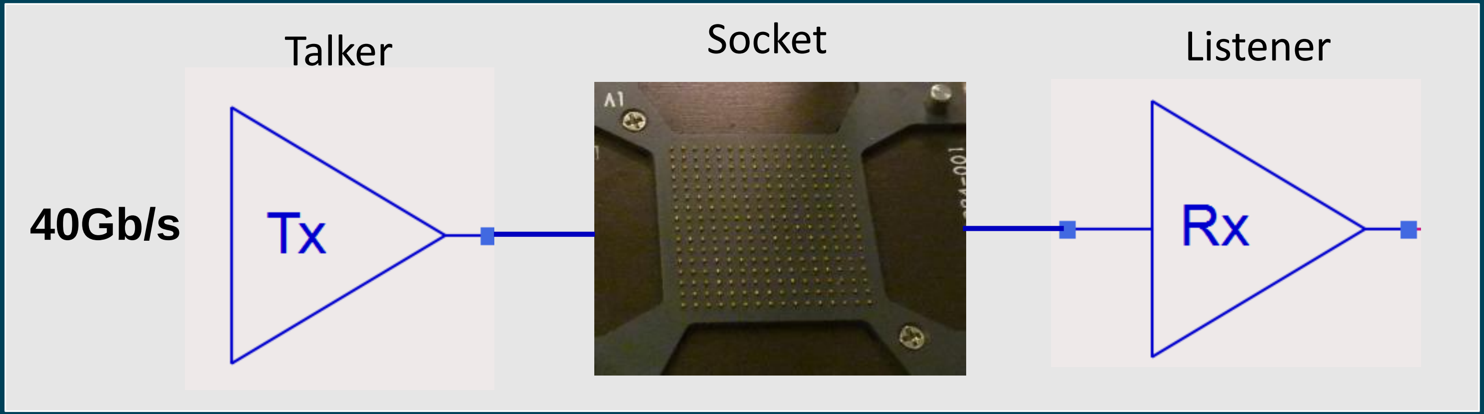




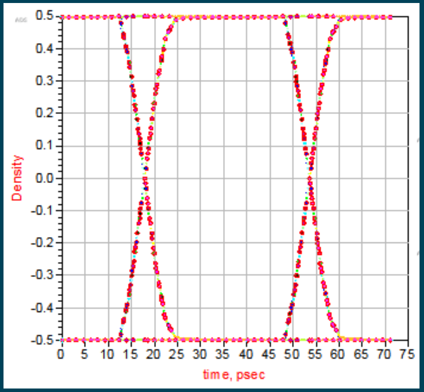
The Tx to Rx connection:

- Digital standards refer to it as the Physical Layer or “the PHY” for short.
- Simulation tools call it the channel

Why Do I Need Signal Integrity?

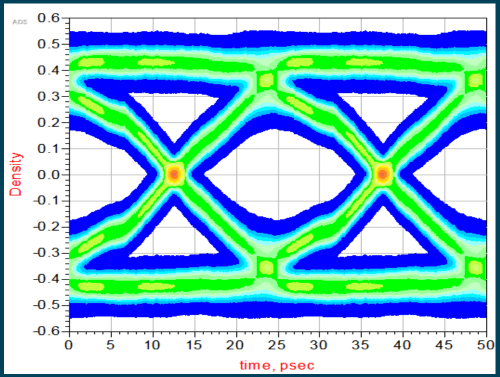


What I Simulate



A Transparent Socket

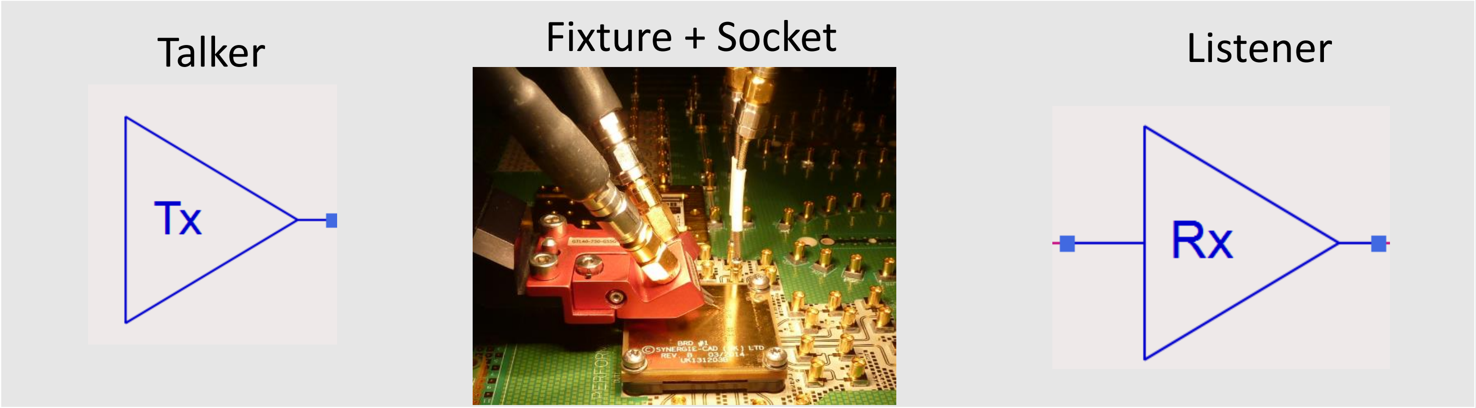
What I Measure



Socket + Fixture

1) I should find a new job.
2) What is the fixture?
3) As-fabricated materials?
4) How can I tell what is wrong?
5) What should I fix first?

The Full-Path Measurement

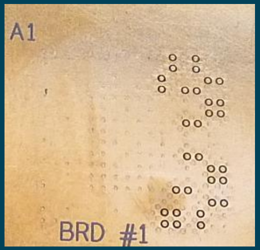

Talker

Fixture + Socket

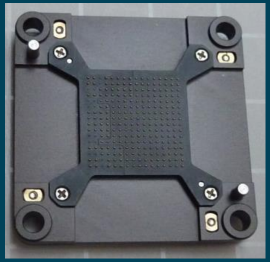
Listener

Probe GSG-GSG

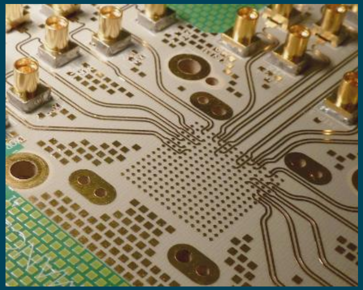
Probe to Socket Interposer



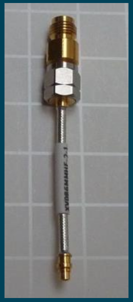
Socket DUT



PCB Footprint to Microstrip



PCB MMPX to 1.85mm Coax



Why can’t I just measure the socket directly?

Eric Bogatin's Rule #9

Rule # 9: Never do a measurement or simulation without first anticipating what you expect to see.

- Simulations and measurements minimize risk
- Knowing what to expect saves time and money
- If you get it right you feel good
- If you get it wrong you will learn something

Signal and Power Integrity expert Eric Bogatin is the author of:
Signal Integrity and Power Integrity Simplified,
Prentice Hall, 2nd edition 2010

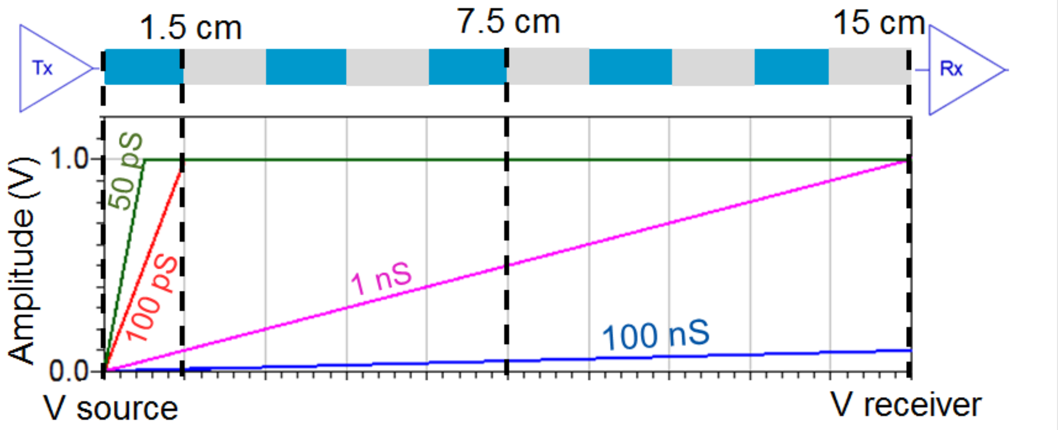
Signal Integrity Basics

- Material Loss :
  - Dielectric and Conductor
- Impedance Loss and S-Parameters
  - Reflections
  - Stub vs Series Resonator
  - Filter

Time Travel is not Allowed

What is high speed ?

V≠IR



Step Edge Voltage Along the Signal Path

Transient.avi

The Channel has finite length:

- Speed of Tx : *Signal Rise-time*
- Type of Data : *Data Rate Gb/s*
- Speed of Channel: *Time Delay*

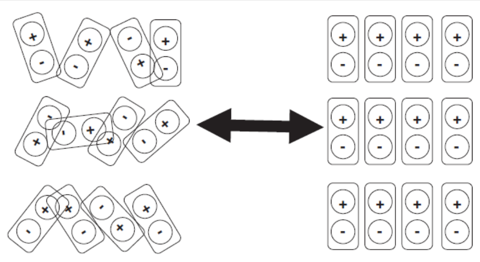
$$\text{Rise Time}_{20-80\%} = \frac{0.22}{Frequency_{3dB}}$$

$$\text{Unit Interval} = \frac{1}{DataRate_{NRZ}}(ps)$$

$$velocity = \frac{12}{\sqrt{Dk}}\left(\frac{mils}{ps}\right)$$

Channel Loss Materials

Dielectric Loss

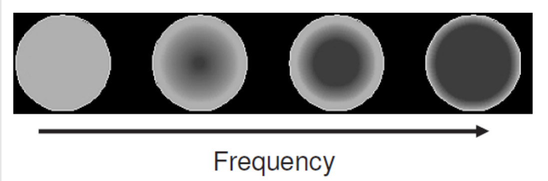


$$\text{Dielectric Loss} \approx 2.3\, f \sqrt{\varepsilon_r}\, \tan\delta \;\; \text{dB/inch}$$

$$\text{example: } 2.3\,(1\text{GHz})\sqrt{4}\,(0.02) \approx 0.092\ \text{dB/inch}$$

Conductor Loss

Current Density



$$1\text{oz Copper Loss} \approx \frac{36}{w\,Z_0}\sqrt{f}\,\tan\delta \;\; \text{dB/inch}$$

$$example: \frac{36}{(10mils)(50\Omega)}\sqrt{1GHz} \approx 0.07\ \text{dB/in}$$

Chapter 9 in Eric Bogatin's *Signal Integrity and Power Integrity*, 2010

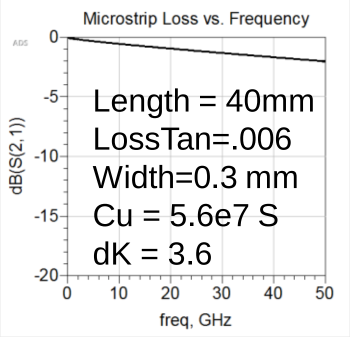
Losses from materials:

- Dielectric loss caused by dipole movement with rapidly changing fields. Proportional to frequency.

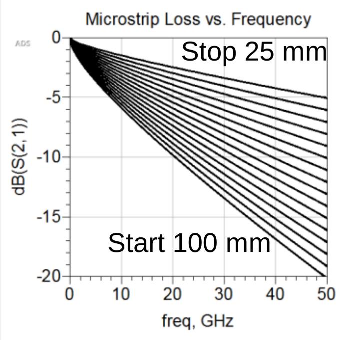
- Conductor loss with skin effect pushing currents to lowest inductance path. Proportional to square root of frequency.

Data - Channel Loss PCB Materials

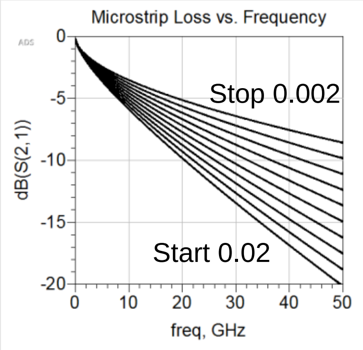
My Application



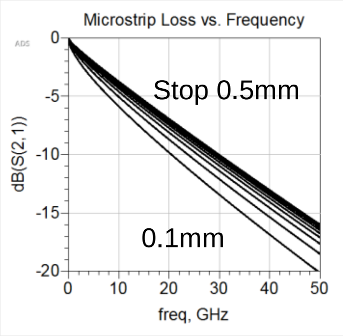
Worst Case vs Length 100mm to 25mm



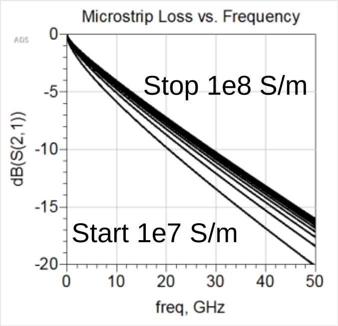
Worst Case vs Loss Tangent 0.02 to 0.002



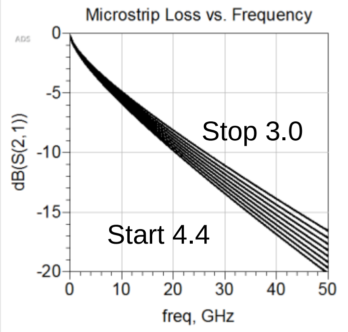
Worst Case vs Width 0.1mm to 0.5mm



Worst Case vs Conductivity 1e7 S/m to 1e8 S/m



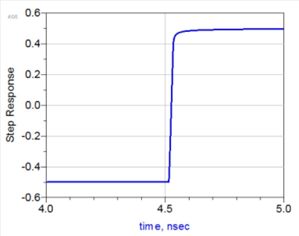
Worst Case vs dK 3.0 to 4.4



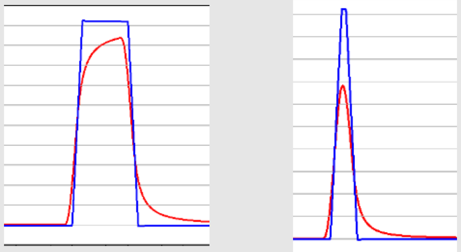
Worst Case: 100mm Length, 0.02 LossTan, 0.1mm Width, 1e7 S/M, 4.4 dK

PCB Material Loss in the Time Domain

Step Response

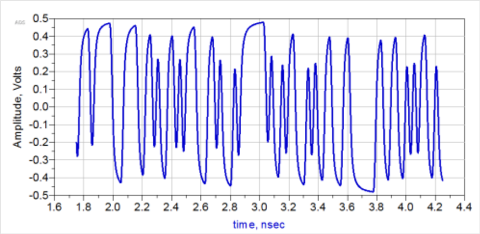


Single Bit Response (SBR)

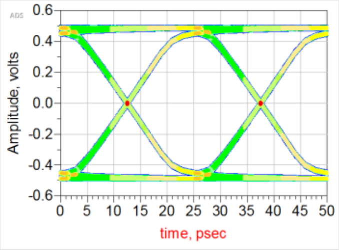

10 Gb/s

40 Gb/s

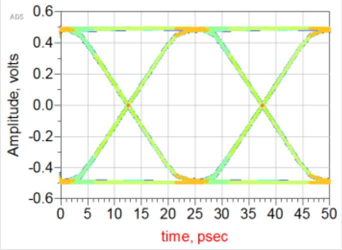
40 Gb/s PRBS9 Waveform Worst case PCB Materials



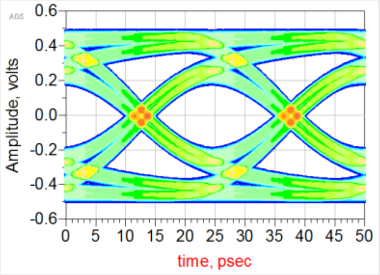
Eye Diagram Socket Application



Best Case PCB Material



Worst Case PCB Material



Effective Loss Tangent

Leveraging old PCB technology

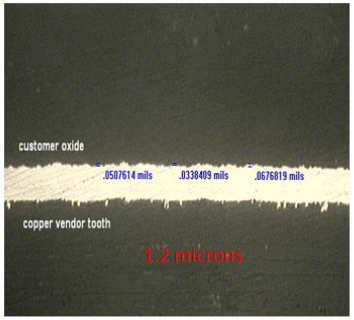
New SI requirements for the PCB fabrication document:

-Glass Weave
-Copper Profile
-Test Structures for as-fabricated PCB losses.

Pictures from Lee Ritchey of Speeding Edge, “13-TU2 Breaking the 32 Gb/s Barrier: PCB Materials, Simulations, Measurements”, DesignCon2015

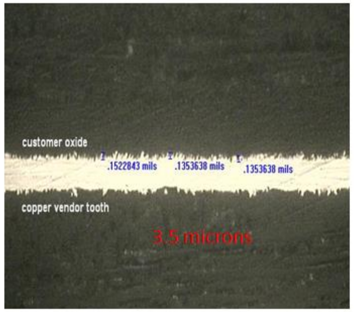
Copper Foil Profile – surface roughness

Supplier # 1 Oxide



Good Loss

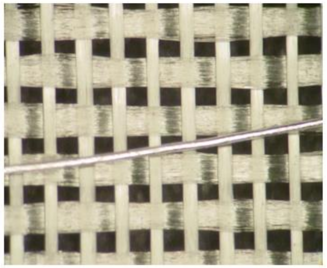
Supplier # 2 Oxide



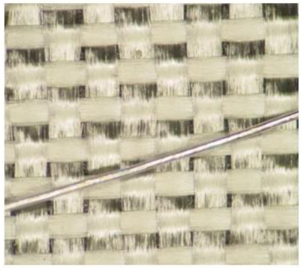
Poor Loss

Glass Weave – dK variation

Two Common Glass Weaves Styles



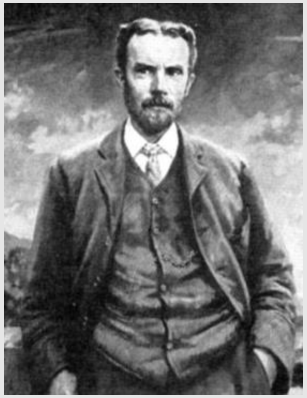
1080 GLASS WEAVE
(very open weave)



3313 GLASS WEAVE
(uniformly spread weave)

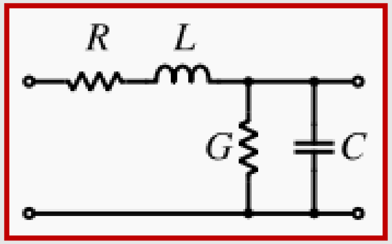
A 3.5 MIL WIRE IS SPREAD ACROSS THE WEAVE TO PROVIDE SCALE OF A TYPICAL TRACE

Telegrapher's Equations



Oliver Heaviside
1850-1925

Voltages and Currents are changing with Time and Distance (Magnitude and Phase)



- Create a simple model of a transmission line.
- Utilize calculus to analyze the model when summing a series of incremental length sections.

For small R and G

$$\frac{\partial^2}{\partial t^2}V = \frac{1}{LC}\frac{\partial^2}{\partial x^2}V$$

$$\frac{\partial^2}{\partial t^2}I = \frac{1}{LC}\frac{\partial^2}{\partial x^2}I$$

Sinusoidal Input

$$E = E_o . e^{-j\omega(\frac{x}{c}-t)}$$

$$\frac{\partial^2 V(x)}{\partial x^2} + \omega^2 LC \cdot V(x) = 0$$

$$\frac{\partial^2 I(x)}{\partial x^2} + \omega^2 LC \cdot I(x) = 0$$

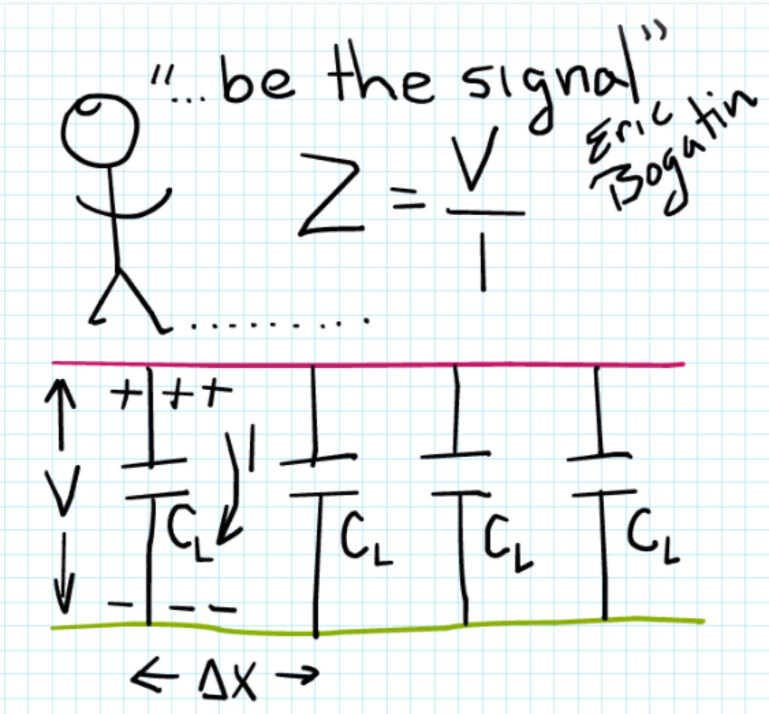
Resulting Relationships

$$v = \frac{1}{\sqrt{LC}}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$

Characteristic Impedance Z_0



Derivation from Telegrapher Equations:

$$Z_0 = \sqrt{\frac{L}{C}}$$

Derivation from transmission line charging:

Independent of Length

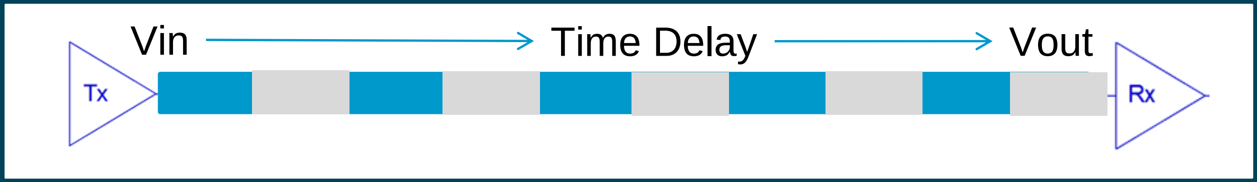
$$Z_0 = \frac{1}{vC_L}$$

$$C = C_L \Delta x \quad , \quad I = \frac{\Delta Q}{\Delta t} \quad , \quad \Delta Q = CV \quad \Delta t = \frac{\Delta x}{v}$$

$$then \;\; I = \frac{C_L \Delta x V}{\frac{\Delta x}{v}} = vC_L V \;\; \text{and} \;\; Z = \frac{V}{I} = \frac{1}{vC_L}$$

Impedance Reflections

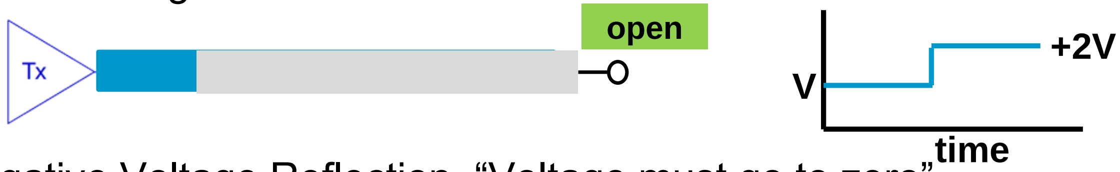
“Reflections are the reality when time traveling is not allowed”



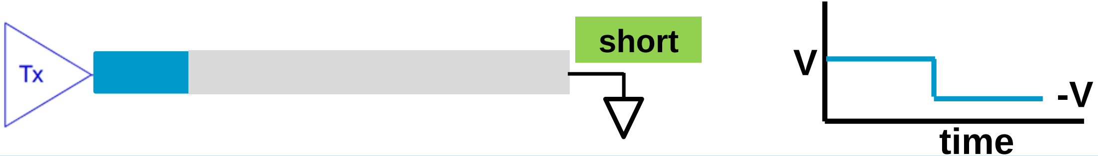
Vin does not show up instantaneously at Vout, and therefore Vin requires a round trip delay to adjust to the Vout termination. Initial Vin only sees the “characteristic impedance” Zo.

Thought Experiment for Impedance Reflections

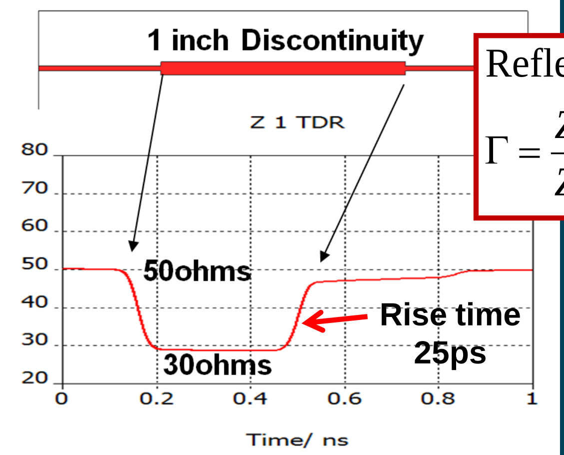
OPEN - Positive Voltage Reflection “Current must flow back to the source”



SHORT - Negative Voltage Reflection “Voltage must go to zero”

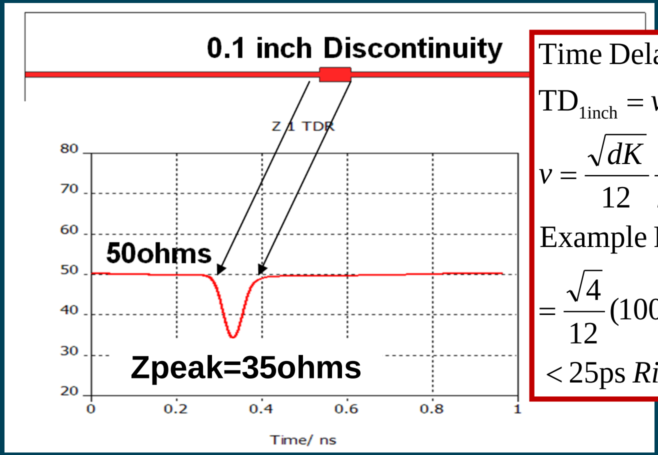


Magnitude of the Reflection



Reflection :

$$\Gamma = \frac{Z_{\Delta x} - Z_0}{Z_{\Delta x} + Z_0}$$



Time Delay :

$$TD_{1inch} = vL$$

$$v = \frac{\sqrt{dK}}{12}\frac{ns}{mil}$$

Example FR4 :

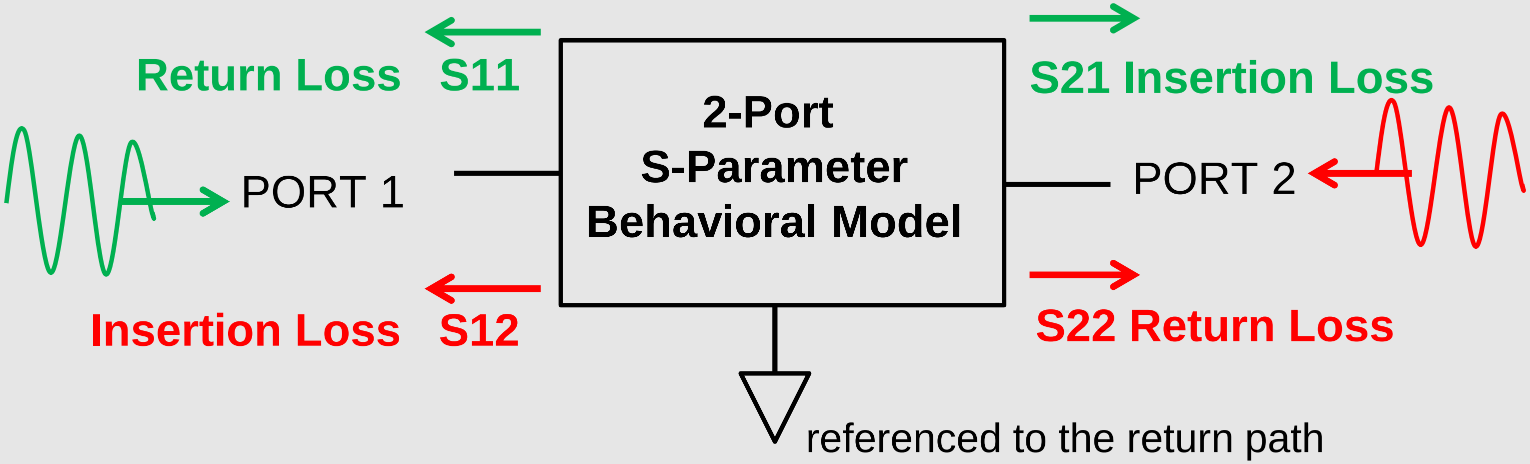
$$= \frac{\sqrt{4}}{12}(100) \approx 17\,ps$$

$$< 25ps\ Rise\ time$$

Bit Rate	~1/10th Rise Time Feature Size	High Speed Feature Size
1 MBit	3 m (10 ft)	Matched Termination
10 MBit	30 cm (12 in)	T-Line Zo
100 MBit	3 cm (1.2 in)	Connector Zo
1 GBit	3 mm (120 mils)	Passive SMT Zo
5 GBit	0.6 mm (24 mils)	Via Zo
10 GBit	0.3 mm (12 mils)	Die, Package, PCB Co-sim
40 GBit	0.075 mm (6 mils)	Machining Tolerances

Circuit Model with Reflections

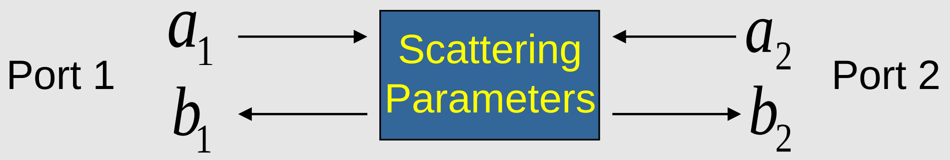
S-Parameter Behavioral Model



S-Parameters (S11, S21, S12, S22) .s2p Touchstone file

Measuring S-Parameters is Easy

2-Port Network Scattering Parameters



Relation of Incident and Reflected Voltage Waves

$$b_1 = S_{11}a_1 + S_{12}a_2$$

$$b_2 = S_{21}a_1 + S_{22}a_2$$

Matrix Form

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}$$

Termination in Zo Results in 0 Reflections at that Port and one of the terms goes to zero:

Port 2 Terminated in Zo

a_2=0

$$S_{11} = \frac{b_1}{a_1} = \frac{V_1^-}{V_1^+} \text{ and } S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+}$$

Port 1 Terminated in Zo

a_1=0

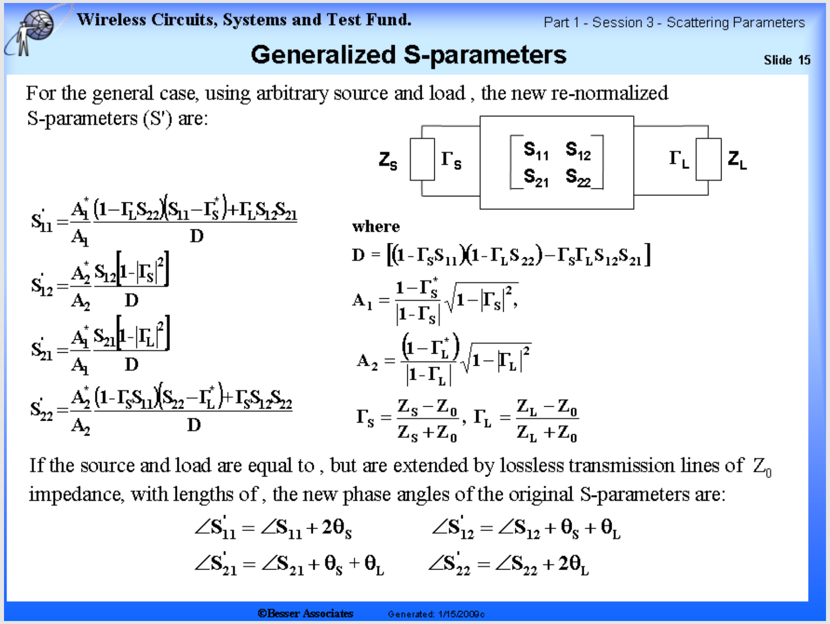
$$S_{12} = \frac{b_1}{a_2} = \frac{V_1^-}{V_2^+} \text{ and } S_{22} = \frac{b_2}{a_2} = \frac{V_2^-}{V_2^+}$$

Need to know Z_0 of the S-Parameter

- S-Parameters can be renormalized for any Source and Load Impedance using the Zo used for measurement.

S-Parameters can be converted to the Z or Y matrices which are independent of Source and Load Impedances.

Passive Circuits and Systems
By Rowan Gilmore, Les Besser
Published by Artech House, 2003
ISBN 1580535216, 9781580535212



Wireless Circuits, Systems and Test Fund. Part 1 - Session 3 - Scattering Parameters

Generalized S-parameters

Slide 15

For the general case, using arbitrary source and load , the new re-normalized S-parameters (S') are:

$$S'_{11} = \frac{A_1^*}{A_1}\frac{(1-\Gamma_L S_{22})(S_{11}-\Gamma_S^*)+\Gamma_L S_{12} S_{21}}{D}$$

$$S'_{12} = \frac{A_2^*}{A_2}\frac{S_{12}\left[1-|\Gamma_S|^2\right]}{D}$$

$$S'_{21} = \frac{A_1^*}{A_1}\frac{S_{21}\left[1-|\Gamma_L|^2\right]}{D}$$

$$S'_{22} = \frac{A_2^*}{A_2}\frac{(1-\Gamma_S S_{11})(S_{22}-\Gamma_L^*)+\Gamma_S S_{12} S_{22}}{D}$$

where

$$D = \left[(1-\Gamma_S S_{11})(1-\Gamma_L S_{22})-\Gamma_S \Gamma_L S_{12} S_{21}\right]$$

$$A_1 = \frac{1-\Gamma_S^*}{|1-\Gamma_S|}\sqrt{1-|\Gamma_S|^2},$$

$$A_2 = \frac{(1-\Gamma_L^*)}{|1-\Gamma_L|}\sqrt{1-|\Gamma_L|^2}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \quad \Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}$$

If the source and load are equal to , but are extended by lossless transmission lines of Z_0 impedance, with lengths of , the new phase angles of the original S-parameters are:

$$\angle S'_{11} = \angle S_{11} + 2\theta_S \qquad \angle S'_{12} = \angle S_{12} + \theta_S + \theta_L$$

$$\angle S'_{21} = \angle S_{21} + \theta_S + \theta_L \qquad \angle S'_{22} = \angle S_{22} + 2\theta_L$$

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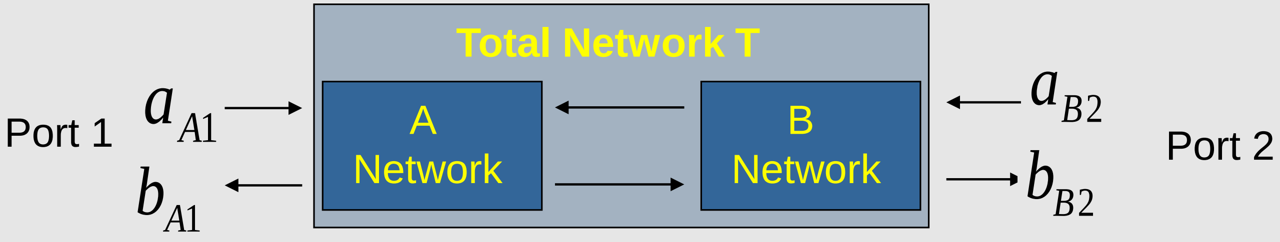
Cascading S-Parameters

Cascading Two 2-Port Networks



Multiplying S-Parameter Matrices Doesn't Work

$$S_T \neq S_A S_B$$

Convert to Normalized Incident and Reflected Wave T-Matrix

$$T_T = T_A T_B$$

From S to T

$$T_{11} = \frac{-\det(S)}{S_{21}} \qquad T_{21} = \frac{-S_{22}}{S_{21}}$$

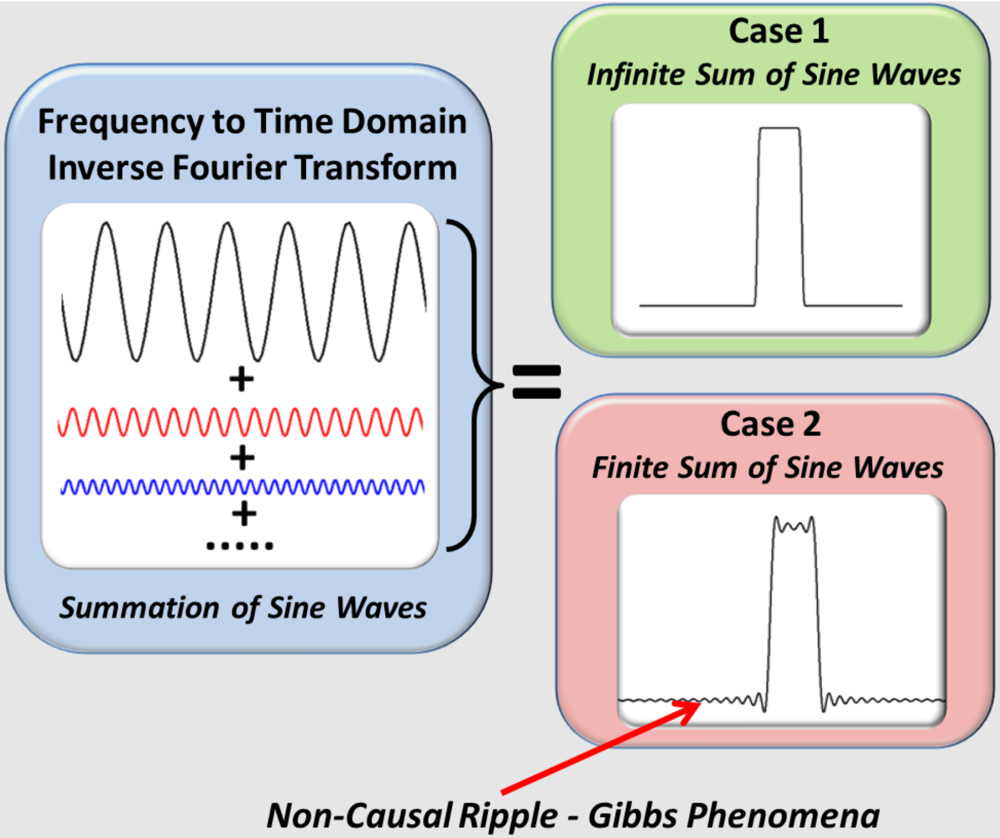
$$T_{12} = \frac{S_{11}}{S_{21}} \qquad T_{22} = \frac{1}{S_{21}}$$

From T to S

$$S_{11} = \frac{T_{12}}{T_{22}} \qquad S_{21} = \frac{1}{T_{22}}$$

$$S_{12} = \frac{\det(T)}{T_{22}} \qquad S_{22} = \frac{-T_{21}}{T_{22}}$$

Conversion to the Time Domain Inverse Fourier Transform



Frequency to Time Domain Inverse Fourier Transform

Summation of Sine Waves

Case 1

Infinite Sum of Sine Waves

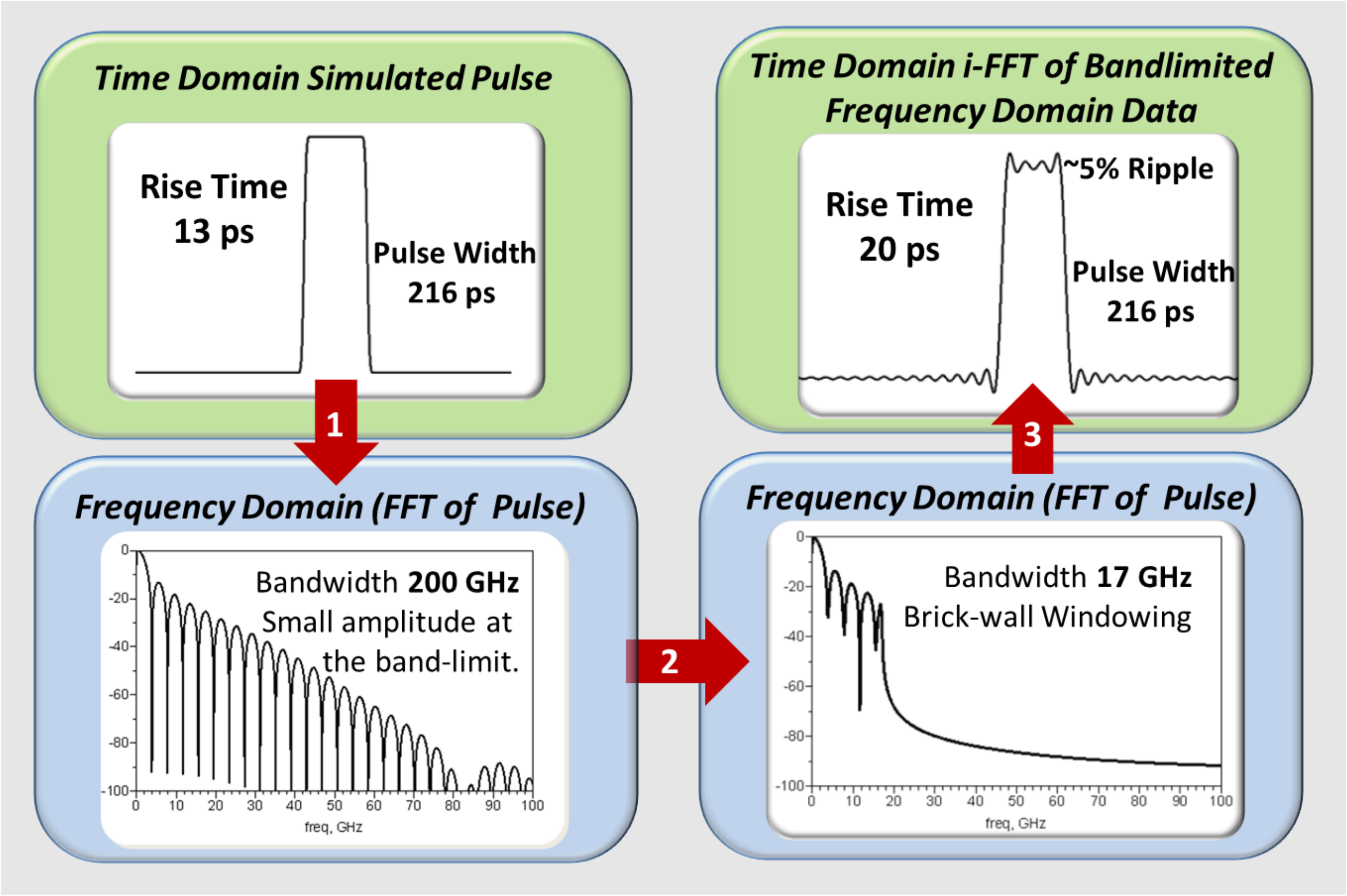
Case 2

Finite Sum of Sine Waves

Non-Causal Ripple - Gibbs Phenomena

28 Gb/s Tx	Bandwidth Rule-of-Thumb
Rise Time 13 ps 3 dB B.W.	17 GHz
Rise Time 5 ps 3 dB B.W.	44 GHz
3rd Harmonic	42 GHz
5th Harmonic	70 GHz

Band-Limited S-Parameters



Time Domain Simulated Pulse

Rise Time 13 ps

Pulse Width 216 ps

Frequency Domain (FFT of Pulse)

Bandwidth **200 GHz**
Small amplitude at the band-limit.

Frequency Domain (FFT of Pulse)

Bandwidth **17 GHz**
Brick-wall Windowing

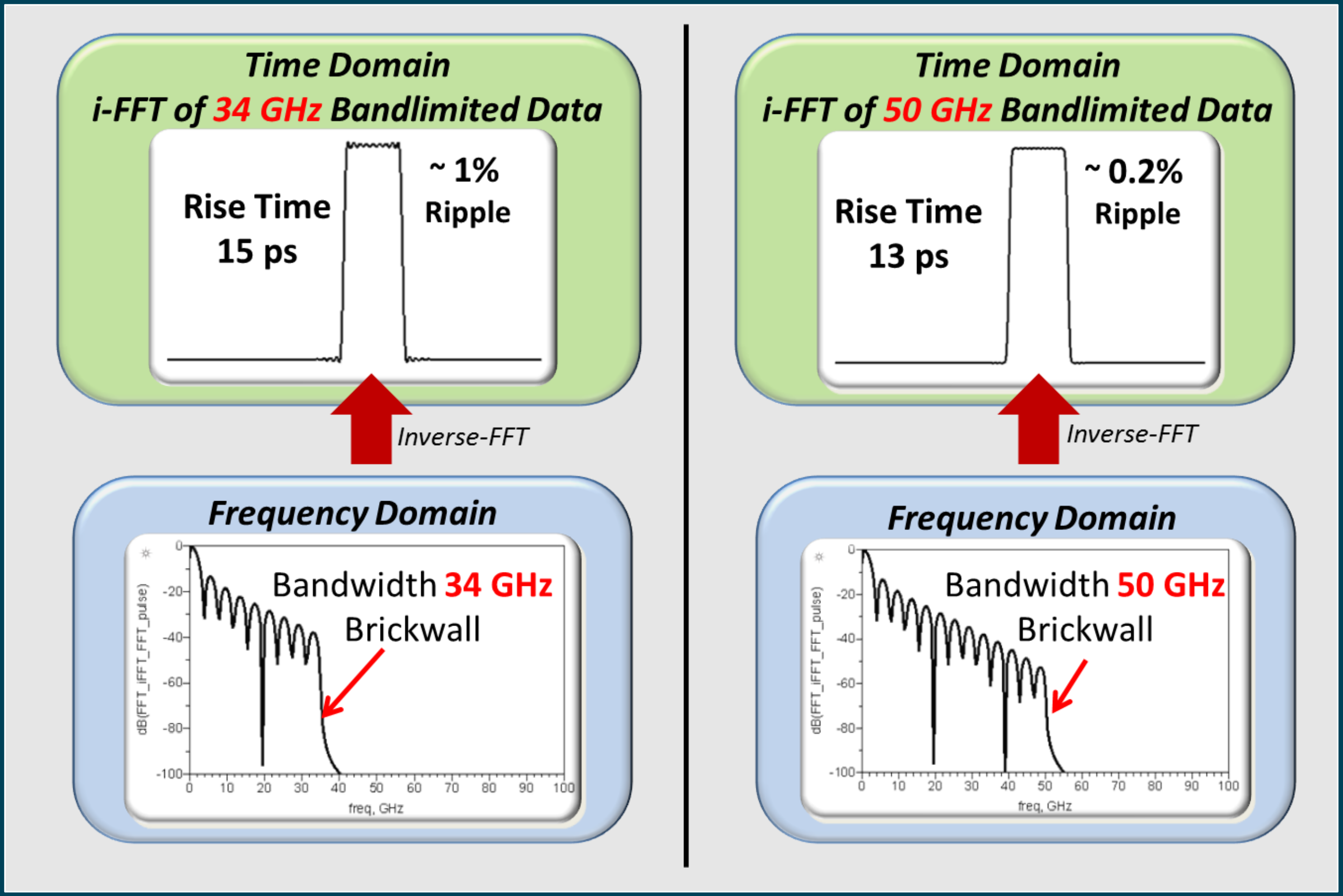
Time Domain i-FFT of Bandlimited Frequency Domain Data

~5% Ripple

Rise Time 20 ps

Pulse Width 216 ps

Channel Bandwidth



Time Domain
i-FFT of 34 GHz Bandlimited Data

Rise Time 15 ps

~ 1% Ripple

Inverse-FFT

Frequency Domain

Bandwidth **34 GHz** Brickwall

Time Domain
i-FFT of 50 GHz Bandlimited Data

Rise Time 13 ps

~ 0.2% Ripple

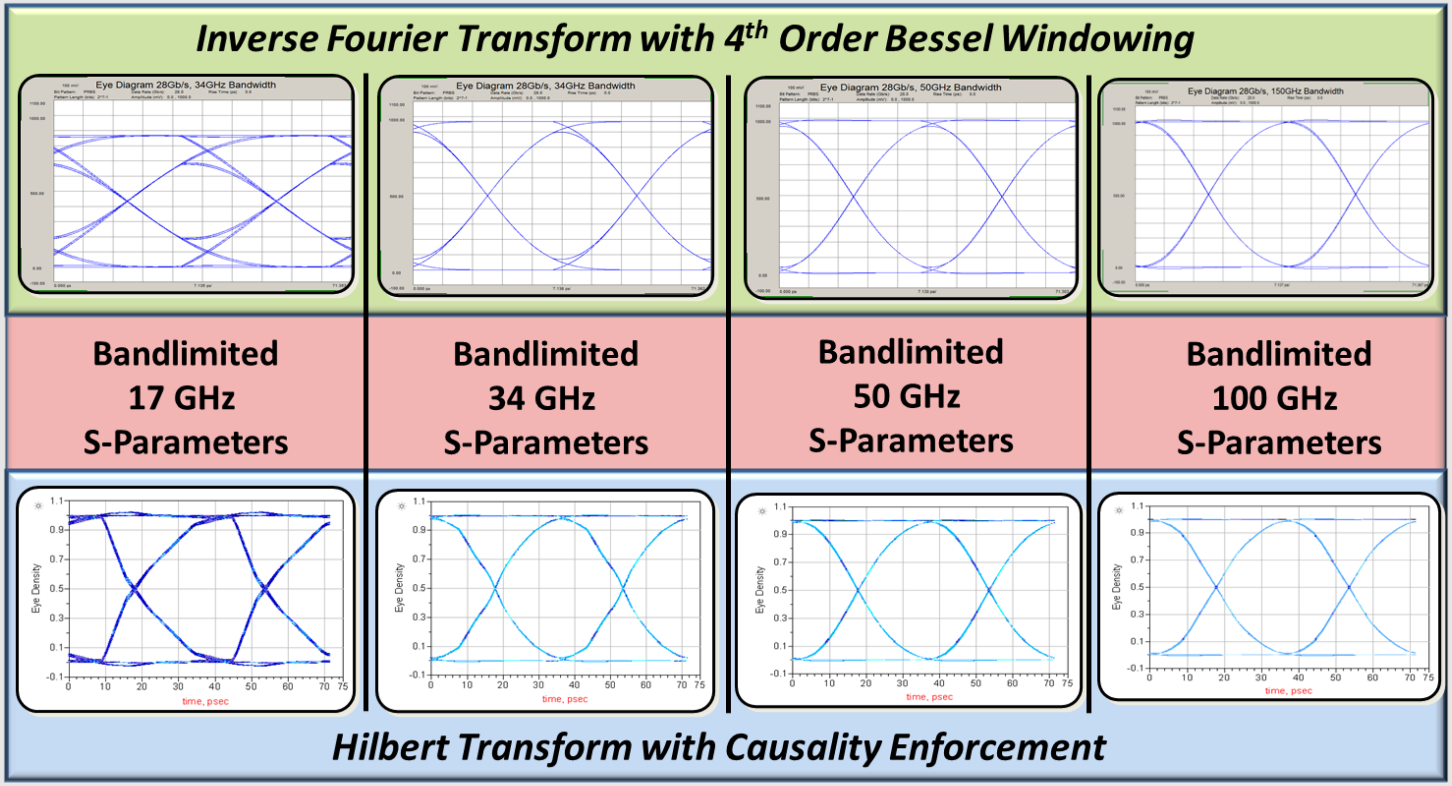
Inverse-FFT

Frequency Domain

Bandwidth **50 GHz** Brickwall

Fourier vs Causal Hilbert Transform

28Gbps , PRBS9 Signal

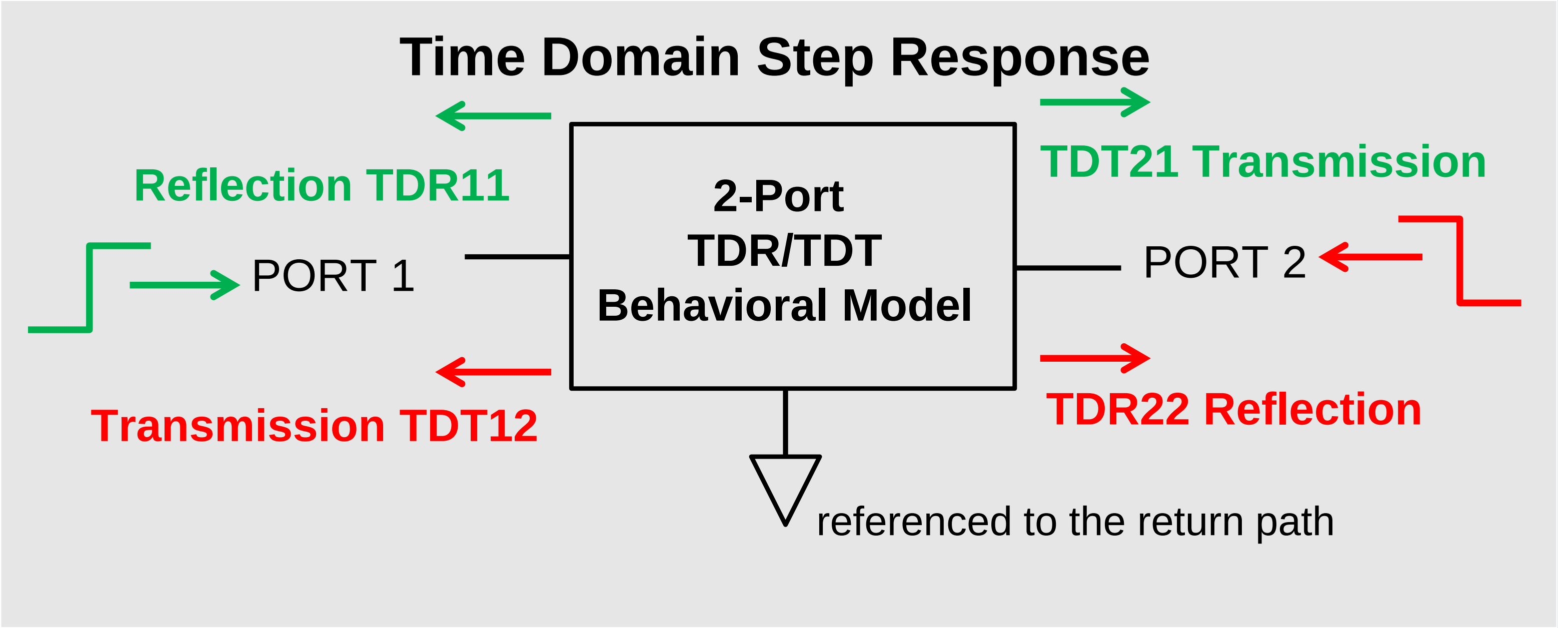


Inverse Fourier Transform with 4th Order Bessel Windowing

Bandlimited 17 GHz S-Parameters	Bandlimited 34 GHz S-Parameters	Bandlimited 50 GHz S-Parameters	Bandlimited 100 GHz S-Parameters

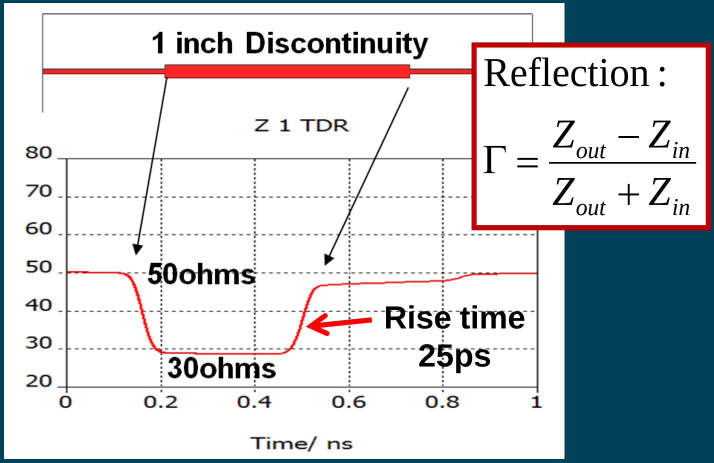
Hilbert Transform with Causality Enforcement

Time Domain Behavioral Model
TDR and TDT



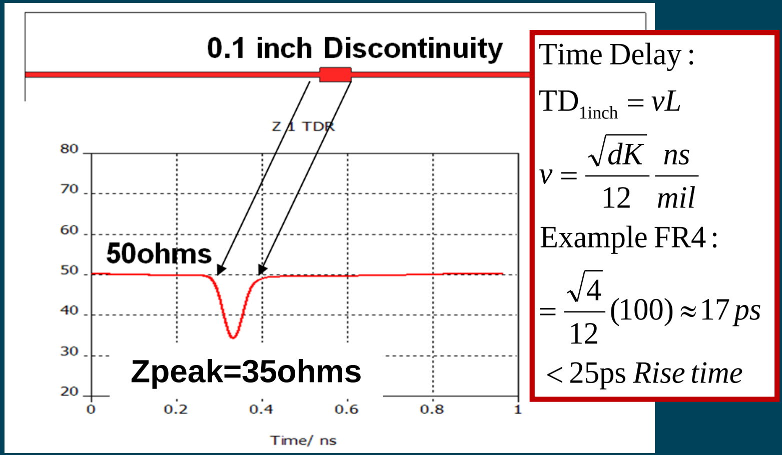
TDR – Time Domain Reflectometry
TDT – Time Domain Transmissivity

Back to the Impedance Reflection



Reflection :

$$\Gamma = \frac{Z_{out} - Z_{in}}{Z_{out} + Z_{in}}$$



Time Delay :

$$TD_{1inch} = vL$$

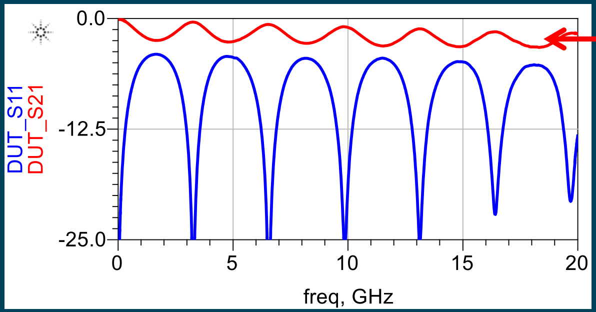
$$v = \frac{\sqrt{dK}}{12}\frac{ns}{mil}$$

Example FR4 :

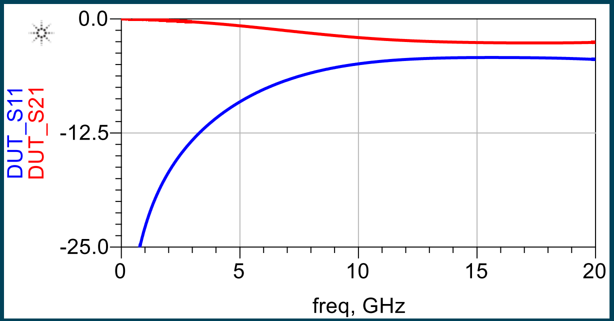
$$= \frac{\sqrt{4}}{12}(100) \approx 17\,ps$$

< 25ps *Rise time*

Check out the Frequency Domain

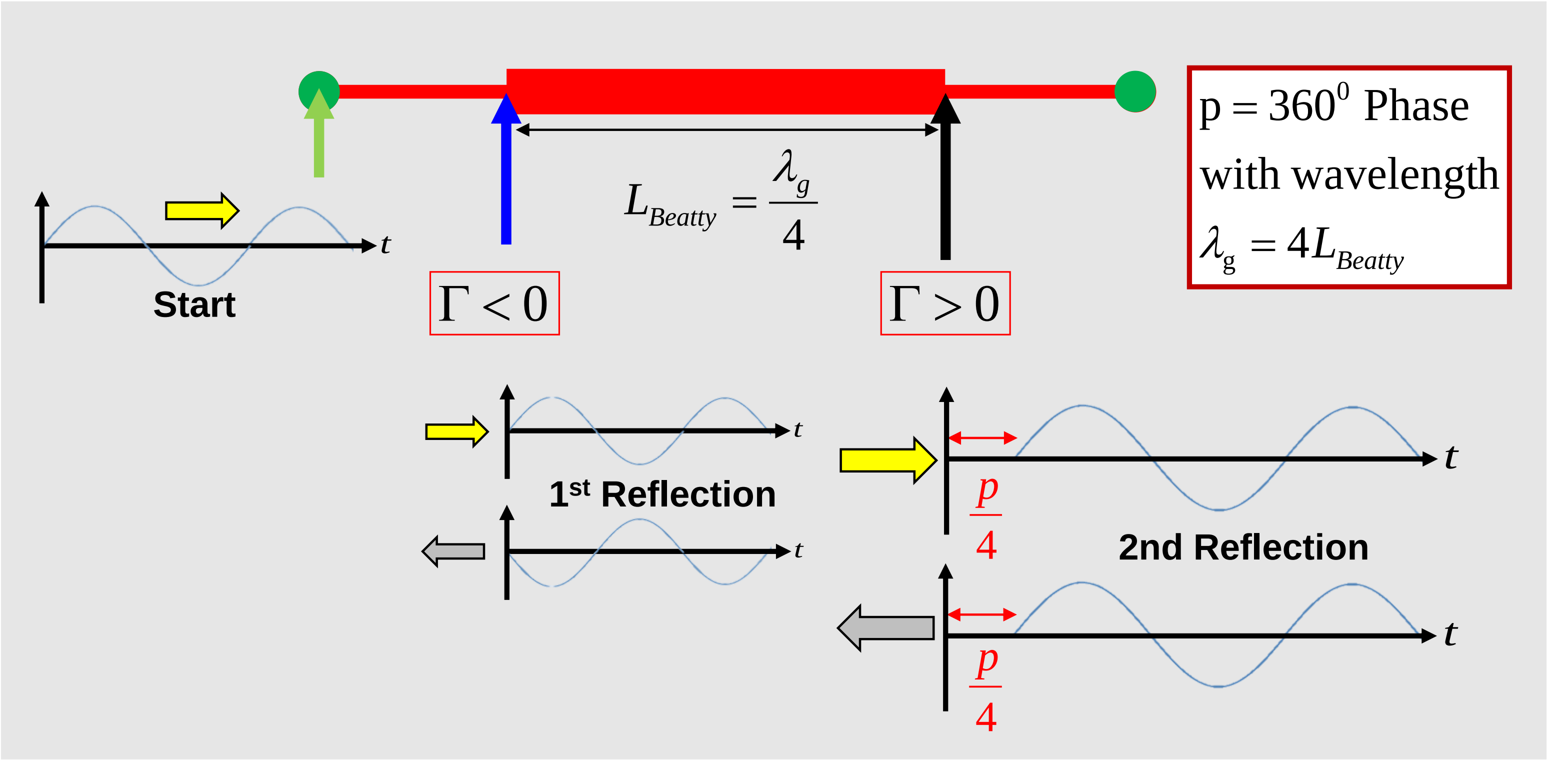


What is this ripple for S21?



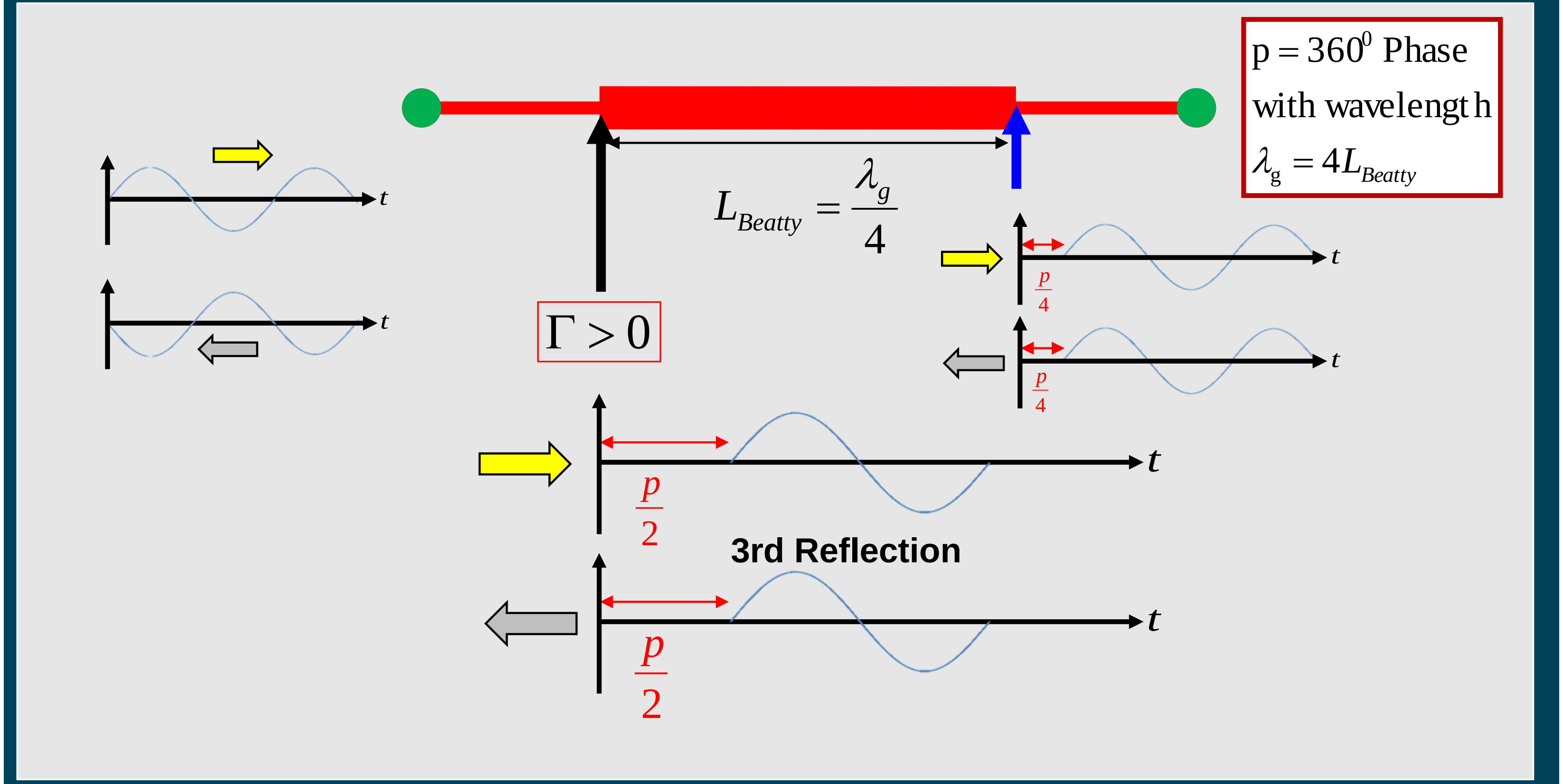
Multiple Reflections

Series Beatty Resonator (L=λ/4)



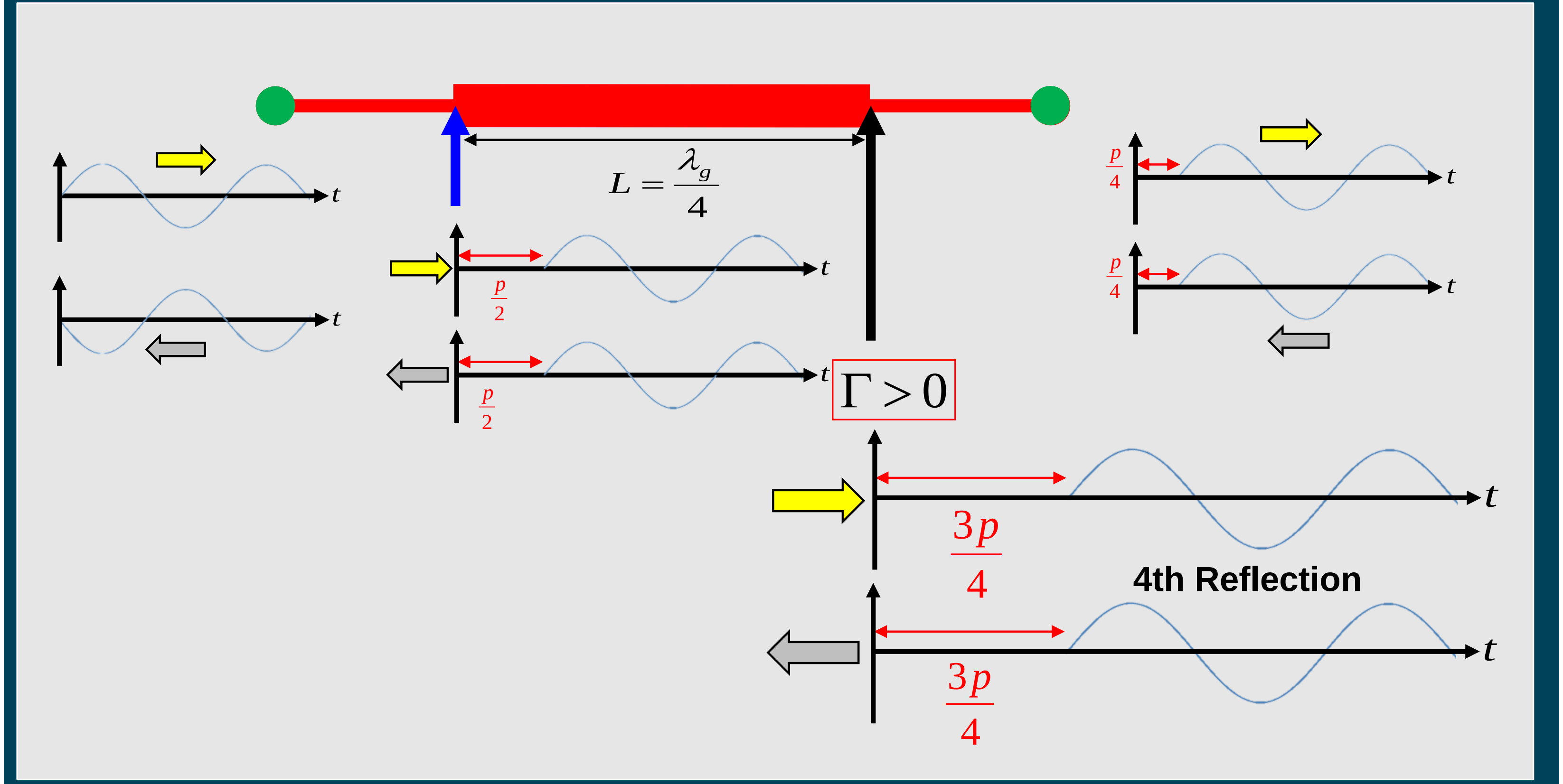
$p = 360^0$ Phase
with wavelength
$\lambda_g = 4L_{Beatty}$

Series Beatty Resonator

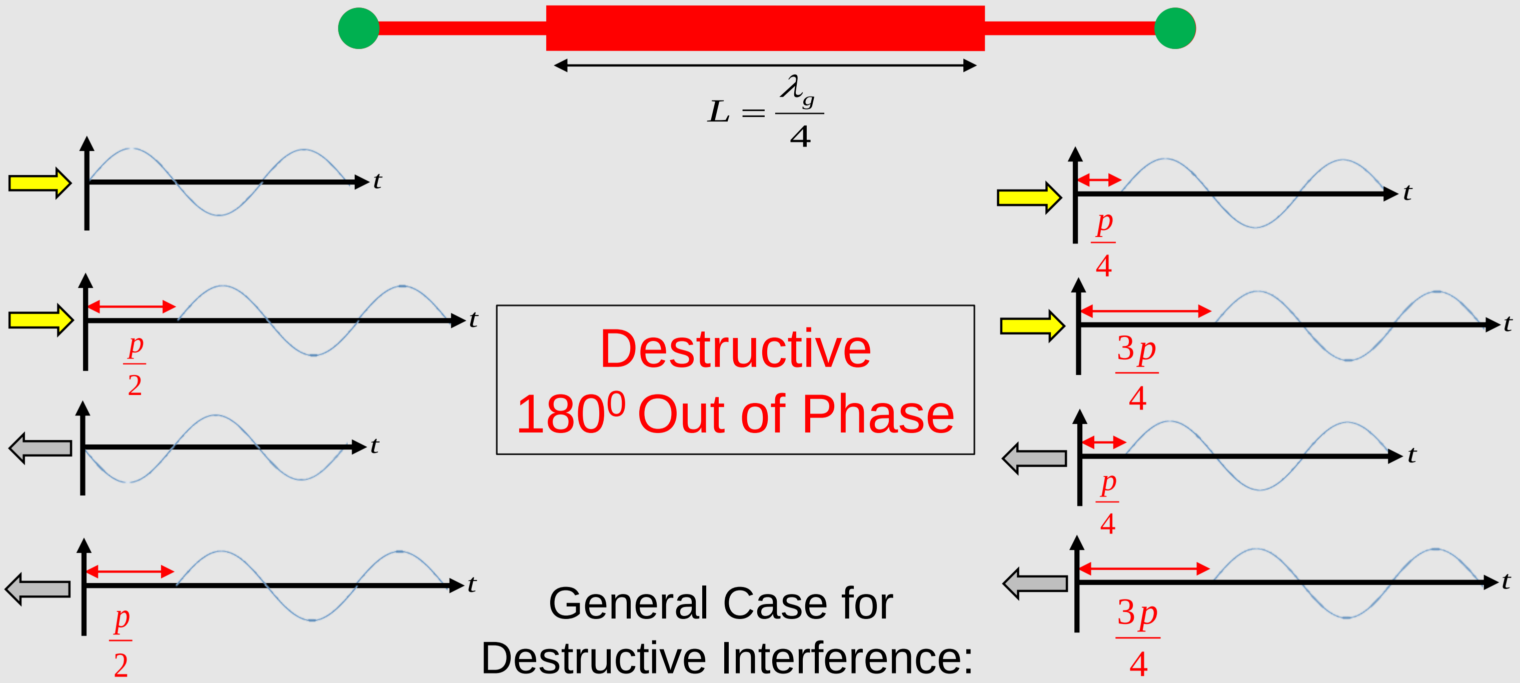


$p = 360^0$ Phase with wavelength $\lambda_g = 4L_{Beatty}$

Series Beatty Resonator



Destructive Multiple Reflections



$$L = \frac{\lambda_g}{4}$$

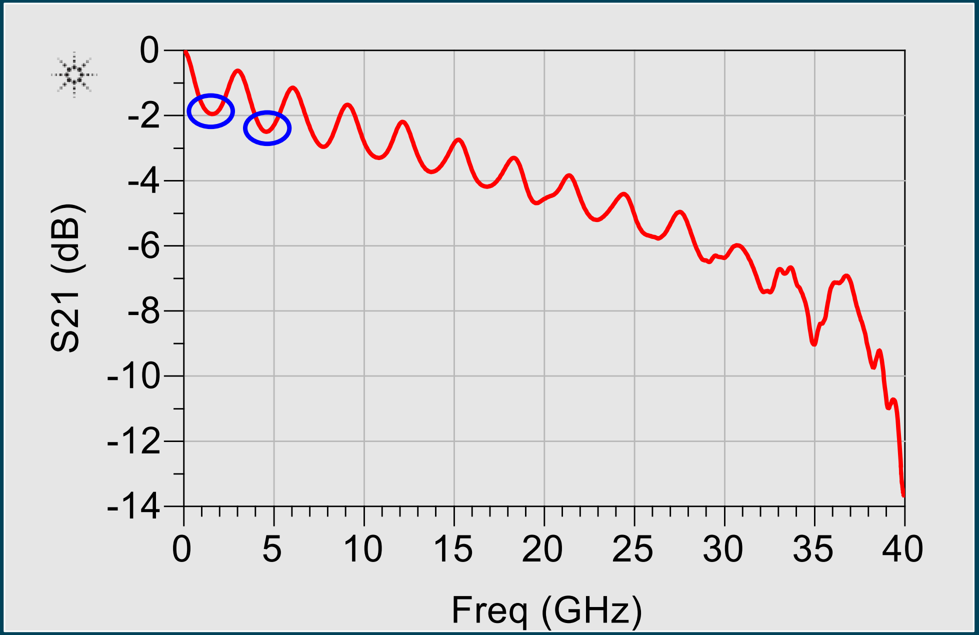
Destructive
180^0 Out of Phase

General Case for
Destructive Interference:

$$L_{resonance} = \frac{n\lambda}{4} \quad \text{for odd n} = 1,3,5.....$$

Destructive Interference

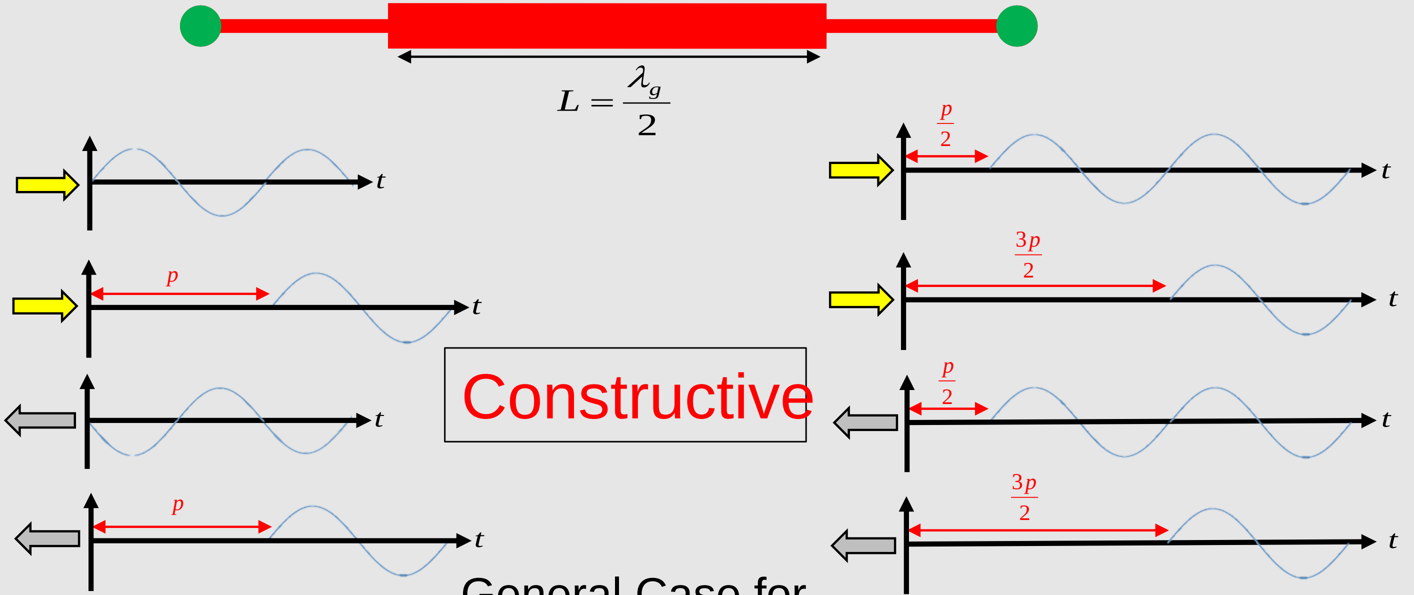
Series
Impedance
Discontinuity



Quarter-wavelength line (L=nλ/4 for odd n=1,3,5…)

1. Destructive interference
2. Cancellation of waves
3. Minimum transmission (S21)

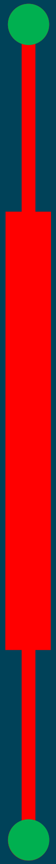
Constructive Multiple Reflections



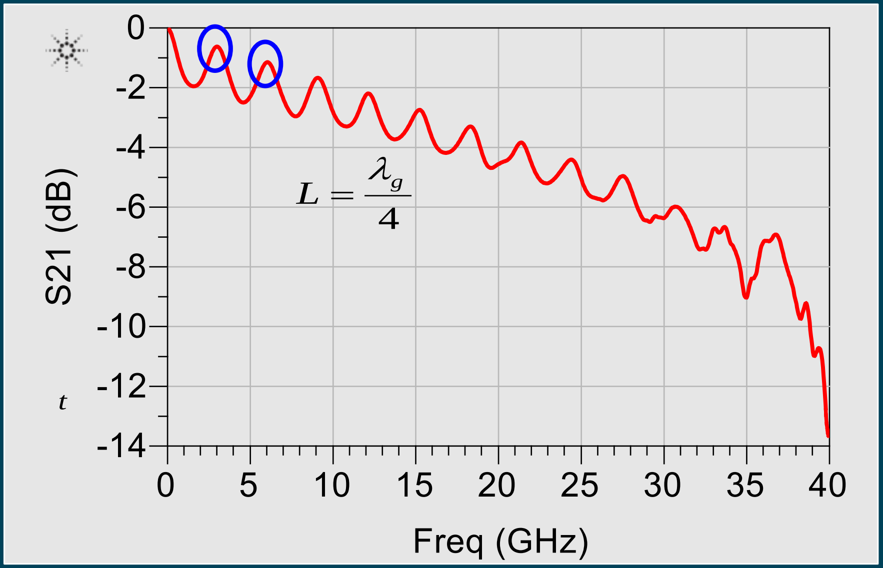
General Case for
Destructive Interference:

$$L_{resonance} = \frac{n\lambda}{2} \quad \text{for } n = 1,2,3.....$$

Constructive Multiple Reflections



Series
Impedance
Discontinuity

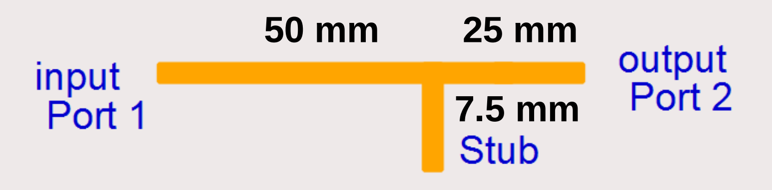


Half-wavelength line (L=nλ/2 for n=1,2,3…)

1. Constructive interference
2. Addition of waves
3. Maximum transmission (S21)

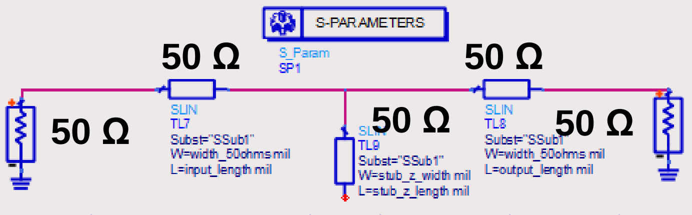
What about a Stub Discontinuity

Stub Resonance

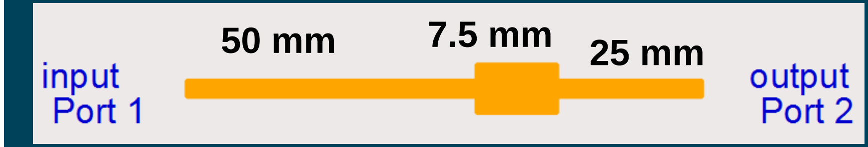


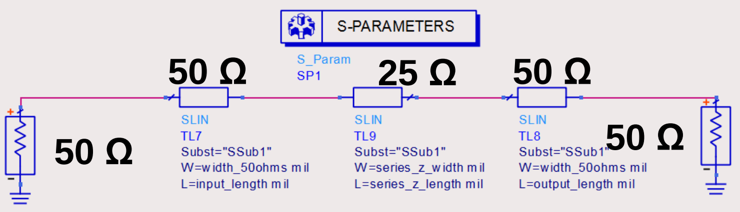
T-Line Model for Simulation

Fast Frequency Domain Sweep



Series Resonance





Reflection:

$$\Gamma = \frac{Z_{\Delta x} - Z_0}{Z_{\Delta x} + Z_0}$$

Simple simulations benefit analysis of TDR/TDT measurements.

Partial Reflection :

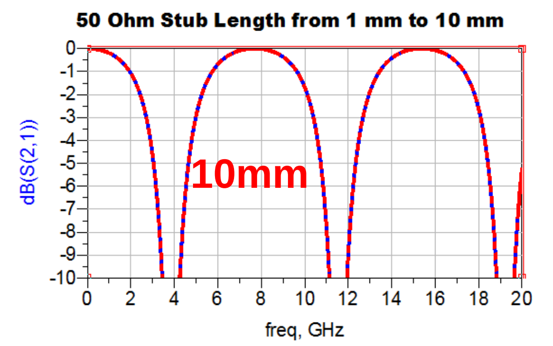
$$\Gamma_{series} = \frac{25-50}{25+50} = -\frac{1}{3}$$

Reflection :

$$\Gamma_{stub} = \frac{\infty - 50}{\infty + 50} = 1$$

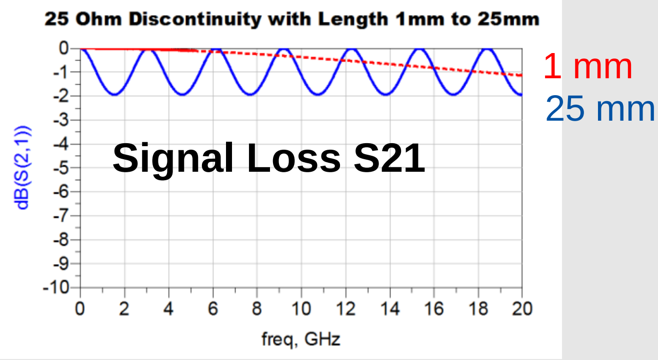
Stub vs Series Resonators

Stub Resonance

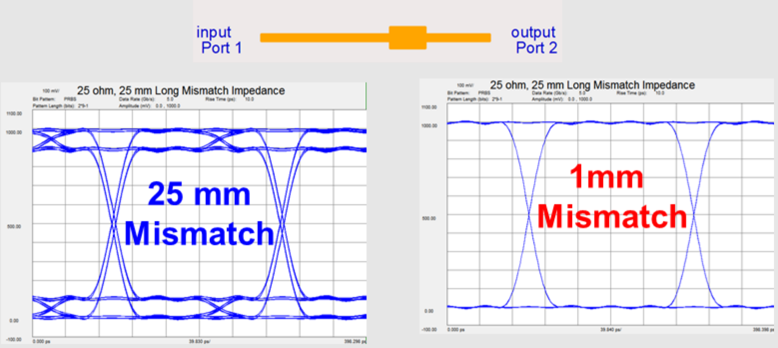


5 GB/s, PRBS 7

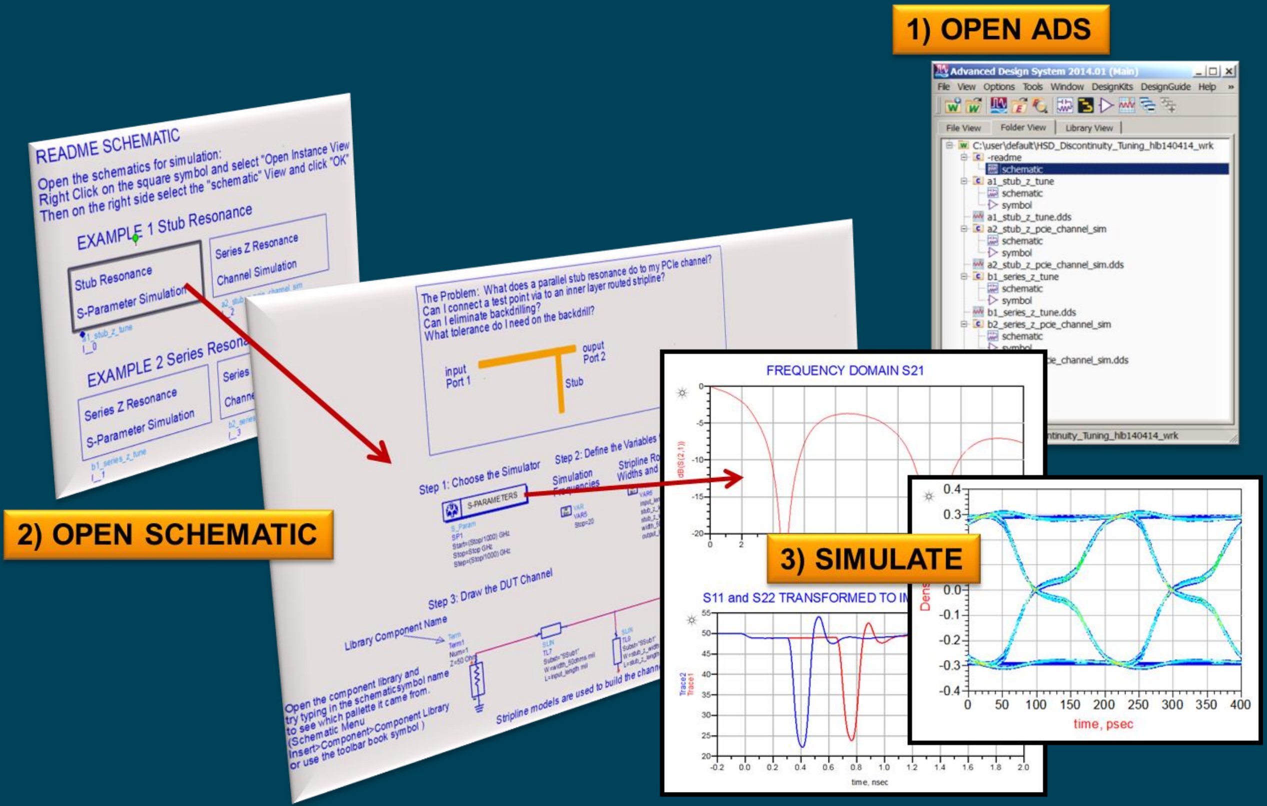
Series Resonance



5 GB/s, PRBS 7



Hands-on Impedance Lab



1) OPEN ADS

2) OPEN SCHEMATIC

3) SIMULATE

README SCHEMATIC

Open the schematics for simulation:
Right Click on the square symbol and select "Open Instance View"
Then on the right side select the "schematic" View and click "OK"

The Problem: What does a parallel stub resonance do to my PCIe channel?
Can I connect a test point via to an inner layer routed stripline?
Can I eliminate backdrilling?
What tolerance do I need on the backdrill?

Step 1: Choose the Simulator

Step 2: Define the Variables

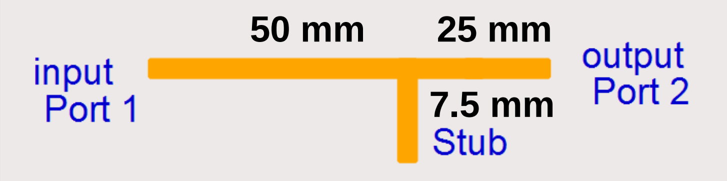
Step 3: Draw the DUT Channel

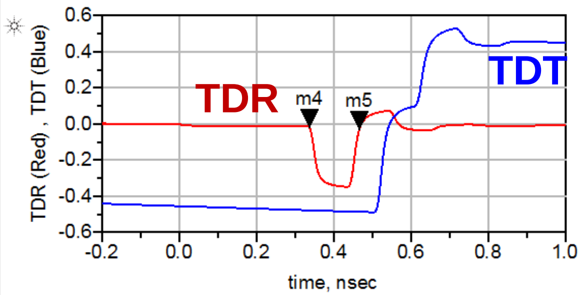
Open the component library and try typing in the schematic symbol name to see which pallette it came from.
(Schematic Menu
Insert>Component>Component Library
or use the toolbar book symbol)

Stripline models are used to build the channel

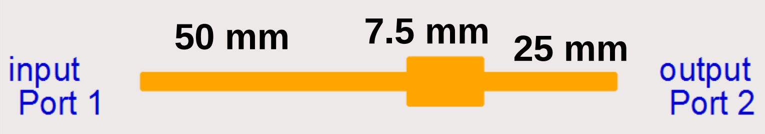
Hands-on Impedance Lab

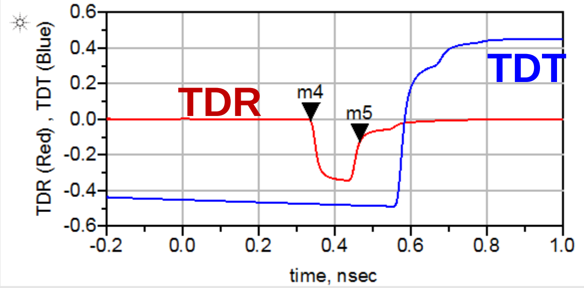
Stub Resonance





Series Resonance





Excess C and L Calculations

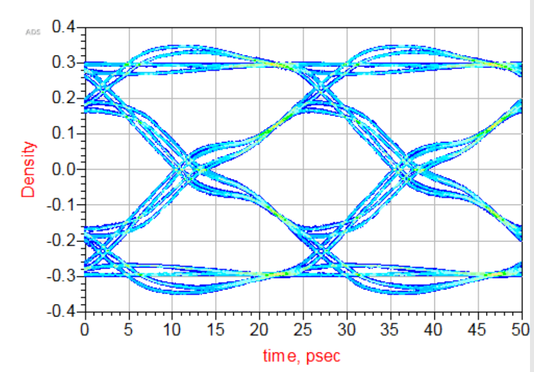
$$C_{\mathrm{Total}} = \frac{t_d}{Z_0} \qquad C = \frac{2\tau}{Z_0} = -\frac{2}{Z_0}\int_0^{+\infty} \mathrm{reflected\_n} \cdot dt$$

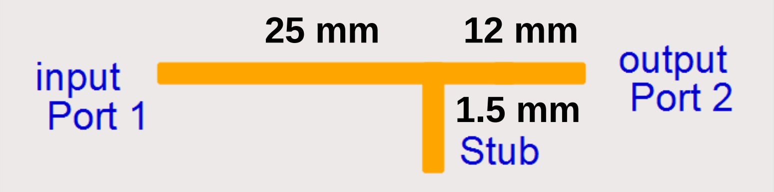
$$L_{\mathrm{Total}} = t_d Z_0 \qquad L = 2Z_0\tau = 2Z_0 \int_0 \mathrm{reflected\_n} \cdot dt$$

Integrate from Marker 4 to 5 to get Excess C = 1.4 pF

Why is the Stub So Bad?

Stub Resonance 25 Gb/s





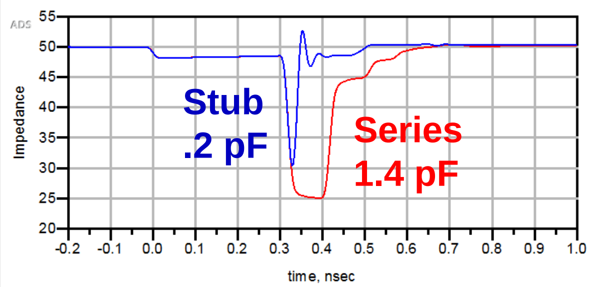
25 mm

12 mm

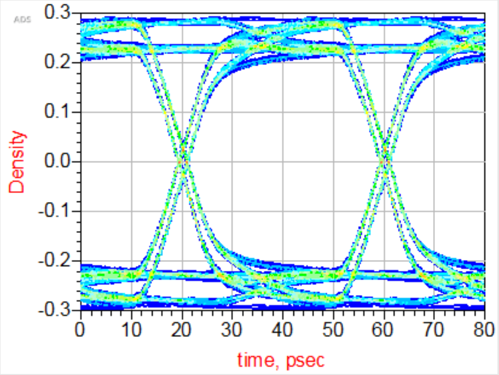
input
Port 1

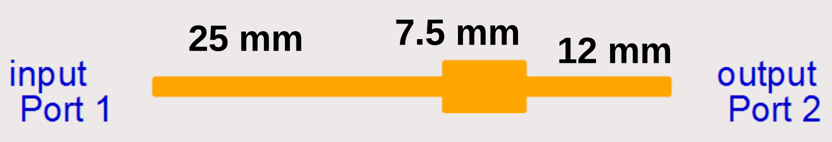
output
Port 2

1.5 mm
Stub



Series Resonance 25 Gb/s





25 mm

7.5 mm

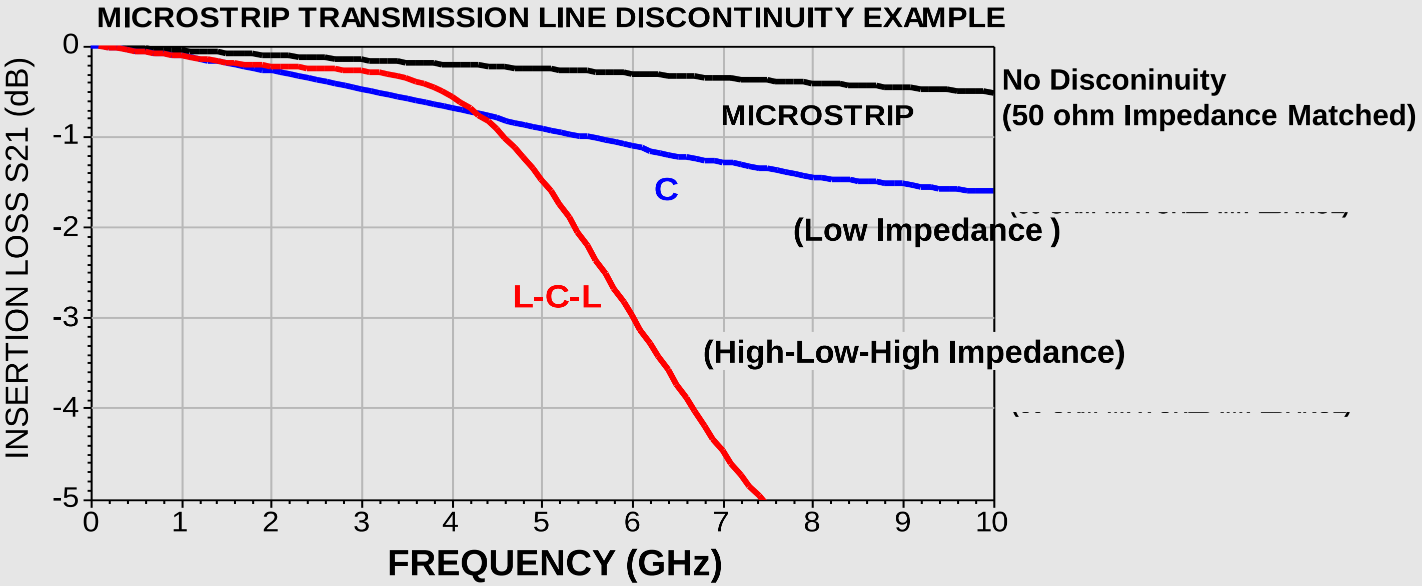
12 mm

input
Port 1

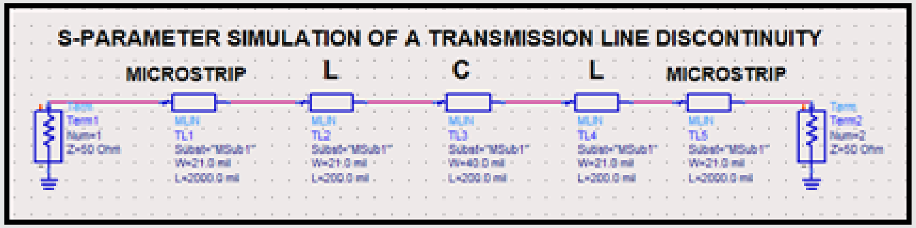
output
Port 2

Impedance Losses

Transition Discontinuity the size of a Via Transition on a 250mil Thick Test Fixture Board



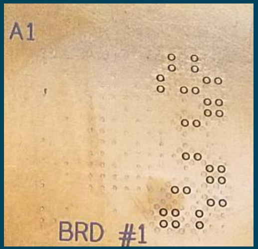
Keysight ADS Simulation



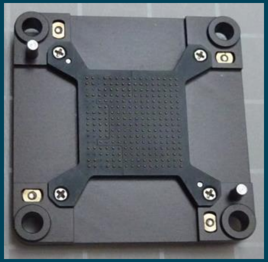
Signal Integrity Basics

Probe
GSG-GSG

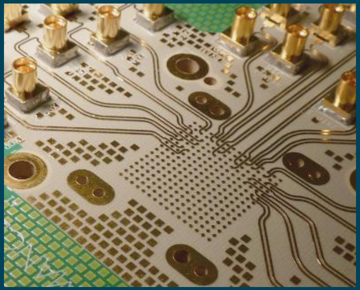
Probe to Socket
Interposer



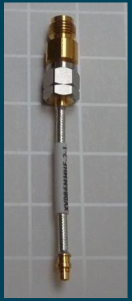
Socket
DUT



PCB Footprint
to Microstrip



PCB MMPX to
1.85mm Coax



40 Gb/s Sockets:
Dielectric losses are low – short path length
Impedance control is critical – every 5 mils counts.

Workshop Agenda

Noon to 1:30 pm ✓ Channel Simulations with Sockets
- Signal Integrity Basics

➡ 1:30 to 2:45 pm ○ SI Challenges with BGA Sockets
- Differential Signaling and Mode Conversion
- NEXT and FEXT coupling

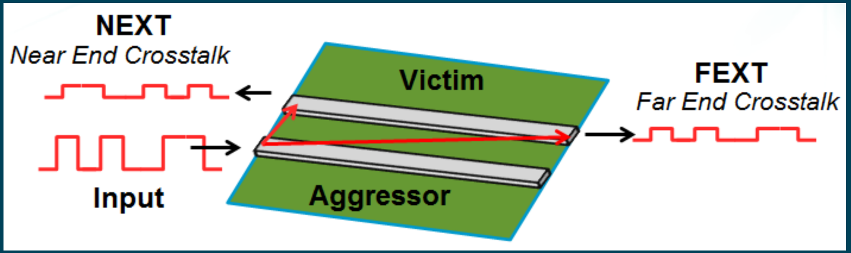
2:45 to 3:15 pm Break

3:15 to 4:30 pm ○ Measurements
- Fixture characterization and de-embedding

4:30 to 6:00 pm ○ Deconstructed Models
- Calibrated simulations
- The Transparent Socket

Each section includes a ~20 minute Hands-On Lab

High Frequency Coupling

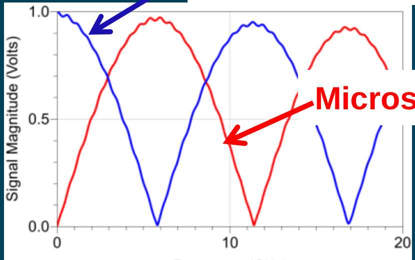


EM simulation for complex radiation and crosstalk.

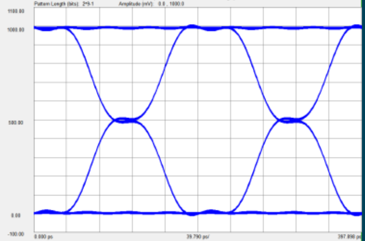
Identical
12mil Traces, 5mil Gap

Microstrip S21 Loss

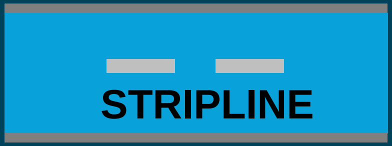
Microstrip FEXT

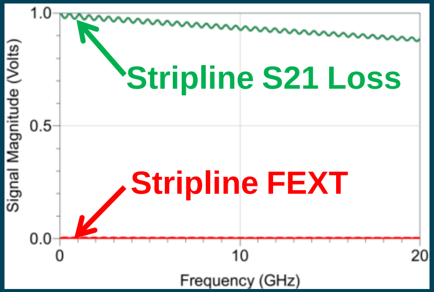


Microstrip 5Gbps Eye



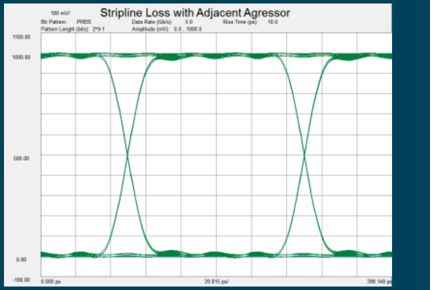
Stripline 5Gbps Eye





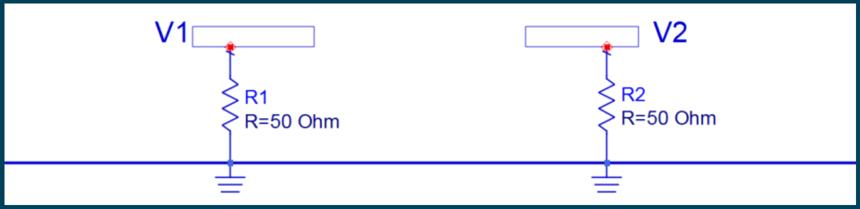
Stripline S21 Loss

Stripline FEXT



Differential Signaling

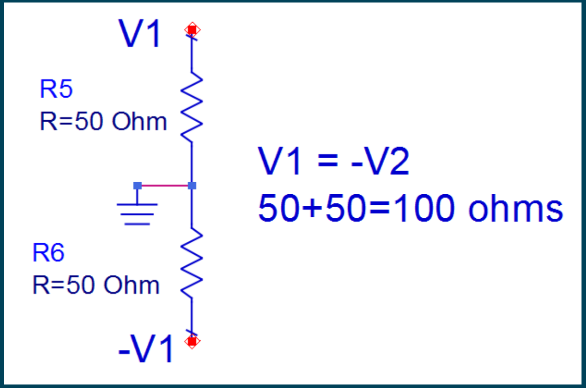
Start Simple: No Coupling



Vdifferential = V1-V2

- Differential signal drives the odd mode of a differential pair
- Differential Impedance seen by the Differential Signal
- Odd mode impedance of one line when driven in the odd mode by the differential signal.

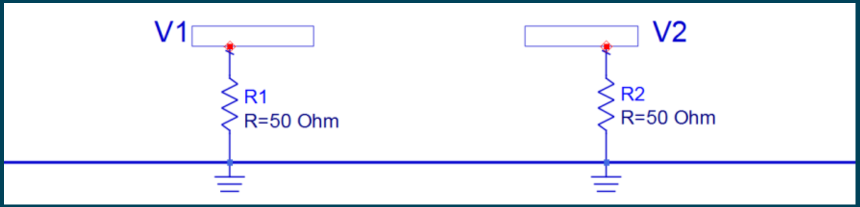
Zdifferential=2(Zodd)



V1 = -V2
50+50=100 ohms

Common Signaling

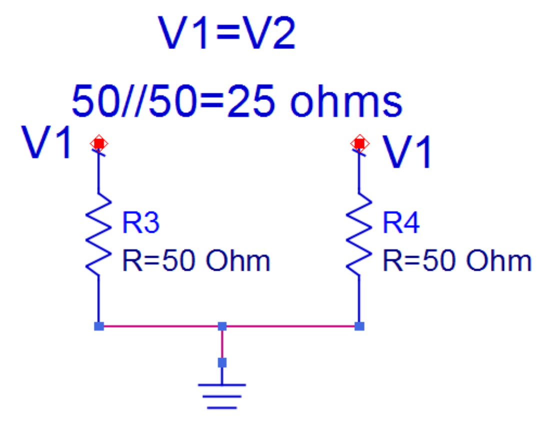
Start Simple: No Coupling



Vcommon = V1+ V2

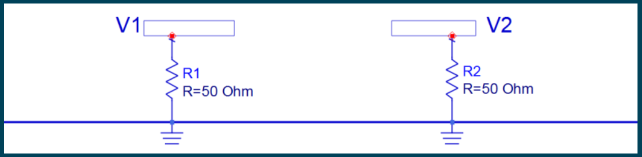
- Common Signal drives the even mode of differential pair
- Common Impedance seen by the Common Signal
- Even mode impedance of one line when driven in the even mode by the common signal.

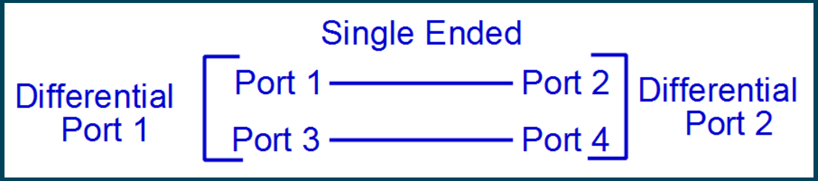
Zcommon=1/2(Zeven)



Imperfect Differential Signaling

When Vcommon ≠ 0




Single Ended
Differential Port 1
Port 1
Port 3
Port 2
Port 4
Differential Port 2

Multiple modes to excite and measure……

2 ports, so 4 measurements for each case 11, 21, 12, and 22:

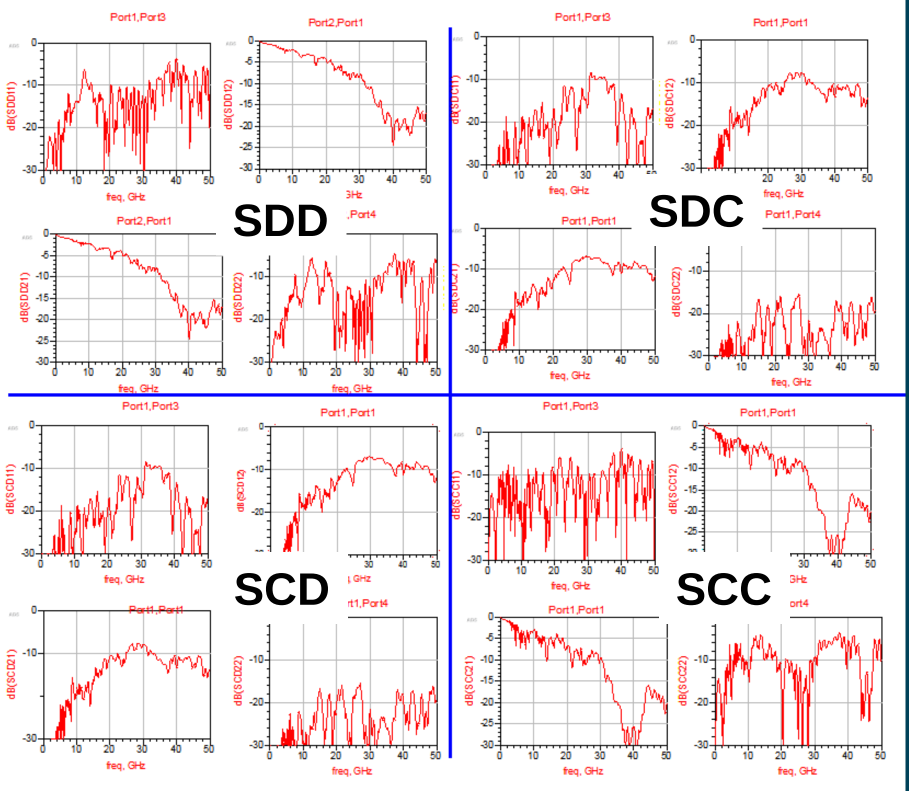
SDD	Differential signal in	→	differential signal out
SCC	Common signal in	→	common signal out
SCD	Differential signal in	→	common signal out
SDC	Common signal in	→	differential signal out

Mixed Mode S-Parameters

Differential In Common In

Differential Out

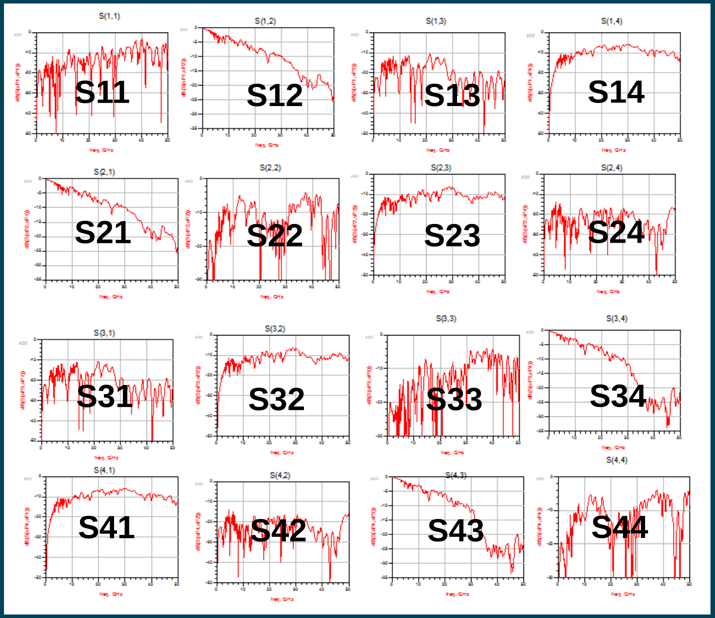
Common Out



SDD11 SDD12 | SDC11 SDC12
SDD21 SDD22 | SDC21 SDC22

SCD11 SCD12 | SCC11 SCC12
SCD21 SCD22 | SCC21 SCC22

Matrix Math Single Ended to Differential



SDD11=0.5*(S11-S13-S31+S33)
SDD21=0.5*(S21-S23-S41+S43)
SDD12=0.5*(S12-S14-S32+S34)
SDD22=0.5*(S22-S24-S42+S44)

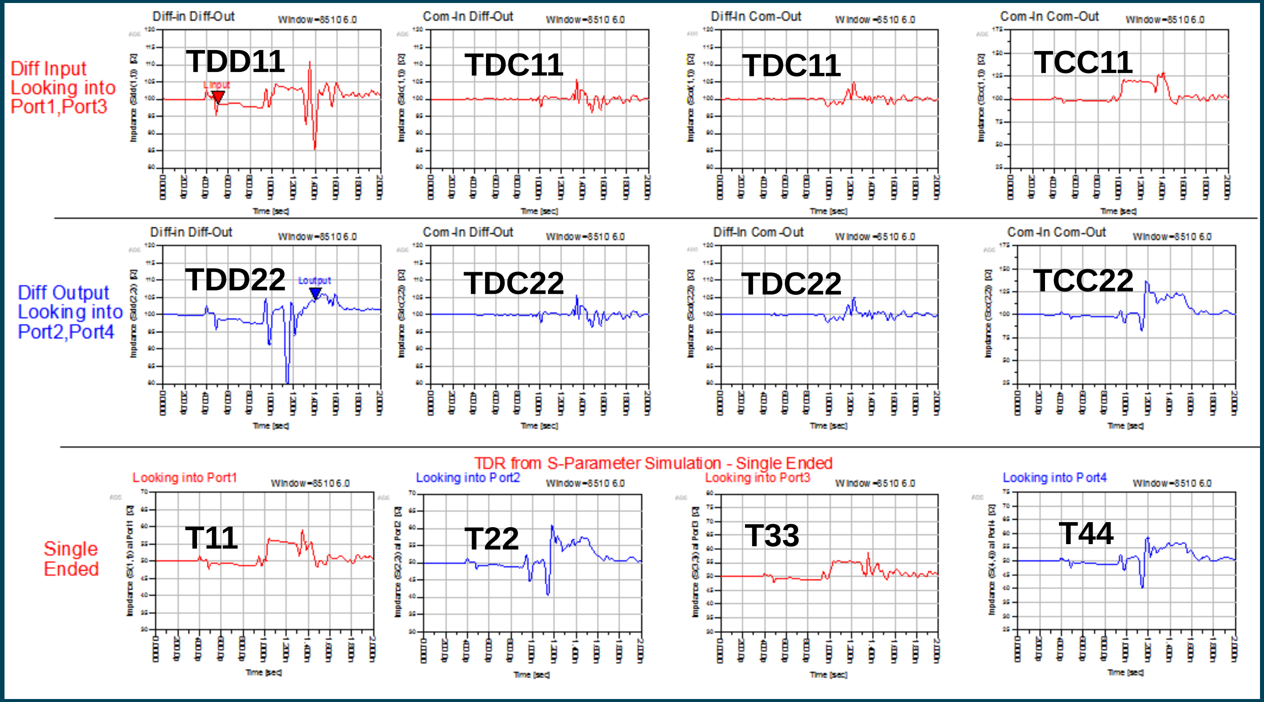
SCD11=0.5*(S11-S13+S31-S33)
SCD21=0.5*(S21-S23+S41-S43)
SCD12=0.5*(S12-S14+S32-S34)
SCD22=0.5*(S22-S24+S42-S44)

SCD11=0.5*(S11+S13-S31-S33)
SCD21=0.5*(S21+S23-S41-S43)
SCD12=0.5*(S12+S14-S32-S34)
SCD22=0.5*(S22+S24-S42-S44)

SCC11=0.5*(S11+S13-S31-S33)
SCC21=0.5*(S21+S23-S41-S43)
SCC12=0.5*(S12+S14-S32-S34)
SCC22=0.5*(S22+S24-S42-S44)

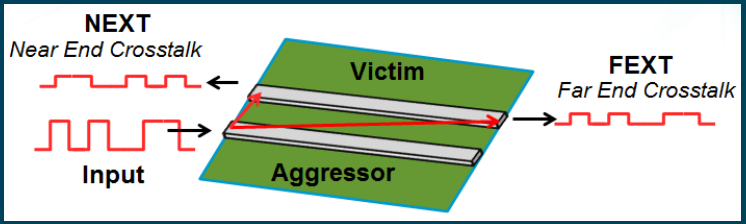
…..and the T-Parameters

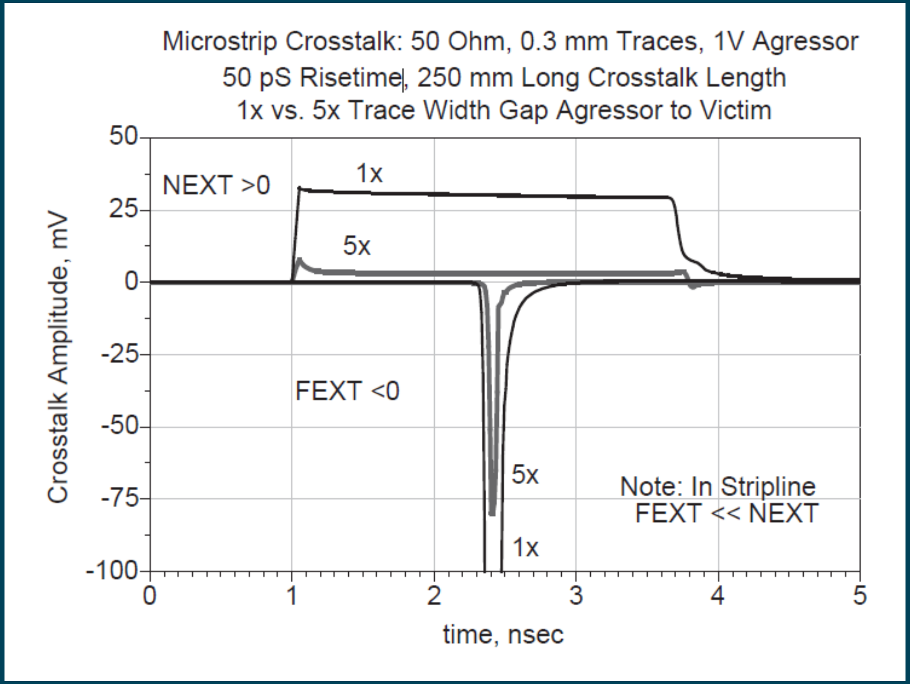
TDR Mixed Mode and Single Ended



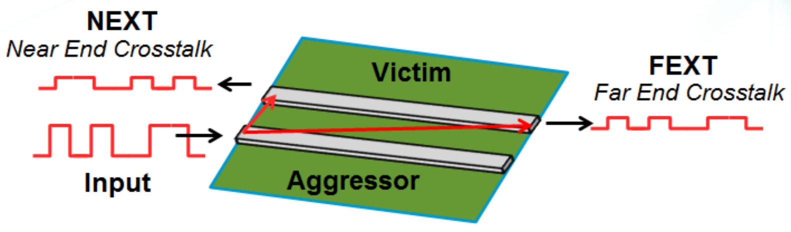
Coupling causes mode conversion and Zdiff ≠ 2*(Zsingle ended)
Coupling adds capacitance, so Single Ended Z must go up for Zdiff=100ohms

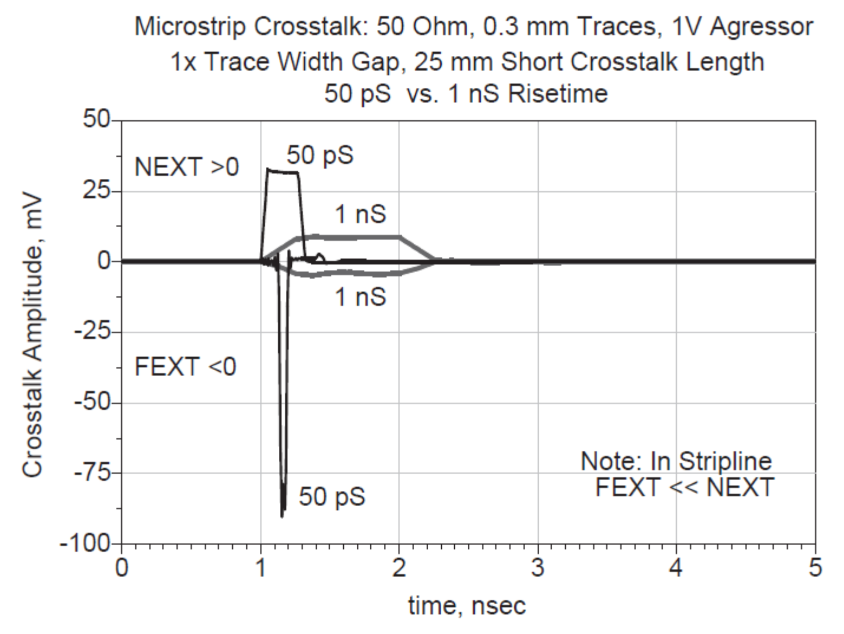
NEXT and FEXT vs Gap Spacing





NEXT and FEXT vs. Rise Time



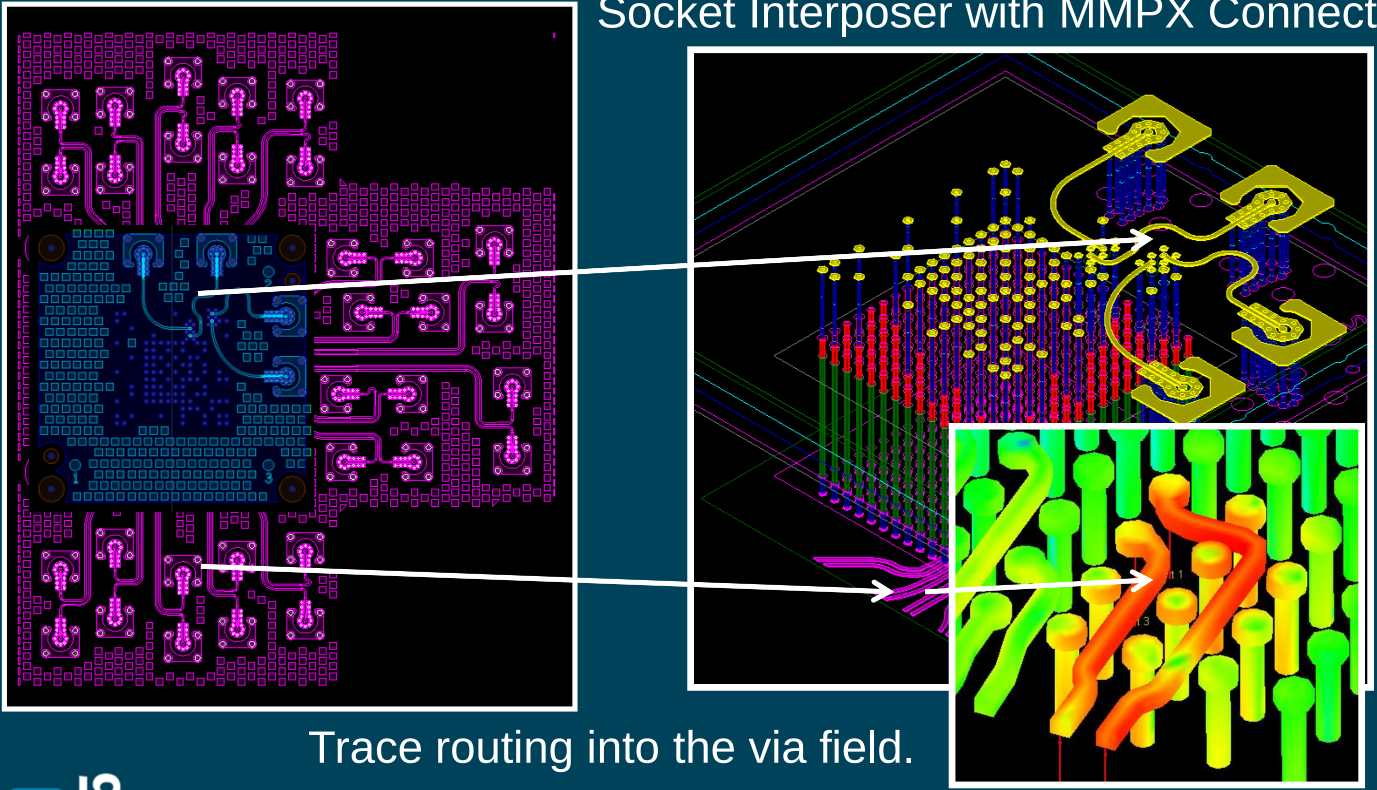


What is ~~“Ground”~~ to the Signal

Think “return current” path!

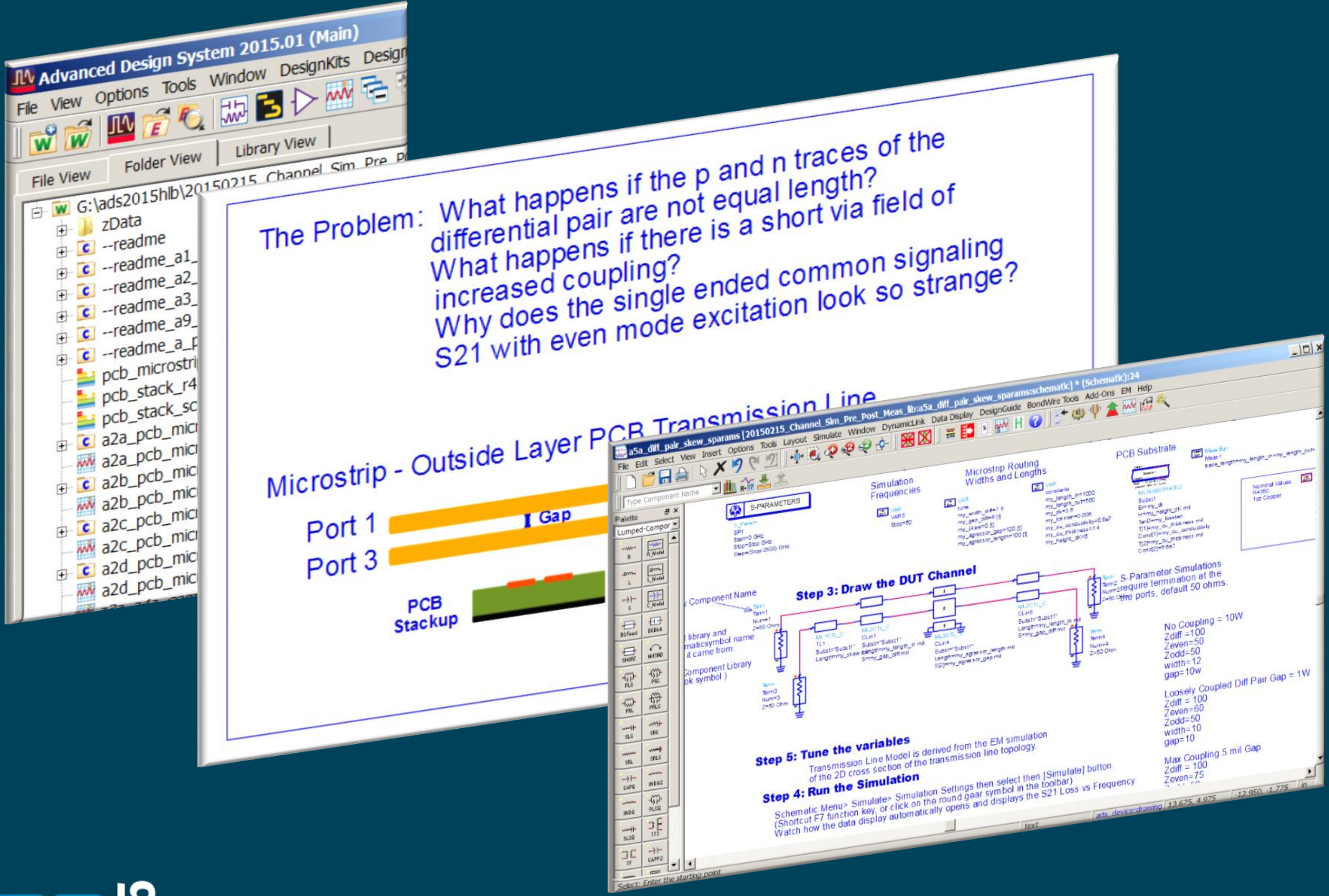
Socket Characterization PCB

Socket Interposer with MMPX Connectors



Trace routing into the via field.

Lab #2 – Differential Pairs



The Problem: What happens if the p and n traces of the differential pair are not equal length?
What happens if there is a short via field of increased coupling?
Why does the single ended common signaling S21 with even mode excitation look so strange?

Microstrip - Outside Layer PCB Transmission Line

Step 3: Draw the DUT Channel

S-Parameter Simulations require termination at the ports, default 50 ohms.

No Coupling = 10W
Zdiff =100
Zeven=50
Zodd=50
width=12
gap=10w

Loosely Coupled Diff Pair Gap = 1W
Zdiff = 100
Zeven=60
Zodd=50
width=10
gap=10

Max Coupling 5 mil Gap
Zdiff = 100
Zeven=75

Step 5: Tune the variables
Transmission Line Model is derived from the EM simulation of the 2D cross section of the transmission line topology.

Step 4: Run the Simulation
Schematic Menu> Simulate> Simulation Settings then select then [Simulate] button.
(Shortcut F7 function key, or click on the round gear symbol in the toolbar)
Watch how the data display automatically opens and displays the S21 Loss vs Frequency

Workshop Agenda

Noon to 1:30 pm	✓ Channel Simulations with Sockets • Signal Integrity Basics
1:30 to 2:45 pm	✓ S-Parameters: • Frequency and Time Domains • Differential Signaling
➡ 2:45 to 3:15 pm	Break
3:15 to 4:30 pm	○ Measurements • Fixture characterization and de-embedding
4:30 to 6:00 pm	○ Deconstructed Models • Calibrated simulations • The Transparent Socket

Each section includes a ~20 minute Hands-On Lab

Workshop Agenda

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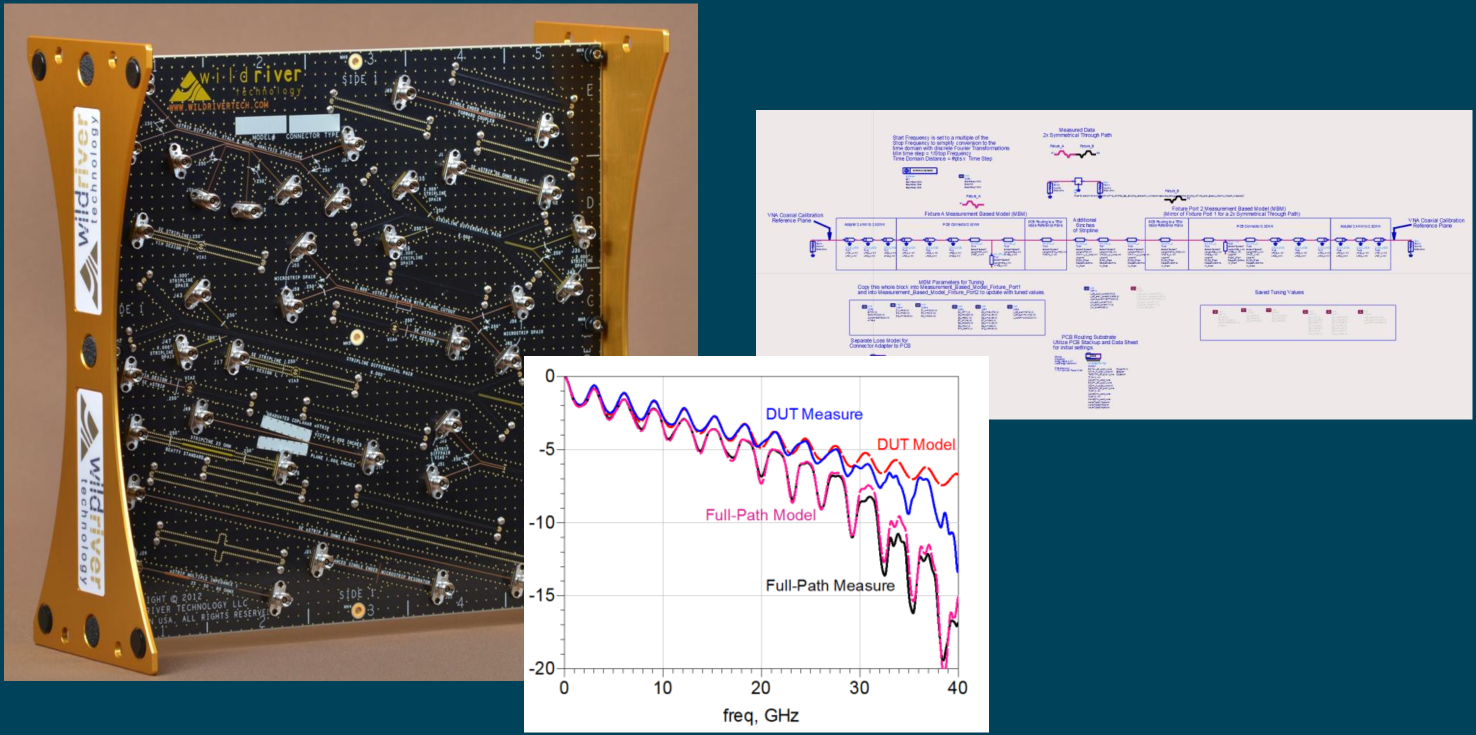
- Calibrated simulations
- The Transparent Socket

Each section includes a ~20 minute Hands-On Lab

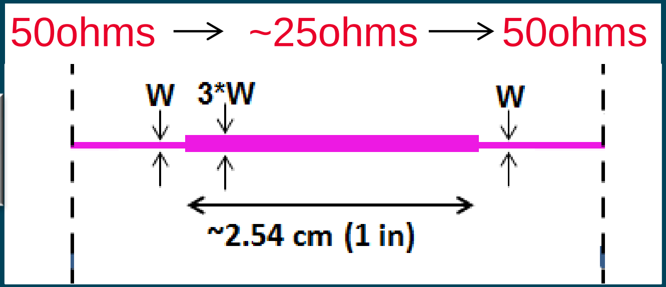
Matching Measurements with Simulations



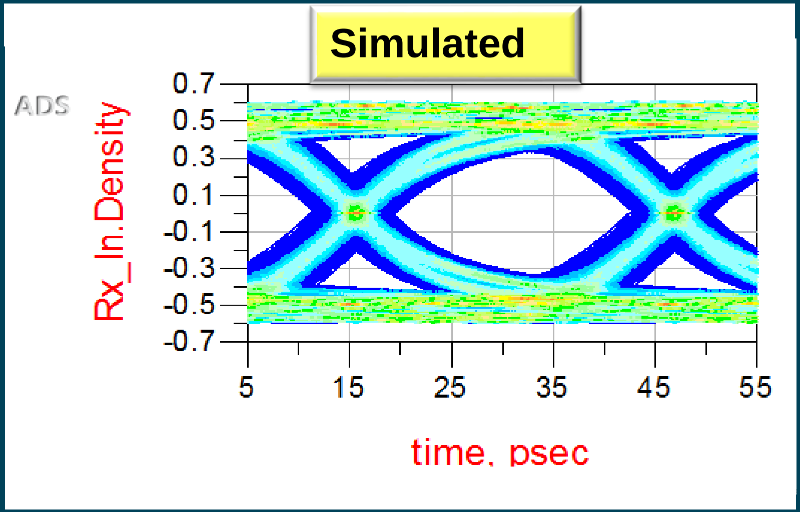
Wild River Technology CMP-28 PCB Platform

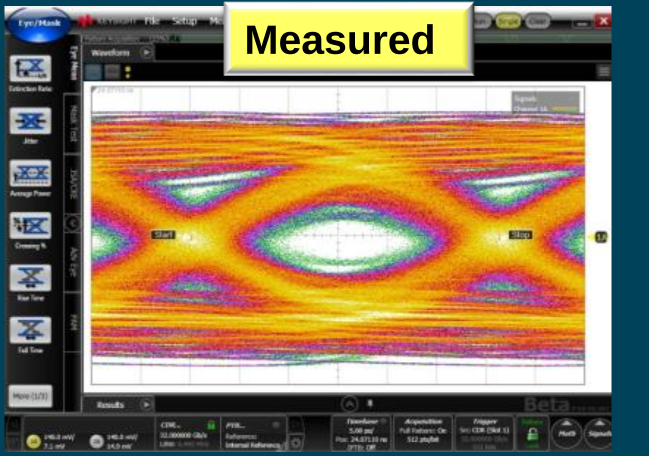
Do I Trust Simulation or Measurement

Simple Change in PCB Trace Width



32 Gb/s PRBS9

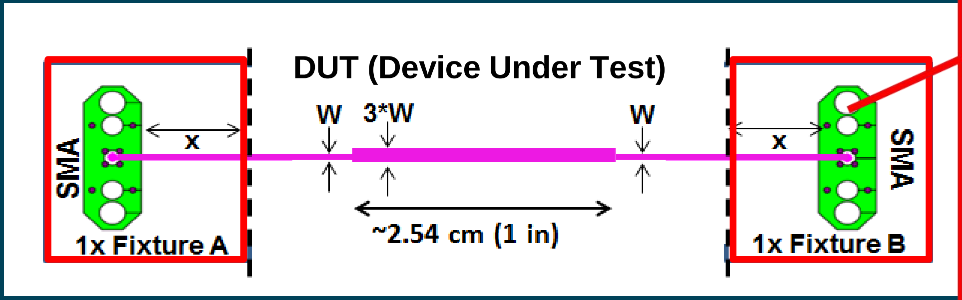

Simulated

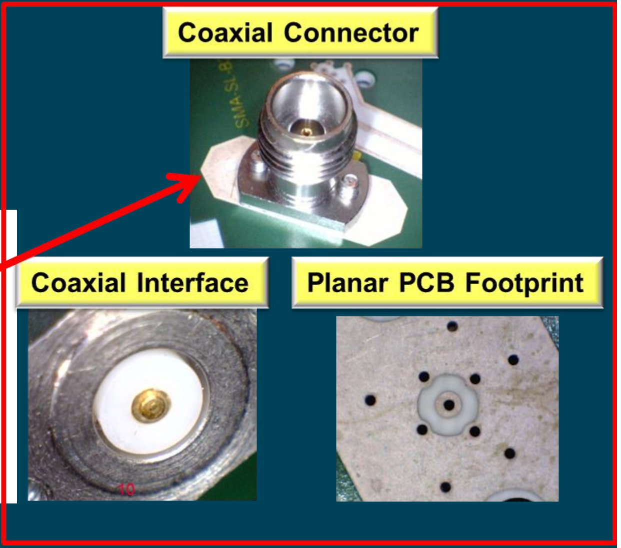

Measured

Measurement Fixtures

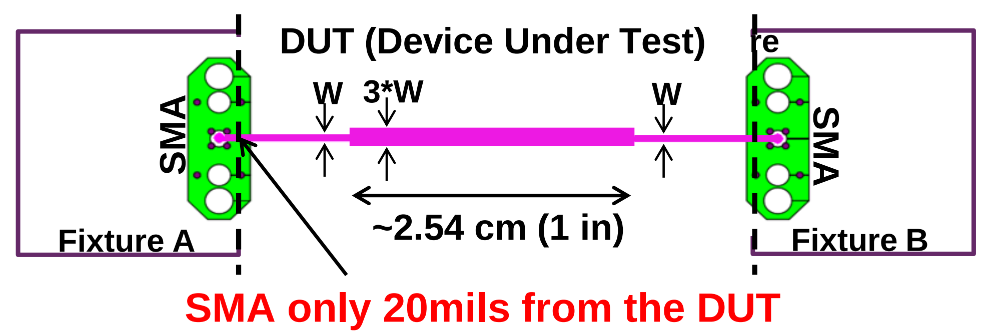
*A **PCB Fixture** transitions from the coax connector to the planar PCB transmission line.*

Standard coaxial SOLT calibrations only calibrate to the end of the coaxial cable!

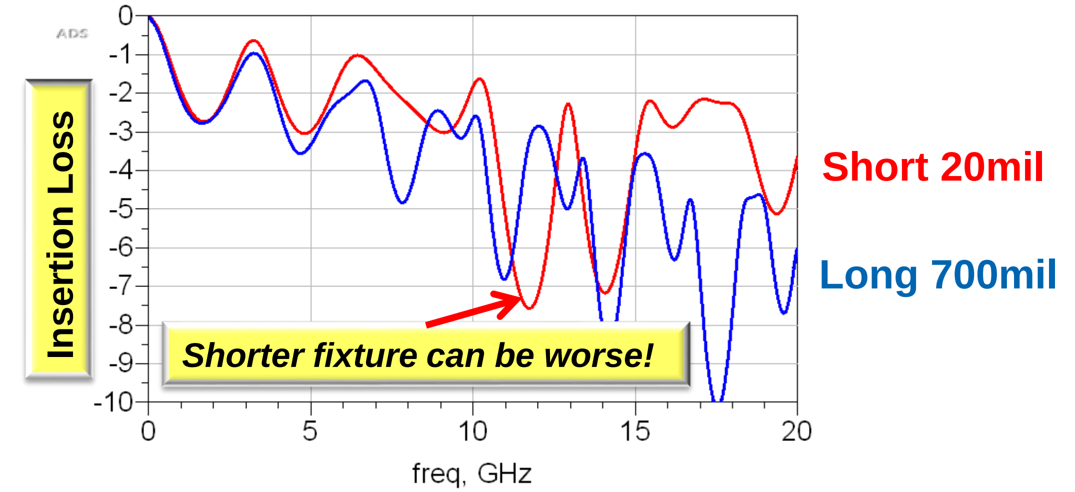




Can I Ignore the Fixture if is Short?

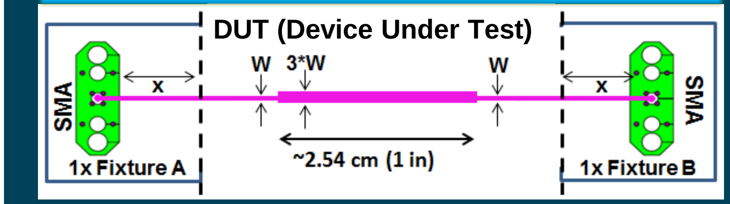


A shorter PCB path does not eliminate impedance reflections from the connector to PCB transition



Fixture Removal Benefits

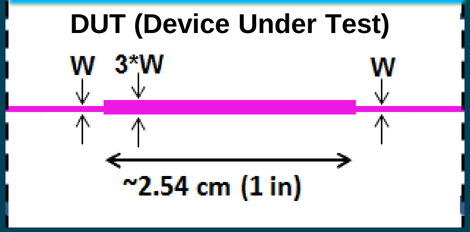
Full-Path Fixture Plus DUT



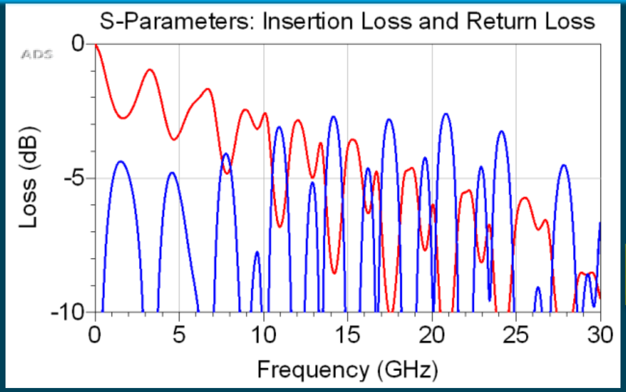
FIXTURE DE-EMBED

T-Matrix

Only the DUT Behavior



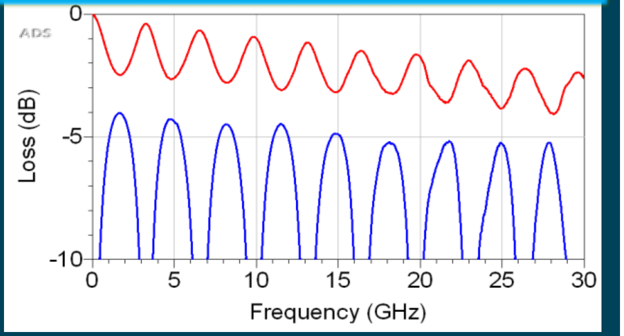
S-Parameters before Fixture De-embed



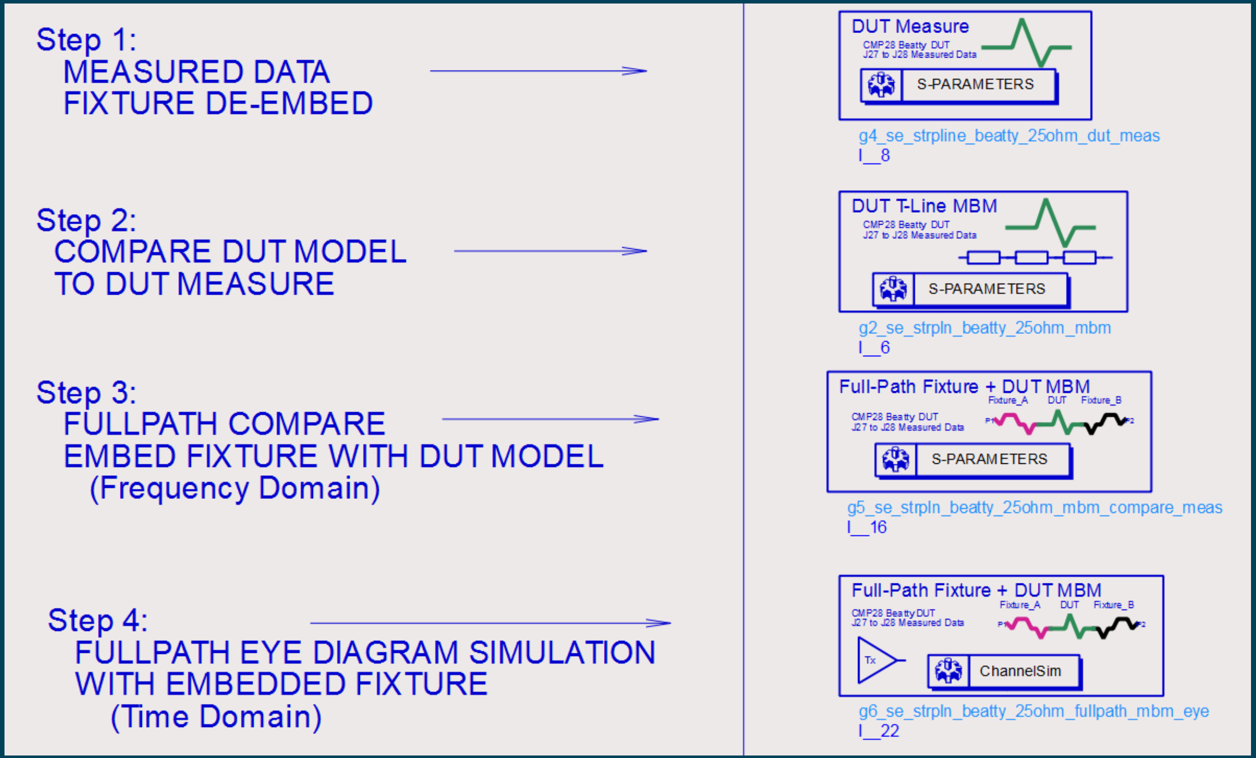
FIXTURE DE-EMBED

T-Matrix

Measured S-Parameters after Fixture De-embed



4-Step Measure / Model Verify



Step 1:
MEASURED DATA
FIXTURE DE-EMBED

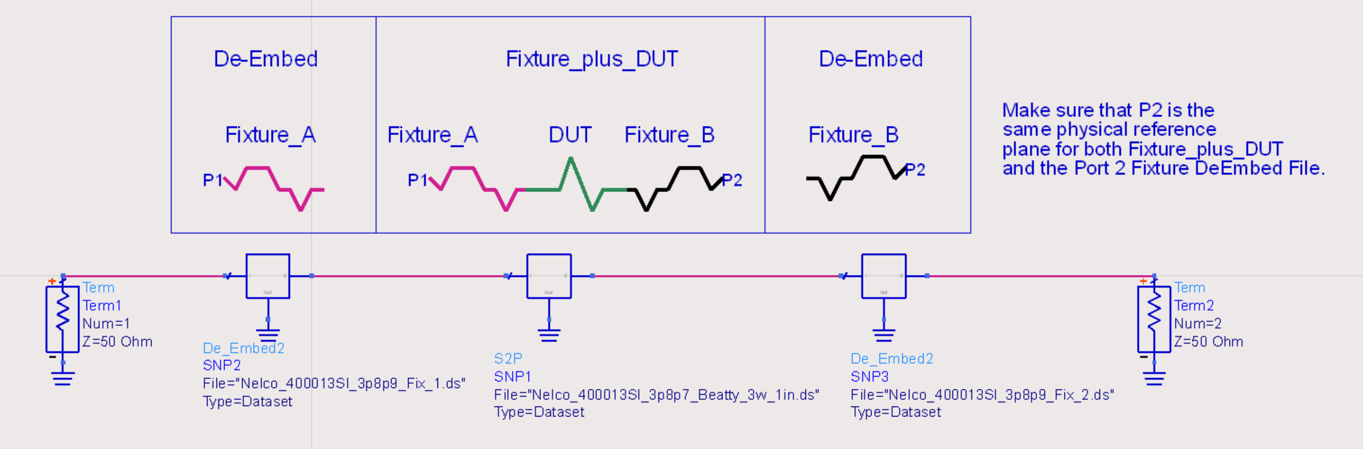
Step 2:
COMPARE DUT MODEL
TO DUT MEASURE

Step 3:
FULLPATH COMPARE
EMBED FIXTURE WITH DUT MODEL
(Frequency Domain)

Step 4:
FULLPATH EYE DIAGRAM SIMULATION
WITH EMBEDDED FIXTURE
(Time Domain)

Step 1 Fixture Removal for S_{DUT}

Schematic for de-embedding the fixture from the full path measurement of DUT + fixtures.



Make sure that P2 is the same physical reference plane for both Fixture_plus_DUT and the Port 2 Fixture DeEmbed File.

Term
Term1
Num=1
Z=50 Ohm

De_Embed2
SNP2
File="Nelco_400013SI_3p8p9_Fix_1.ds"
Type=Dataset

S2P
SNP1
File="Nelco_400013SI_3p8p7_Beatty_3w_1in.ds"
Type=Dataset

De_Embed2
SNP3
File="Nelco_400013SI_3p8p9_Fix_2.ds"
Type=Dataset

Term
Term2
Num=2
Z=50 Ohm

The inverse T-Matrix is used for de-embedding

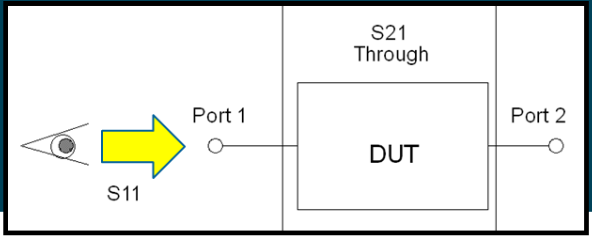
$$T_{DUT} = T_{fixture\_A}^{-1} \, T_{fullpath} \, T_{fixture\_B}^{-1}$$

Output De-Embedded DUT S_Parameters

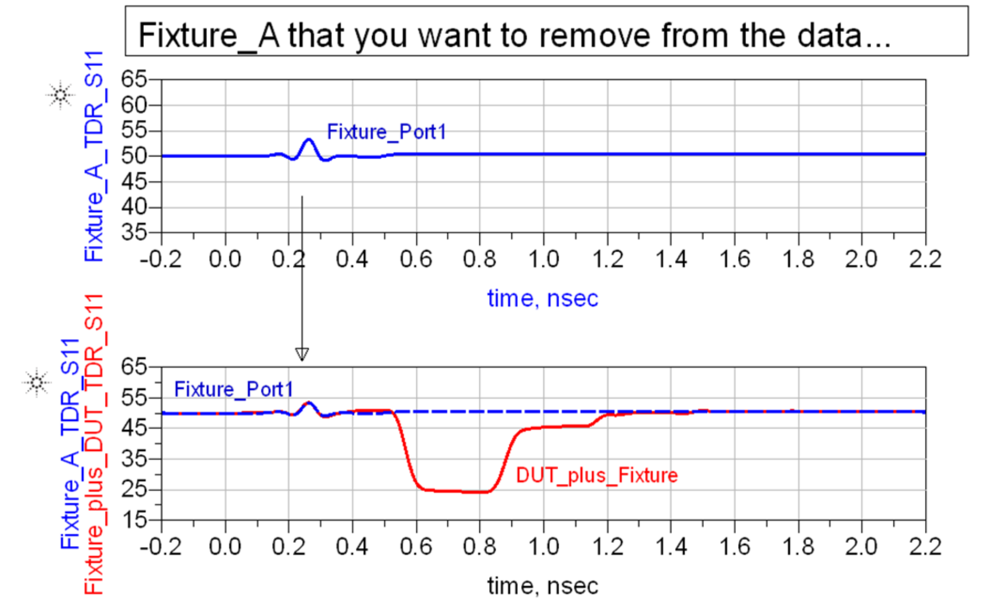
S_{DUT}

Verify Fixture for De-embedding

TDR from S11



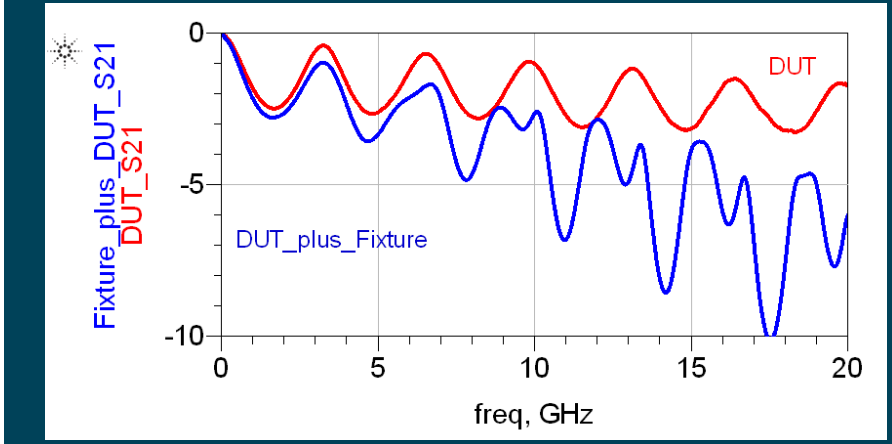
Time domain verifies that the fixture data matches with the actual DUT Fixture

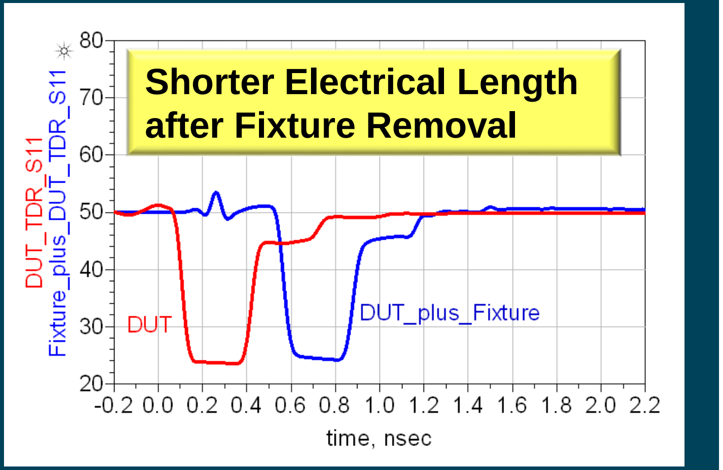


Before and After Fixture Removal

Frequency Domain

Time Domain



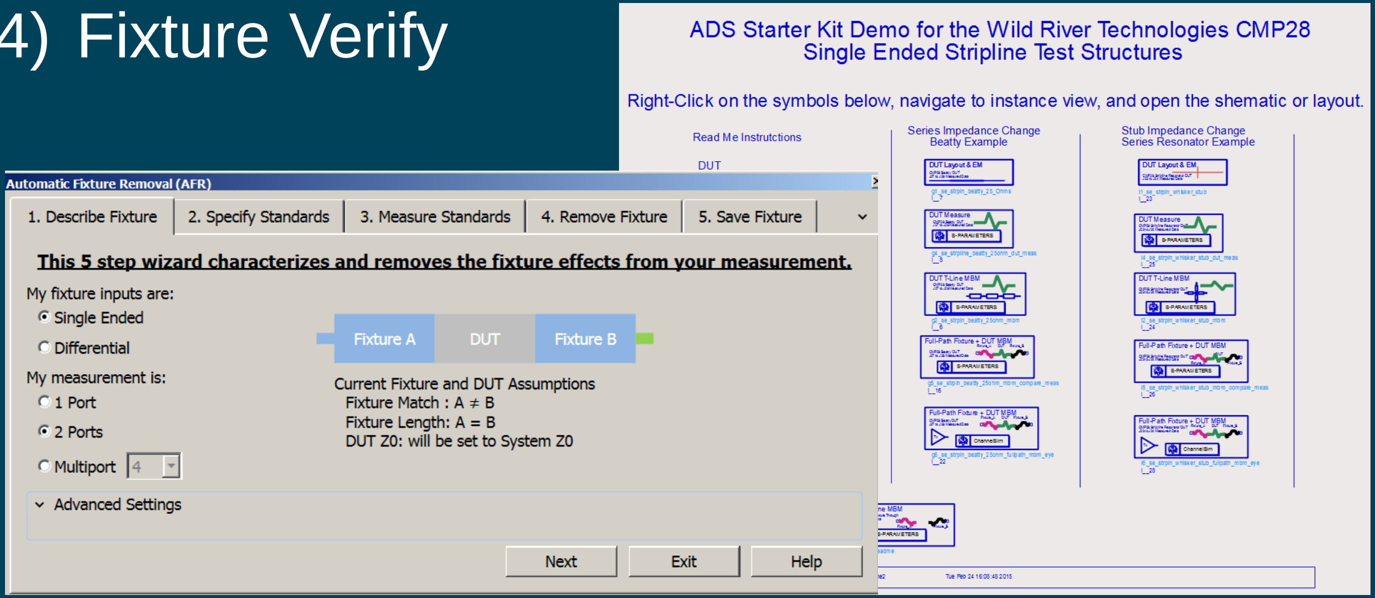


Shorter Electrical Length after Fixture Removal

DUT with Fixture Removed in RED
DUT with Fixture in Blue

Fixture De-Embedding Lab #3

1) Fixture from 2x Through
2) Fixture from AFR
3) Fixture from MBM
4) Fixture Verify



ADS Starter Kit Demo for the Wild River Technologies CMP28
Single Ended Stripline Test Structures

Right-Click on the symbols below, navigate to instance view, and open the shematic or layout.

Automatic Fixture Removal (AFR)

This 5 step wizard characterizes and removes the fixture effects from your measurement.

My fixture inputs are:
● Single Ended
○ Differential

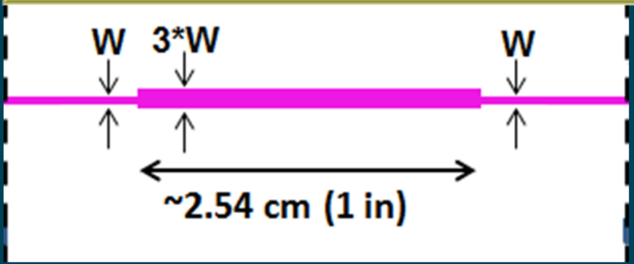
My measurement is:
○ 1 Port
● 2 Ports
○ Multiport 4

Current Fixture and DUT Assumptions
Fixture Match : A ≠ B
Fixture Length: A = B
DUT Z0: will be set to System Z0

DUT Simulation vs Measurement

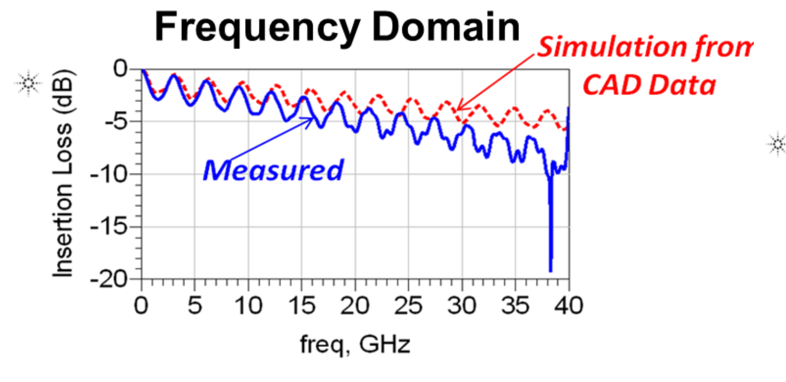
Getting closer…..

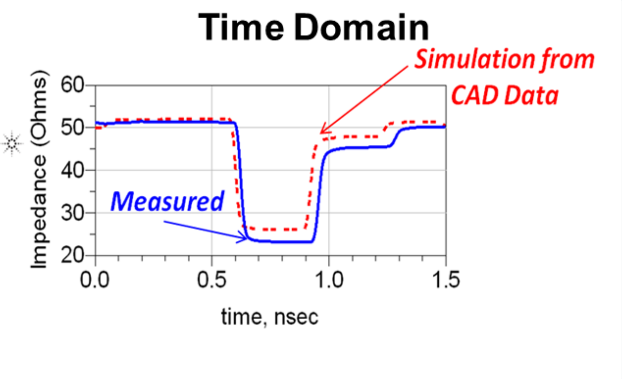
SIMPLE CHANGE IN PCB TRACE WIDTH



PCB Stripline

EM Simulation Fails to Match Measurement at High Frequencies





PCB Design Data vs "As-Fabricated"

Specify Everything in the Fab Doc!

Fabrication Document

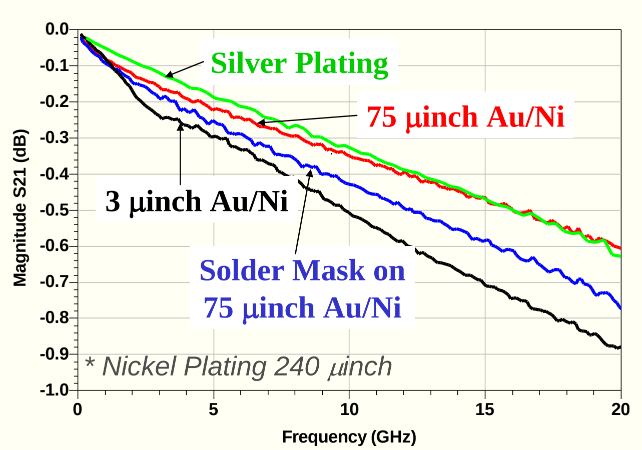
✓ Fabrication Notes
✓ Fabrication Details
✓ Drill Table

Repeatability can be more important than lower loss at high frequencies.

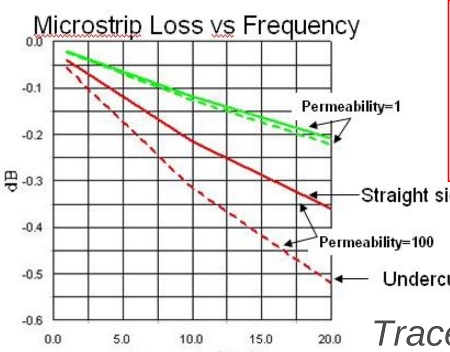
- **Laminate Materials:**
  - Manufacturer Material Tolerances/Repeatability
  - Pre-Preg "B-Stage" Epoxy vs. Core Material
  - Glass Weave
  - **Copper Thickness and Profile**
- **PCB Manufacturing:**
  - **Finished Hole Size vs. Drill Size**
  - Via Back Drilling Tolerance
  - Drill Location Tolerance
  - Edge Routing Tolerance
  - Microstrip plating vs soldermask
  - Copper Thieving
  - Copper Surface Treatment

Microstrip Coatings

Loss Per Inch vs Plating Type



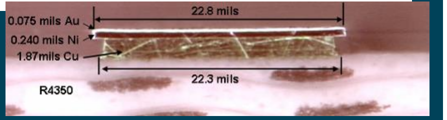
Effect of Nickel Permeability



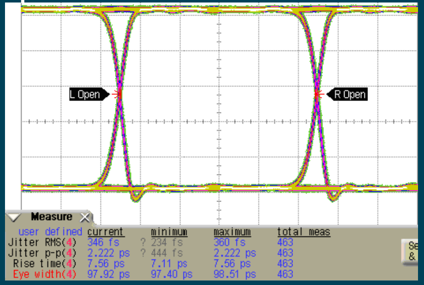
Skin Depth

$$\delta = \sqrt{\frac{2}{\omega \mu \sigma}}$$

Trace Edge Effects

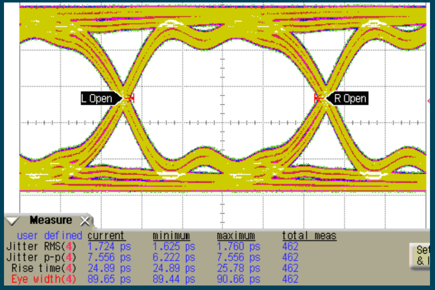


Input 10 GBit PRBS 2^31-1



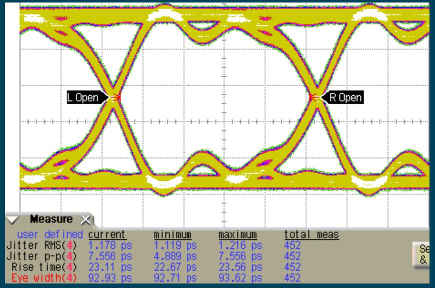
```
user defined current      minimum    maximum    total meas
Jitter RMS(4)  346 fs    ? 234 fs    360 fs     463
Jitter p-p(4)  2.222 ps  ? 444 fs    2.222 ps   463
 Rise time(4)  7.56 ps     7.11 ps   7.56 ps    463
 Eye width(4)  97.92 ps    97.40 ps  98.51 ps   463
```

After 10” Immersion Au/Ni



```
user defined current      minimum    maximum    total meas
Jitter RMS(4)  1.724 ps  1.625 ps   1.760 ps   462
Jitter p-p(4)  7.556 ps  6.222 ps   7.556 ps   462
 Rise time(4)  24.89 ps  24.89 ps   25.78 ps   462
 Eye width(4)  89.65 ps  89.44 ps   90.66 ps   462
```

After 10” Electroplate. Thick Au/Ni



```
user defined current      minimum    maximum    total meas
Jitter RMS(4)  1.178 ps  1.119 ps   1.216 ps   452
Jitter p-p(4)  7.556 ps  4.889 ps   7.556 ps   452
 Rise time(4)  23.11 ps  22.67 ps   23.56 ps   452
 Eye width(4)  92.93 ps  92.71 ps   93.62 ps   452
```

Glass Weave for the PCB fixture

1080 with the gaps is less expensive and commonly used.

3313 with the flat glass weave is popular for microvias to provide for better lasered hole uniformity.

If left unspecified, which one will the fabricator choose?

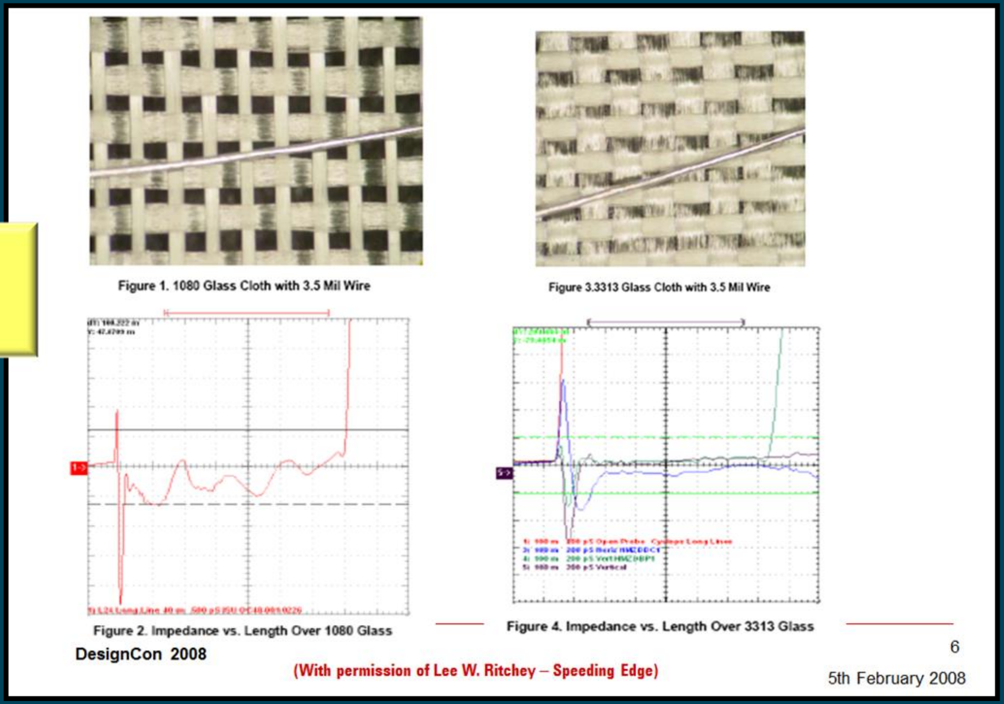


Figure 1. 1080 Glass Cloth with 3.5 Mil Wire

Figure 3.3313 Glass Cloth with 3.5 Mil Wire

Figure 2. Impedance vs. Length Over 1080 Glass

Figure 4. Impedance vs. Length Over 3313 Glass

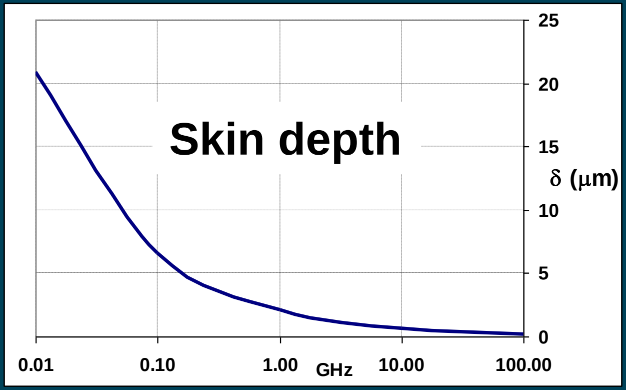
DesignCon 2008

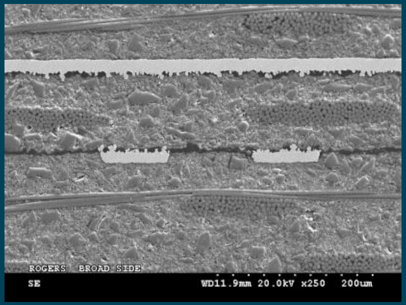
(With permission of Lee W. Ritchey – Speeding Edge)

6

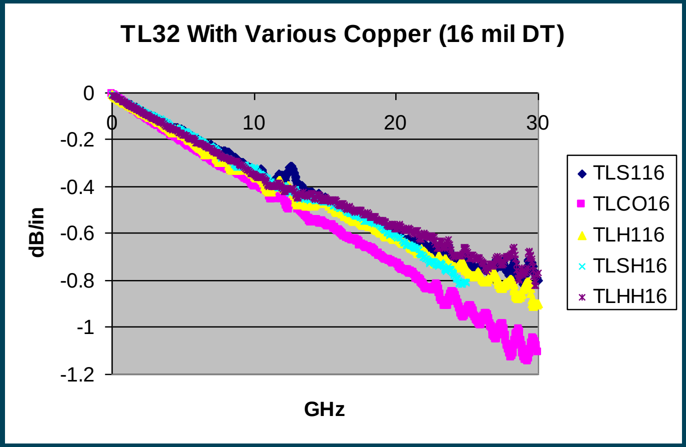
5th February 2008

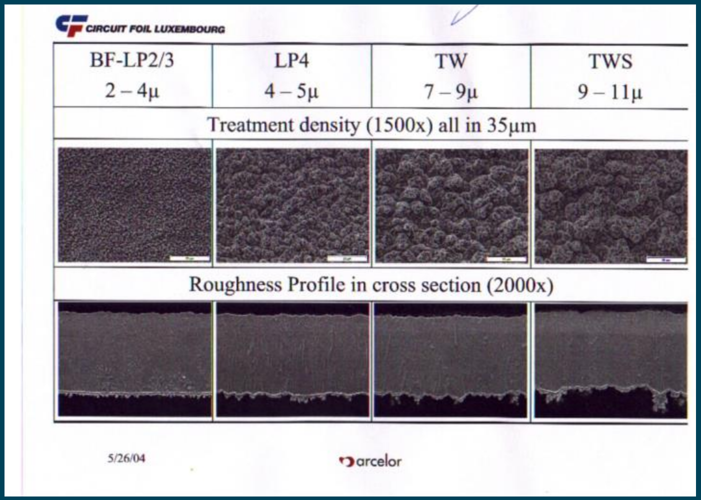
Copper Profile for the PCB Fixture





If left unspecified, which copper profile will they choose?


TL32 With Various Copper (16 mil DT)


CIRCUIT FOIL LUXEMBOURG

BF-LP2/3	LP4	TW	TWS
2 – 4µ	4 – 5µ	7 – 9µ	9 – 11µ

Treatment density (1500x) all in 35µm

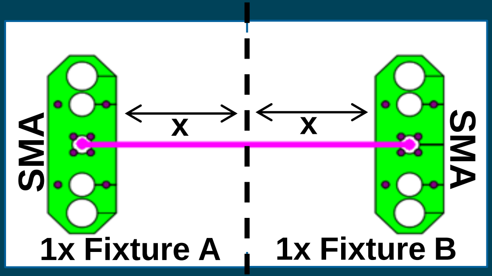
Roughness Profile in cross section (2000x)

5/26/04

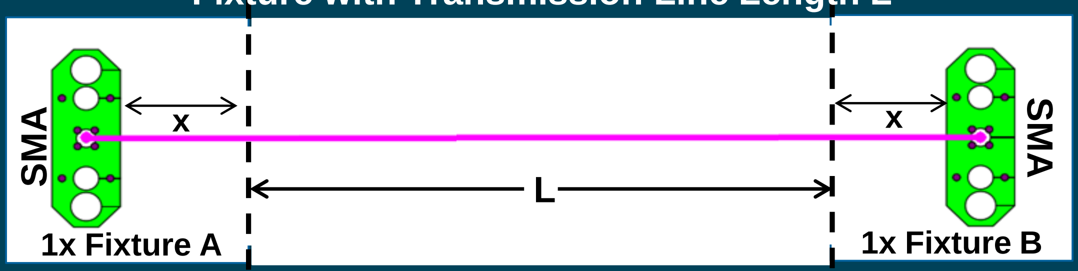
arcelor

PCB Test Structures for as-Fabricated Tolerances

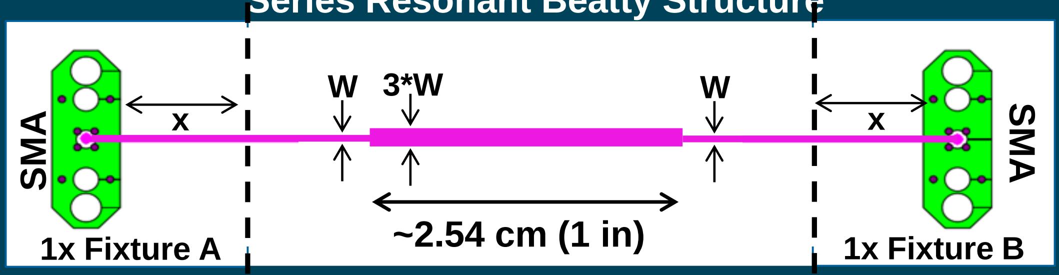
2x Through for Fixture Removal


Fixture with Length 2x

Long Transmission Line for conductor and dielectric losses.

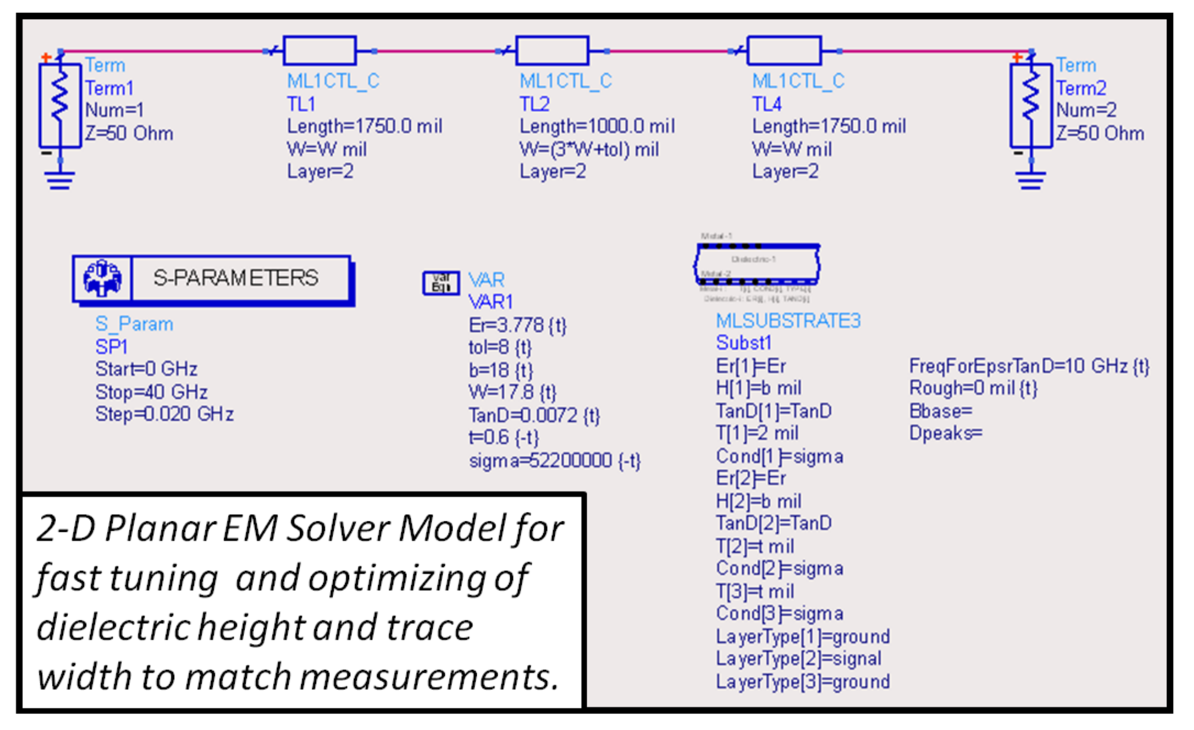

Fixture with Transmission Line Length L

Additional data on trace etching and dielectric height.


Series Resonant Beatty Structure

Step 2 - Tune As-Fabricated Properties

Fast Tune 2D-Planar Model Parameters to Match Measured Data



Term
Term1
Num=1
Z=50 Ohm

ML1CTL_C
TL1
Length=1750.0 mil
W=W mil
Layer=2

ML1CTL_C
TL2
Length=1000.0 mil
W=(3*W+tol) mil
Layer=2

ML1CTL_C
TL4
Length=1750.0 mil
W=W mil
Layer=2

Term
Term2
Num=2
Z=50 Ohm

S-PARAMETERS
S_Param
SP1
Start=0 GHz
Stop=40 GHz
Step=0.020 GHz

VAR
VAR1
Er=3.778 {t}
tol=8 {t}
b=18 {t}
W=17.8 {t}
TanD=0.0072 {t}
t=0.6 {-t}
sigma=52200000 {-t}

MLSUBSTRATE3
Subst1
Er[1]=Er
H[1]=b mil
TanD[1]=TanD
T[1]=2 mil
Cond[1]=sigma
Er[2]=Er
H[2]=b mil
TanD[2]=TanD
T[2]=t mil
Cond[2]=sigma
T[3]=t mil
Cond[3]=sigma
LayerType[1]=ground
LayerType[2]=signal
LayerType[3]=ground

FreqForEpsrTanD=10 GHz {t}
Rough=0 mil {t}
Bbase=
Dpeaks=

2-D Planar EM Solver Model for fast tuning and optimizing of dielectric height and trace width to match measurements.

** Simple T-Line model with out the complexity of fixture connections*

Where to Start Tuning

*PCB Frequency Dependent Losses can be separated into **Conductor** and **Dielectric** Losses*

$$\alpha_{dB} = \alpha_{cond} + \alpha_{diel}$$

*Stripline Conductor Losses require more then 1 line width to determine **dielectric height** and **trace width.***

$$\alpha_{cond} = \frac{36}{wZ_0}\sqrt{f} \qquad Zo = \frac{60}{\sqrt{\varepsilon_r}}\ln\left(\frac{2b+t}{0.8w+t}\right)$$

*Stripline Dielectric Losses only require 1 line length to determine **dielectric loss** and **electrical delay**.*

$$\alpha_{diel} = \frac{\pi}{c_o} f \tan\delta\sqrt{\varepsilon_r}$$

Dielectric loss dominates at high frequencies, conductor losses at low frequencies.

Z_0, characteristic impedance (Ohm)
b, the dielectric height between reference planes (mil)
t, copper thickness of the PCB trace (mil)
w, trace width (mil)
ε_r, dielectric constant
c_o, is the speed of light in vacuum
$\tan\delta$, loss tangent

Causal Dielectric Loss Models

Complex Permittivity

$$\varepsilon_r = \varepsilon_r' - j\varepsilon_r'' = \varepsilon_r'(1 - j\tan\delta)$$

Dielectric Constant

$$\varepsilon'_r$$

Loss Tangent

$$\tan\delta = \left(\frac{\varepsilon_r''}{\varepsilon_r'}\right)$$

Electrical Length L determines Dielectric Constant:

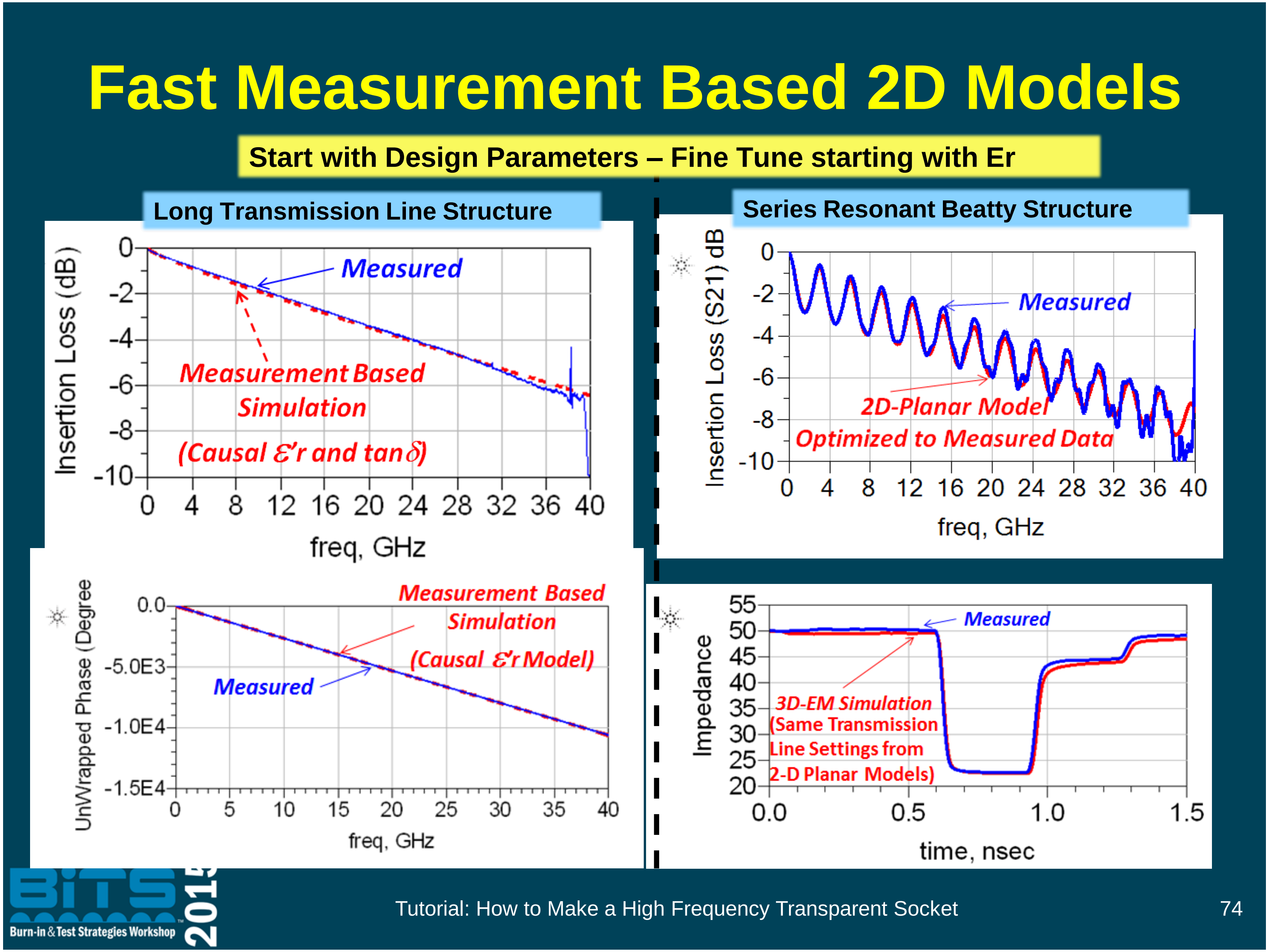
$$\varepsilon_r'(f) = \left(\frac{c_o \times TimeDelay(f)}{L}\right)^2$$

Wide Bandwidth Causal Model for Dielectric Loss – Svensson Djordjevic

$$\varepsilon_r'(f) = \varepsilon'_2 + \frac{\Delta(\varepsilon'_2 - \varepsilon'_1)}{\log(f_2) - \log(f_1)} \times (\log(f_2) - \log(f))$$

Kramers-Kronig Relationship – “To know the real part is to know the imaginary part”

$$\tan\delta = \frac{1}{\varepsilon_r'(f)} \times \frac{\Delta(\varepsilon'_2 - \varepsilon'_1)}{\log(f_2) - \log(f_1)} \times (0.682)$$



Fast Measurement Based 2D Models

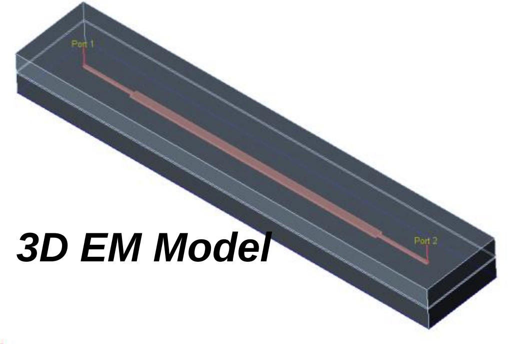
Start with Design Parameters – Fine Tune starting with Er

Long Transmission Line Structure

Series Resonant Beatty Structure

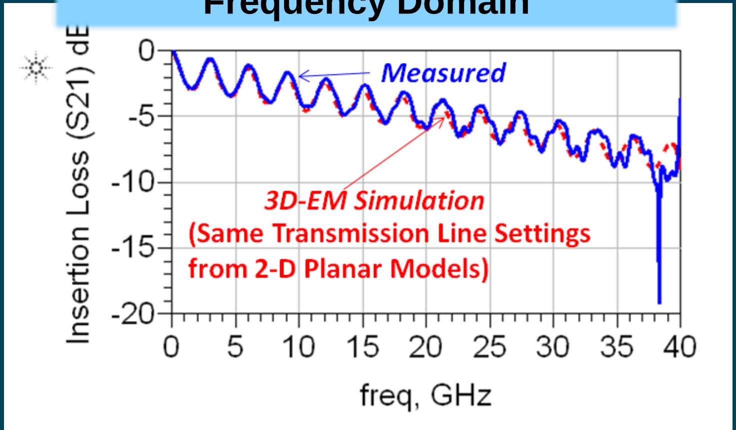
Final Measurement-Based EM Model

Fine Tune EM Model Parameters to Match Measured Data



3D EM Model

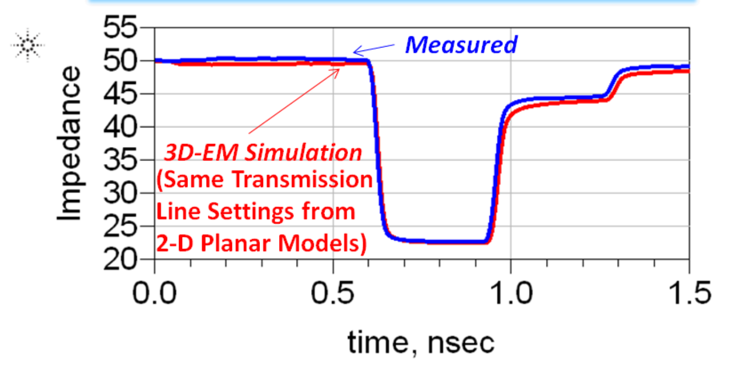
Frequency Domain



Measured

3D-EM Simulation
(Same Transmission Line Settings from 2-D Planar Models)

Time Domain

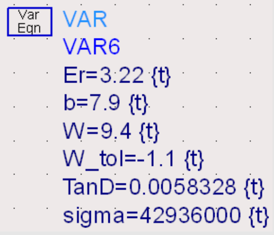


Measured

3D-EM Simulation
(Same Transmission Line Settings from 2-D Planar Models)

Parameters for Tuning

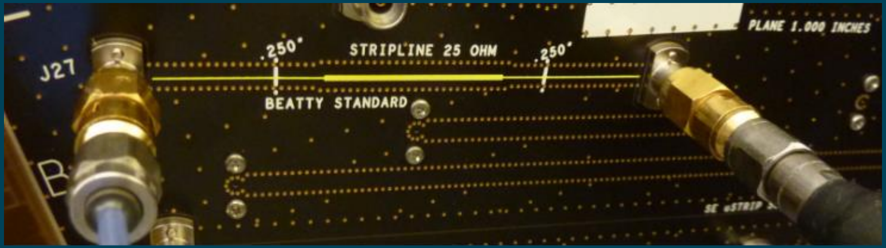
1. Dielectric Constant
2. Loss Tangent
3. Copper Trace Conductivity
4. Dielectric Height
5. Trace Width
6. Etching Tolerance

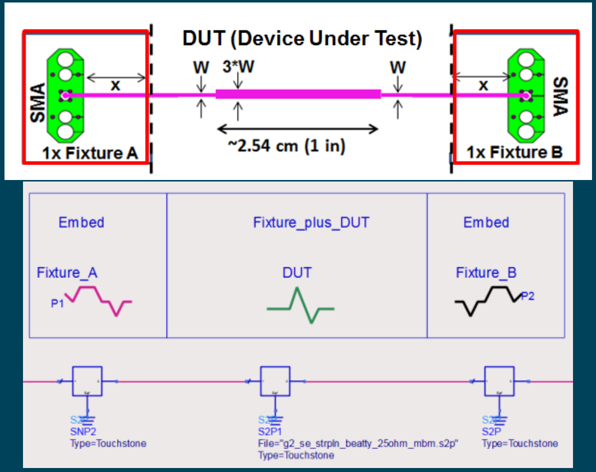


VAR
VAR6
Er=3.22 {t}
b=7.9 {t}
W=9.4 {t}
W_tol=-1.1 {t}
TanD=0.0058328 {t}
sigma=42936000 {t}

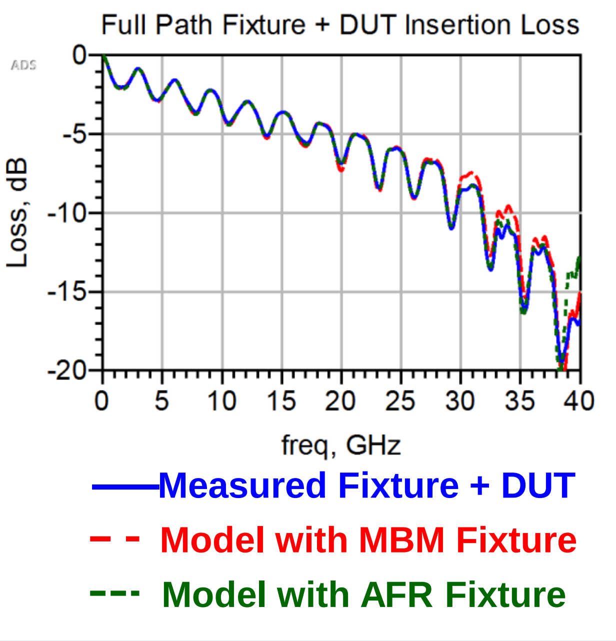
Step 3 – Embed Fixture with Model

$S_{measure}$

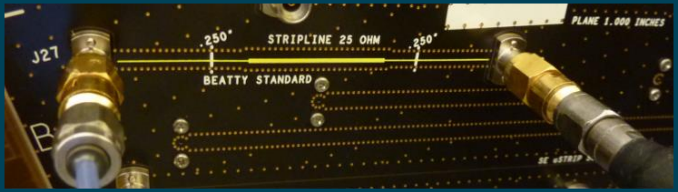




Fixture S-Parameter from AFR and from deconstructed MBM

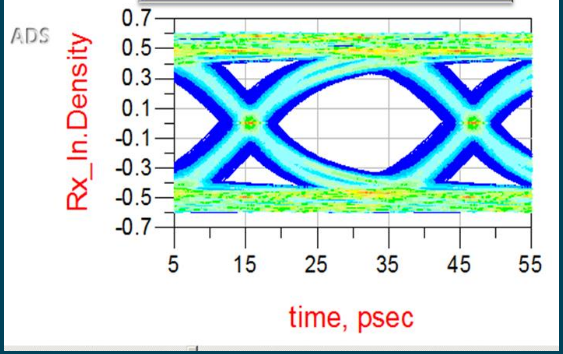


Step 4 – Time Domain Full Path Measure Model Compare

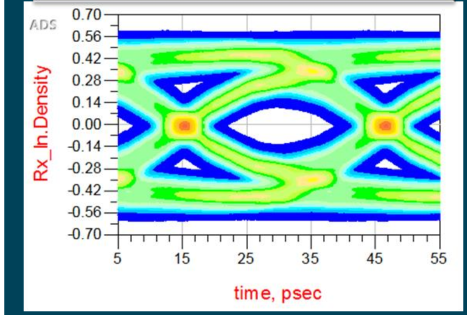


32 Gb/s
PRBS9

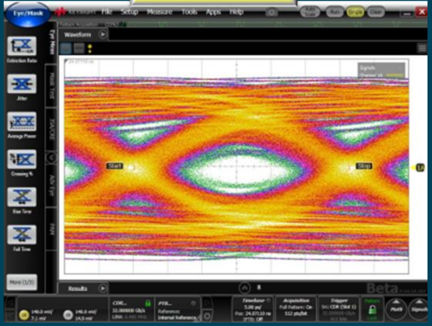
Original Simulation



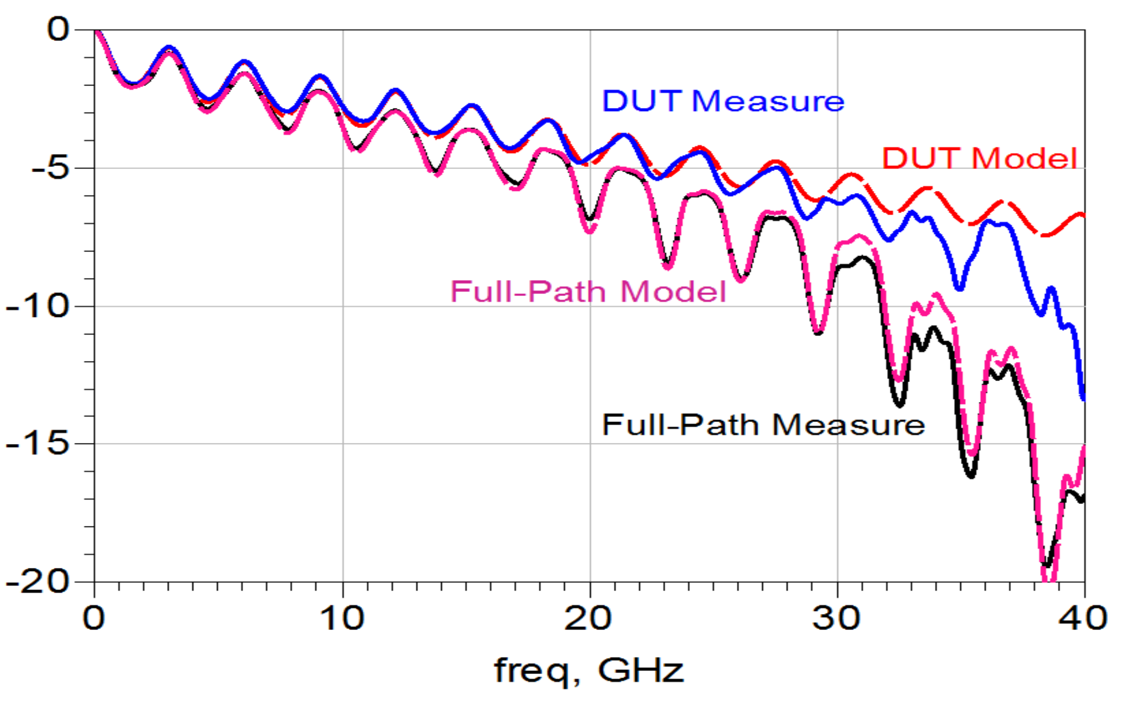
New Simulation with Fixture



Measured



Thank you Mr. Beatty!



Workshop Agenda

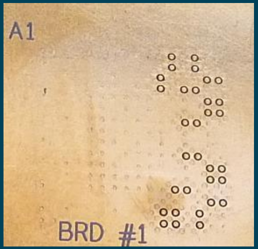
Noon to 1:30 pm	✓ Channel Simulations with Sockets • Signal Integrity Basics
1:30 to 2:45 pm	✓ S-Parameters: • Frequency and Time Domains • Differential Signaling
2:45 to 3:15 pm	Break
3:15 to 4:30 pm	✓ Measurements • Fixture characterization and de-embedding
➡ 4:30 to 6:00 pm	○ Deconstructed Models • Calibrated simulations • The Transparent Socket

Each section includes a ~20 minute Hands-On Lab

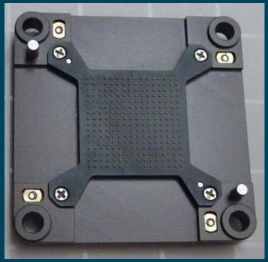
The Full-Path Measurement

Probe
GSG-GSG

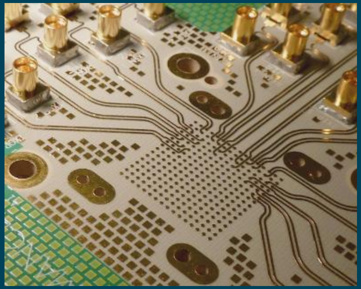
Probe to Socket
Interposer



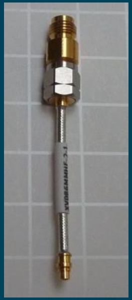
Socket
DUT



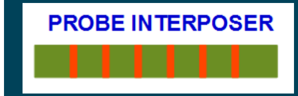
PCB Footprint
to Microstrip

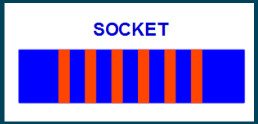


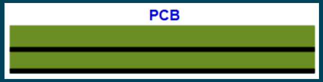
PCB MMPX to
1.85mm Coax

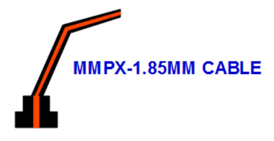


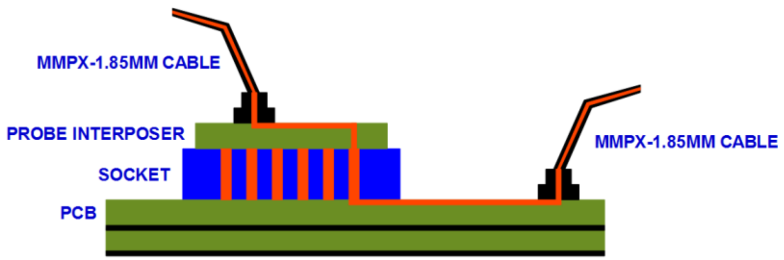
If each component is 50 ohms single ended will it work at 28Gbps?

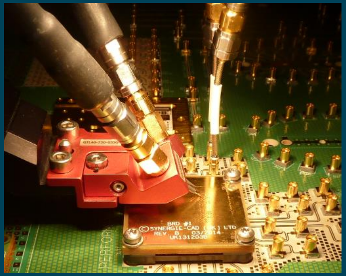




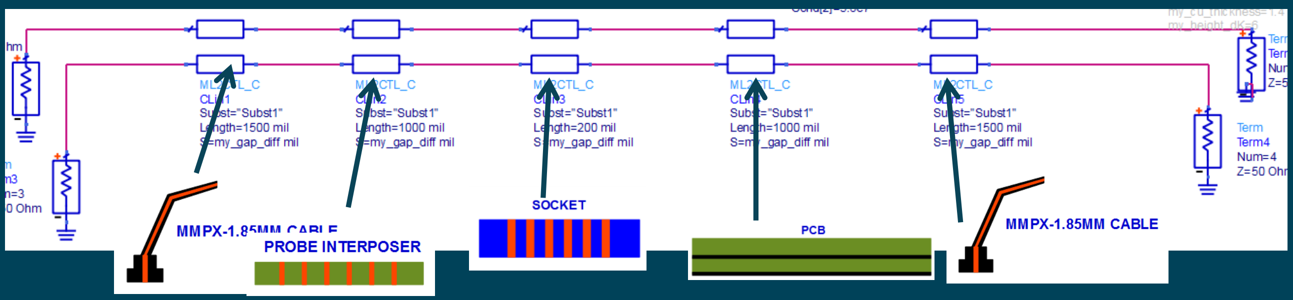






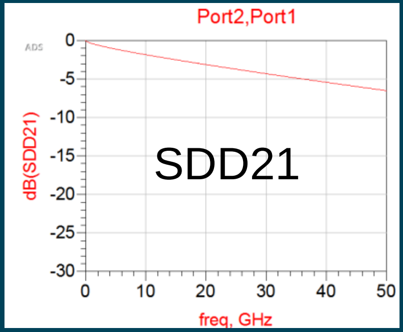


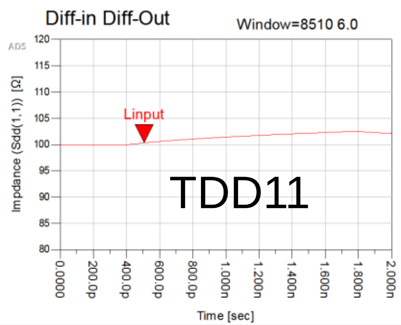
Matched Differential Impedance

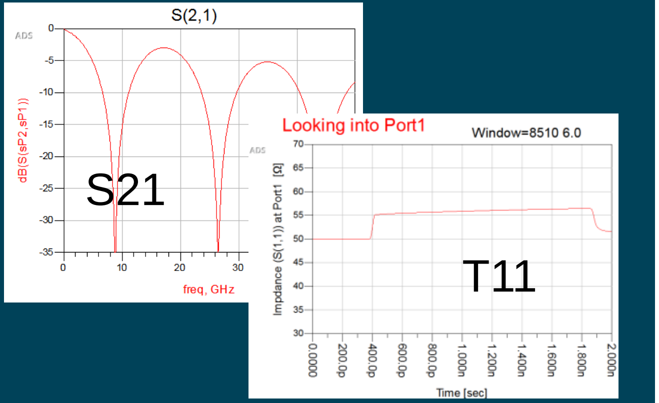


Differential

Single Ended

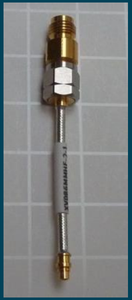




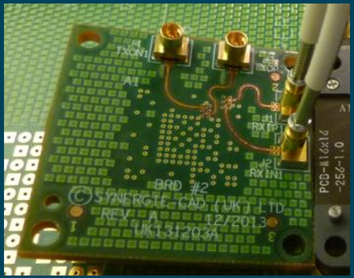


Measured Performance

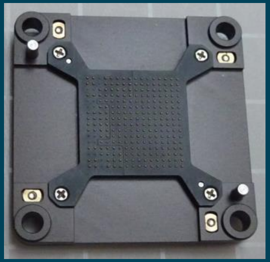
PCB MMPX to 1.85mm Coax



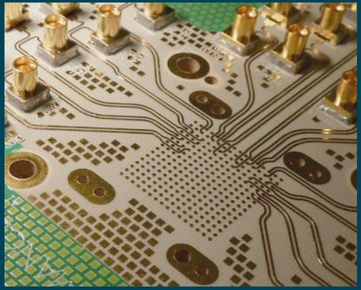
MMPX to Socket Interposer



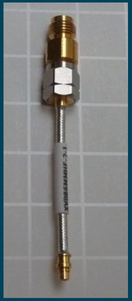
Socket DUT



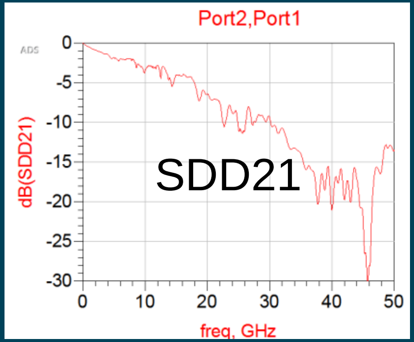
PCB Footprint to Microstrip

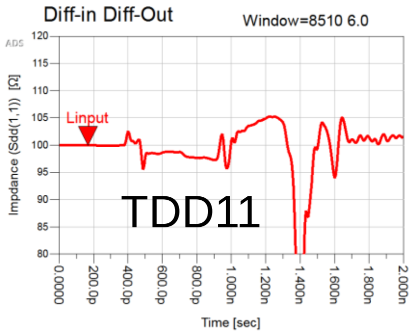


PCB MMPX to 1.85mm Coax

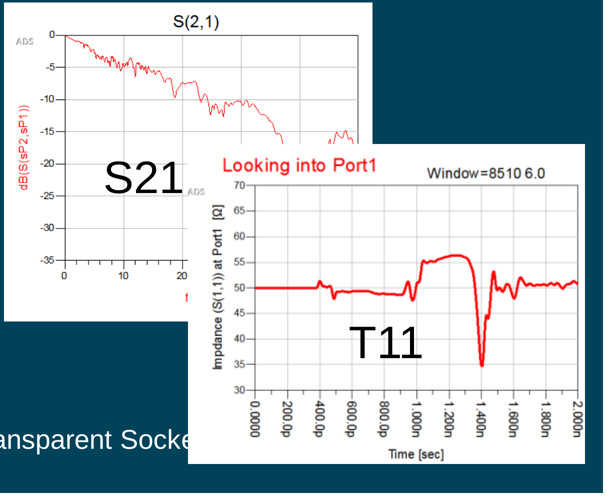


Differential





Single Ended

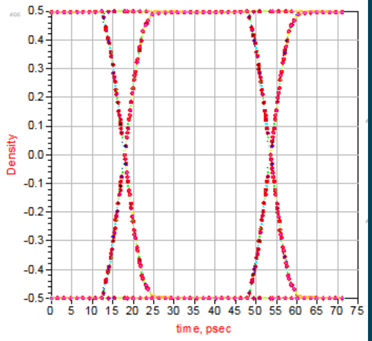


Tutorial: How to Make a High Frequency Transparent Socke

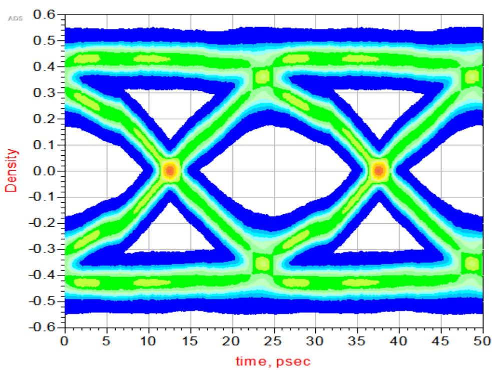
Channel Performance

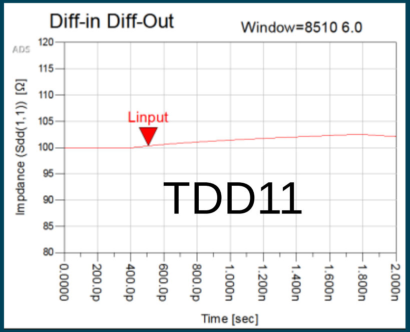
Why isn't the measured path "transparent" to the signal?

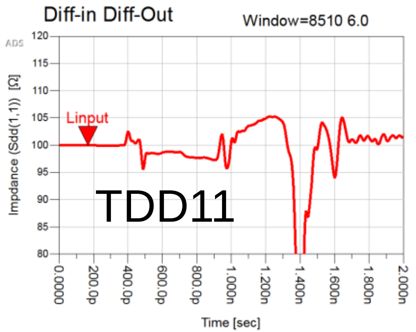
Simulated Channel
Matched Impedance



Measured Channel







A Final Quote

"A theory is something nobody believes, except the person who made it. An experiment is something everybody believes, except the person who made it." — Albert Einstein

"A simulation is something nobody believes, except the person who made it. A measurement is something everybody believes, except the person who made it."
— Paul Huray

Deconstructed Model – Lab#4

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