SIXTEENTH ANNUAL

BiTS

Burn-in & Test Strategies Workshop™

March 15 - 18, 2015

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Archive – Opening Remarks

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Burn-in & Test Strategies Workshop™

March 15 - 18, 2015

Hilton Phoenix / Mesa Hotel
Mesa, Arizona

Welcome

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BiTS 2015

Burn-in & Test Strategies Workshop™

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BiTS Overview

16th Annual

Welcome to the BiTS Workshop!

- Burn-in and Test Strategies Workshop
  - A scope that incorporates next-generation solutions to burn-in and test while also providing vital, current information on traditional technologies

What's NOW & NEXT in Burn-in and Test of Packaged ICs

- The World's Premier Forum For The Latest Information About Burn-in & Test of Packaged IC's
- Extensive & Diverse Technical Program
- The Latest Products & Services at BiTS EXPO
- Many Networking Opportunities

Feedback & Suggestions are Encouraged

Informal and Casual Throughout All Sessions & Activities

Core Values

What's ***Now & Next*** in Burn-in and Test

Premier Event ◆ Cutting Edge ◆ Staying Ahead

Technical Program

BiTS EXPO – 46 Exhibitors

Networking Opportunities

Learn …

Podium Sessions

- 8 Sessions Across 2½ Days; 29 Practical & Useful Presentations

Poster Session

~~• 4~~5 Posters

Renowned Speakers

- Keynote Address
- Distinguished Speaker

Market Reports

- Information about the Test & Socket Markets

BiTS Tutorial

- Learn From An Industry Expert & Build Your Leading Edge Skills

… Explore …

BiTS EXPO

- 46 Companies Are Exhibiting
- Exhibits Area is Open
  - Monday 6:00 – 9:00 pm
  - Tuesday 3:30 – 6:30 pm

… Share

Meet and Chat With Someone You Don't Know!

- Many Opportunities to Network, Share & Discuss Ideas
    - 3 Breakfasts, 2 Lunches, 3 Receptions, 3 Dinners
- Morning and Afternoon Breaks
    - Poster Session During Monday Afternoon
- St. Patrick's Day Social Event
    - Excellent food and drink inspired by the holiday
    - Try your luck in the BiTS Casino!

BiTS Workshop 2015 Schedule

Tutorial Day

Sunday March 15, 2015

Noon	Tutorial – **How to Make a High Frequency Transparent Socket** *Heidi Barnes - Keysight Technologies*	Pueblo Ballroom
6:30 pm	Welcome Reception	Kiva Foyer & Patio
7:30 pm	**Dinner**	Kiva Ballroom
8:30 pm	Distinguished Speaker – **Small Form Factor Package Trends to 2020** *Brandon Prior - Prismark Partners*	Kiva Ballroom
9:30 pm	Adjourn	

Tutorial – Abstract & Biography

Ms. Heidi Barnes is a Senior Application Engineer for High Speed Digital applications in the EEsof EDA Group of Keysight Technologies, a spin-off of Agilent Technologies. Past experience includes over 6 years in signal integrity for ATE test fixtures for Verigy, an Advantest Group, and 6 years in RF/Microwave microcircuit packaging for Agilent Technologies. She rejoined Agilent Technologies in 2012, and holds a Bachelor of Science degree in electrical engineering from the California Institute of Technology.

The ideal transparent socket would make us millions if we could actually find it, but in the real world we cannot simply time travel between two points and ignore what is in the middle. At DC the focus is on the contact resistance, but at the high frequencies of multi-gigabit interconnects one can be plagued by additional dielectric loss, reflections, and complicated multi-mode resonances. This means that if your socket is not working as required at 8, 16, 28 or 40 Gbps then that classic voltmeter sitting on the test bench is not going to do the job. Signal Integrity expert, Dr. Eric Bogatin, emphasizes that a good engineering practice is to always have models or simulations to predict the outcome of a measurement. Often there is a large void between the too simple V=IR calculation and the too complicated full 3D-EM simulation with Maxwell's equations. Engineers confronted with these two options will typically do nothing on the simulation side and then just point to the data sheet.

A better option is to explore the power of simple transmission line theory and network analysis with scattering parameters (S-Parameters). Simple deconstructed transmission line models can be used in simulations to quickly evaluate the impact of resistance, dielectric loss, reflections, and even resonances. The results of the simulations provide valuable insights into how transparent a socket is for your application. Using hands-on computer labs with both frequency domain and time domain simulations attendees at the workshop will be able to test out their ability to debug a failed test socket measurement and get a socket design that is transparent for an 8.4 Gbps PCIe application example. These simple deconstructed transmission line models also improve the effectiveness of full 3D-EM simulations. Knowing what to expect from the EM simulation insures better setup of the stimulus ports, and effective use of simplification trade-offs.

Another way to make a transparent socket is to mathematically remove its effects from the measurement. This can be a simple calibration of removing a static IR drop at DC, but at high frequencies one must calibrate out both the “attenuation” drop and the interaction of reflected signals. To make things even more complicated, one must also keep track of the phase relationship between the current and voltages at high frequencies. Simple transmission line theory and network analysis scattering parameters (S-parameters) do just that, and with a bit of matrix math they can remove the effects of the socket fixture from a measurement. The signal integrity world calls this fixture de-embedding. Using hands-on computer labs and actual test equipment hardware attendees will learn how to measure socket fixture S-parameters using a two-tier Short/Open/Load/Through (SOLT) with 2-port probing or 1-port open calibration techniques. The socket fixture S-parameters can then be used in the time domain to remove the effects of the socket fixture from the measurement making the socket transparent. This sounds too good to be true, and so again one can turn to simulation to see where it can go wrong and get a practical understanding of how and when to implement fixture de-embedding.

The goal of this half-day tutorial is to give the attendees a toolbox of both simulation and measurement signal integrity techniques for characterizing a socket and ways to make it transparent for high frequency multi-gigabit applications.

Distinguished Speaker – Abstract & Biography

Mr. Brandon Prior is a Senior Consultant at Prismark Partners. He joined Prismark in 1996 and is the author of their Semiconductor and Packaging Report.In his role at Prismark, he provides market and competitive analyses within semiconductor packaging and interconnects.

Mr. Prior will share an overview of the global packaging market. His presentation will focus on the impact and growth of small form factor packages such as multi-row QFN, WLCSP, Fan-Out WLCSP and MIS BGA on the electronics industry infrastructure. Teardowns of products from early adopters such as Apple, Samsung, Huawei, and Xiaomi will be used to highlight how fast this change is occurring.

BiTS Workshop 2015 Schedule

Frontiers Day

Monday March 16, 2015

8:00 am	Opening Remarks – **Ira Feldman** *General Chair*	Kiva Ballroom
9:00 am	Keynote Address – **Making Sense of the Internet of Tomorrow** *Joe Bruen - Freescale Semiconductor*	Kiva Ballroom
10:00 am	Break & Networking	Kiva Foyer & Patio
10:30 am	Session 1 – **Putting MEMS to the Test** *Testing MEMS Devices*	Kiva Ballroom
12:30 pm	Lunch	Kiva Foyer & Patio

BiTS Workshop 2015 Schedule

Frontiers Day

Monday March 16, 2015

1:30 pm	Session 2 – **Spanning the Socket Rainbow** *Test Socket Applications*	Kiva Ballroom
3:30 pm	Poster Session	Kiva Ballroom
4:30 pm	Session 3 – **Wafer Level Pots of Gold** *Wafer Level Chip Scale Packaging (WLCSP)*	Kiva Ballroom
6:00 pm	**BiTS EXPO & Reception**	Atrium
9:00 pm	Adjourn	

Technical Program

Title
Tutorial **How to Make a High Frequency Transparent Socket** Heidi Barnes, Keysight Technologies
Distinguished Speaker **Small Form Factor Package Trends to 2020** Brandon Prior, Prismark Partners
Opening Remarks Ira Feldman, General Chair
Keynote Address **Making Sense of the Internet of Tomorrow** Joe Bruen, Freescale Semiconductor
Closing & Awards Ira Feldman, General Chair

Session	Title
1	**Putting MEMS to the Test** *Testing MEMS Devices*
2	**Spanning the Socket Rainbow** *Test Socket Applications*
3	**Wafer Level Pots of Gold** *Wafer Level Chip Scale Packaging (WLCSP)*
4	**Material Magic** *Materials and Fabrication Processes*
5	**Handle With Care** *Test Cell Integration*
6	**Lord of the Dance** *Simulation & Performance*
7	**All That Glitters Is Or Is Not Gold & Do You Believe in Leprechauns?** *Contact Technology & Marketplace*
8	**Looking For That Four Leaf Clover** *Test Cell Integration*
Poster	**Poster Session**

BiTS Awards

- Best Presentation
- Best Poster
- Best Data Presented
- Most Inspirational Presentation
- Best Presentation, Tutorial in Nature
- Attendee Choice

… and …

BiTS "Special" Award

For the Least Concealed Sales Pitch

(Almost)
Brilliant
Disguise

"Semi-retired" but always available…

bitsworkshop.org

Your Complete Source For Information About BiTS

Current Workshop

- Call For Papers
- EXPO & Sponsorships
- Advance/Final Program
- Registration Information & Forms; Register On-line
- Author Information
- Hotel Information/Travel

Features

- Committee Members
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- Archive of past BiTS
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Plus Premium Archive…

BiTS Premium Archive

- Multimedia
    - Audio with synchronized slides & pointer
    - BiTS 2013 & BiTS 2014
    - BiTS 2015 posted shortly after BiTS
- Additional content
    - Tutorials
- Subscription Model
    - BiTS 2015 Professional Attendees – Subscription for One Year
    - Subscriber – Nominal Fee
        - Applied to BiTS 2016 Registration

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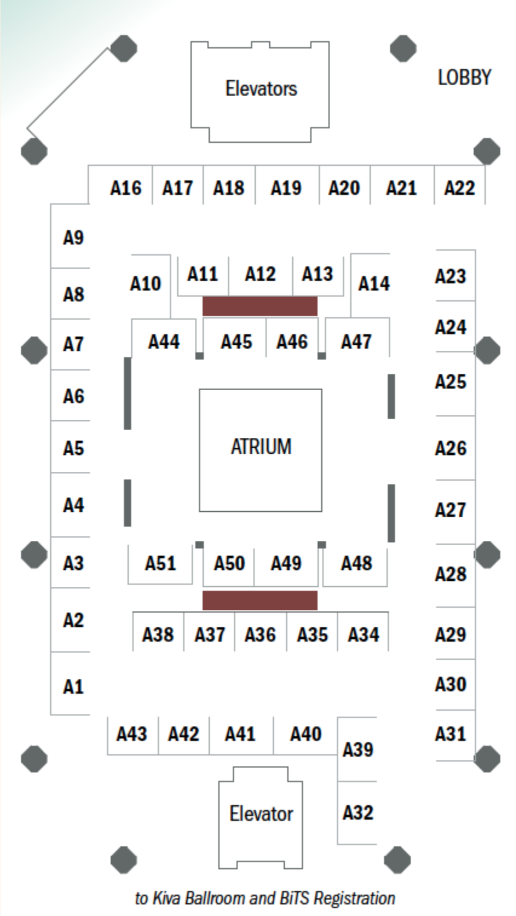
BiTS EXPO



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Casino Night

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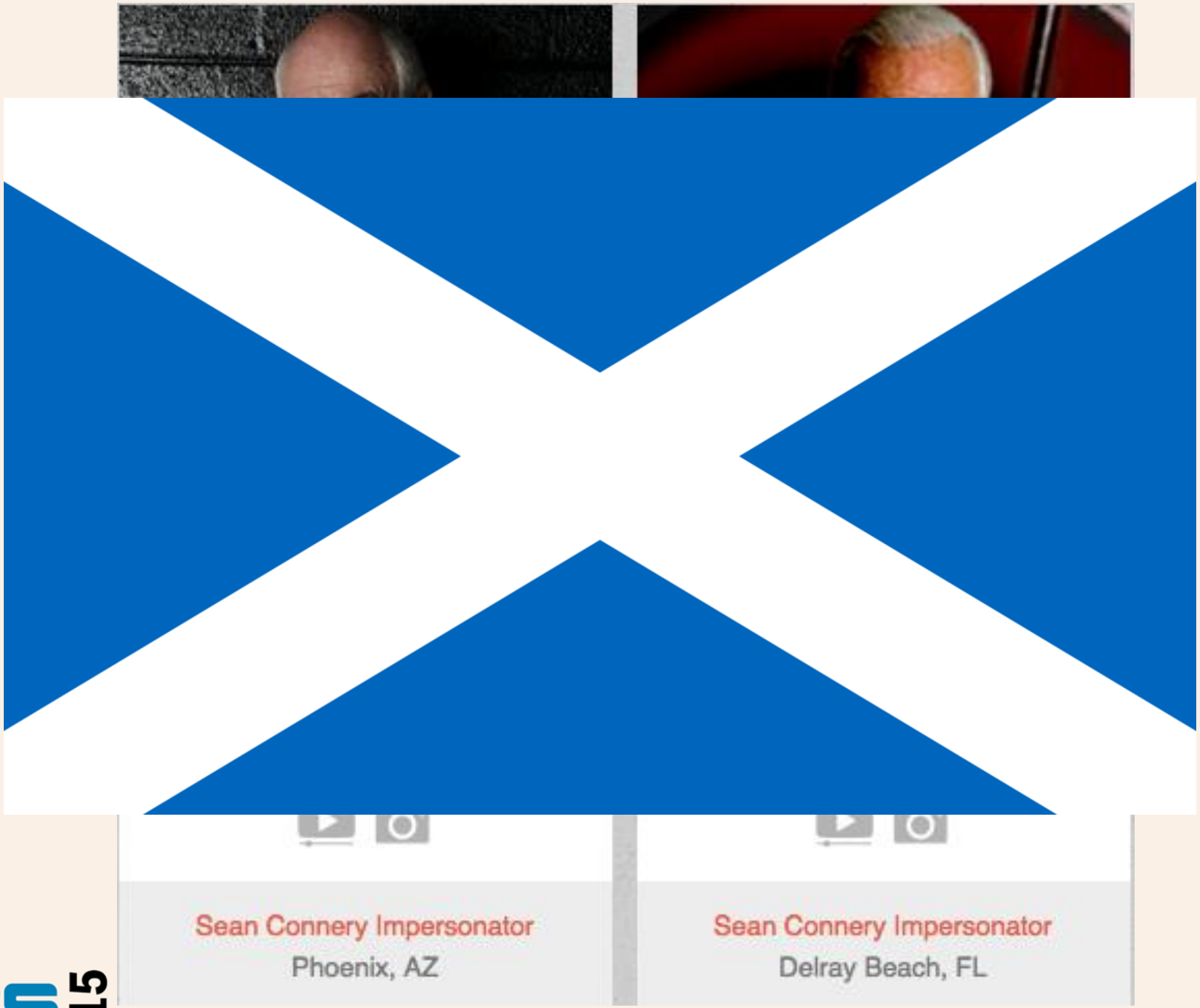

Sean Connery Impersonator
Phoenix, AZ

Sean Connery Impersonator
Delray Beach, FL

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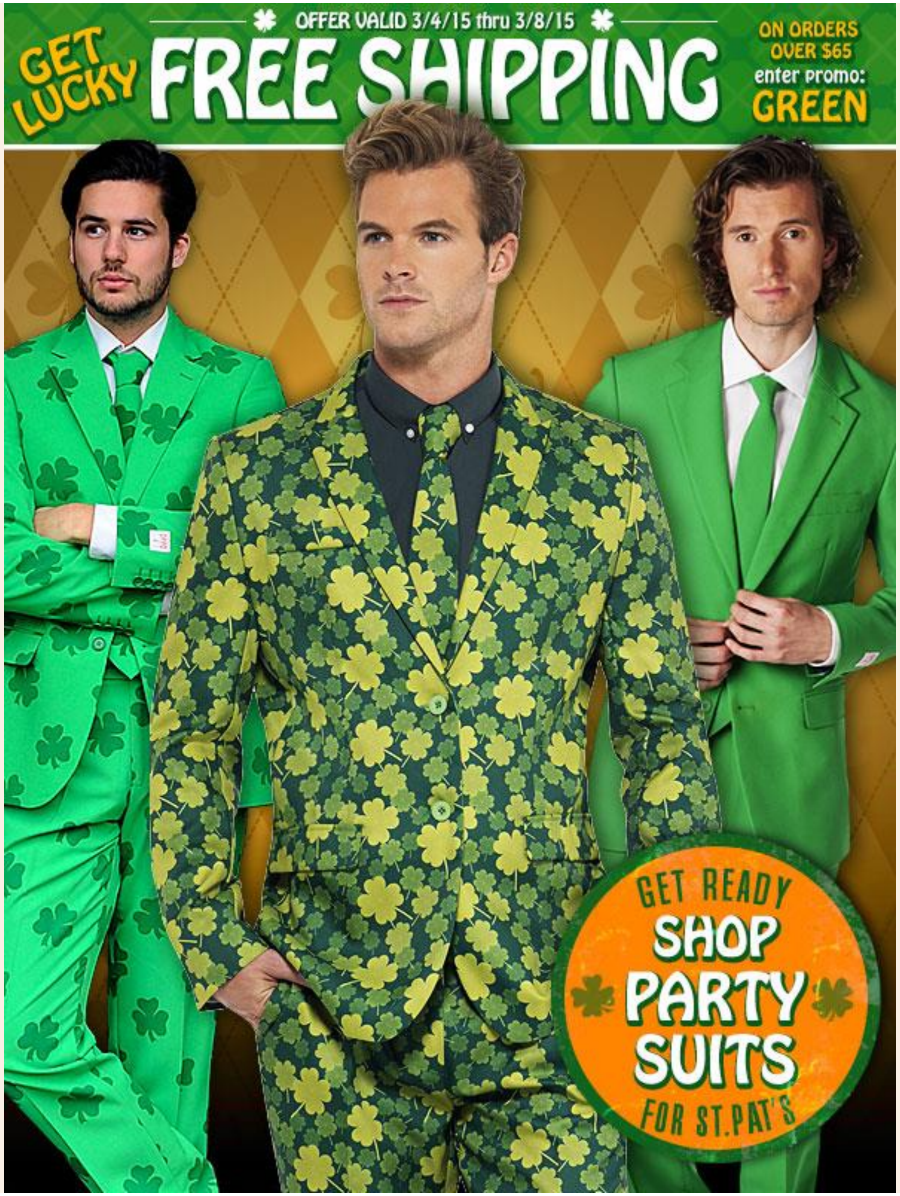

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Schedule At A Glance

SUNDAY *March 15*	MONDAY *March 16*	TIME	TUESDAY *March 17*	WEDNESDAY *March 18*
SCHEDULE	Continental Breakfast Registration Desk Open	7 00	Continental Breakfast Registration Desk Open	Continental Breakfast Registration Desk Open
		7 30		
		8 00	**SESSION 4** **Materials & Fabrication Processes**	**SESSION 7** **Contact Technology & Marketplace**
	Opening Remarks	8 30		
	KEYNOTE ADDRESS Dr. Babak Taheri	9 00		
		9 30		
	Break & Networking	10 00	Break & Networking	Break & Networking
Registration Desk Open	**SESSION 1** **Testing MEMS Devices**	10 30	**SESSION 5** **Test Cell Integration**	**SESSION 8** **Test Cell Integration**
		11 00		
TUTORIAL Pt. 1 **Signal Integrity Basics** Ms. Heidi Barnes		11 30		
		12 00		Awards & Closing Remarks
	Lunch	12 30	Lunch	*Adjourn Workshop*
		1 00		Visit the BiTS website for program details and descriptions. BITSWORKSHOP.ORG BiTS WORKSHOP
	SESSION 2 **Test Socket Applications**	1 30	**SESSION 6** **Simulation & Modeling**	
		2 00		
		2 30		
Break & Networking		3 00		
TUTORIAL Pt. 2 **Measurement Techniques** Ms. Heidi Barnes	**POSTER SESSION** Break & Networking	3 30	BiTS EXPO	
		4 00		
	SESSION 3 **WLCSP**	4 30		
		5 00		
		5 30		
Welcome Reception	BiTS EXPO	6 00		
		6 30	**SOCIAL EVENT** **Celebrate St. Patrick's Day!** Music, Food, Beverages & Games	
		7 00		
Dinner		7 30		
		8 00		
DISTINGUISHED SPEAKER Mr. Brandon Prior		8 30		
	Adjourn for the day	9 00		
Adjourn for the day		9 30	*Adjourn for the day*	

Shanghai

Coming soon!
Late October 2015

BiTS 2016

March 6 – 9 , 2016

Hilton Phoenix / Mesa Hotel

Exterior Renovations – New Paint, Lighting & Design

Guest Room Renovation – New Bedroom plus remodeled bathrooms

Call for BiTS 2016

March 6-9, 2016 ◆ Mesa, Arizona

Presentations ◆ Posters ◆ Tutorial

Share your latest work and advancements as an **AUTHOR**! Your presentation or poster will be part of a stimulating and comprehensive program. Explore a demanding topic as a **TUTORIAL INSTRUCTOR**. Share your expertise with participants eager to build their leading edge skills. Presentation, Poster & Tutorial proposals addressing a broad range of burn-in and test subjects are welcome, including, but not limited to:

- Socketing/Contacting of Contemporary and Advanced Packaging Technologies
- PCBs, Materials, Handlers, Contact
- Technologies, Burn-in Tooling
- Modeling, Characterization & Analysis
- Process & Operational Challenges
- WLCSP Test for KGD or Final Test
- MEMS and Non-Electrical Stimuli Test

BiTS EXPO 2016 & Sponsors

The EVENT for exhibiting your company's products & services. Showcase and promote what is ***Now & Next!***

Don't miss out! See the registration desk to sign up now at the early-bird discount rate. **BiTS EXPO** is sure to sell out!

For more information about BiTS 2016
please contact the BITS Office
bitsinfo@bitsworkshop.org

Have the LAST WORD!

Overall Workshop Evaluation

	Excellent	Good	Fair	Poor
Technical Program	☐	☐	☐	☐
Exhibits	☐	☐	☐	☐
Facilities	☐	☐	☐	☐
Meals/Social Activities	☐	☐	☐	☐
Registration Process	☐	☐	☐	☐
Overall Evaluation	☐	☐	☐	☐

	Yes	No
Do You Want to Attend BiTS 2016?	☐	☐

Tell Us!

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