
SIXTEENTH ANNUAL
BiTS
Burn-in & Test Strategies Workshop
March 15 - 18, 2015
Hilton Phoenix / Mesa Hotel
Mesa, Arizona
Archive – Distinguished Speaker
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Distinguished Speaker

BiTS Workshop 2015 Schedule

Tutorial Day

Sunday March 15 8:30 pm

Small Form Factor Package Trends to 2020

Brandon Prior

Senior Consultant

Prismark Partners

Distinguished Speaker – Abstract & Biography

Mr. Brandon Prior is a Senior Consultant at Prismark Partners. He joined Prismark in 1996 and is the author of their Semiconductor and Packaging Report.In his role at Prismark, he provides market and competitive analyses within semiconductor packaging and interconnects.

Mr. Prior will share an overview of the global packaging market. His presentation will focus on the impact and growth of small form factor packages such as multi-row QFN, WLCSP, Fan-Out WLCSP and MIS BGA on the electronics industry infrastructure. Teardowns of products from early adopters such as Apple, Samsung, Huawei, and Xiaomi will be used to highlight how fast this change is occurring.

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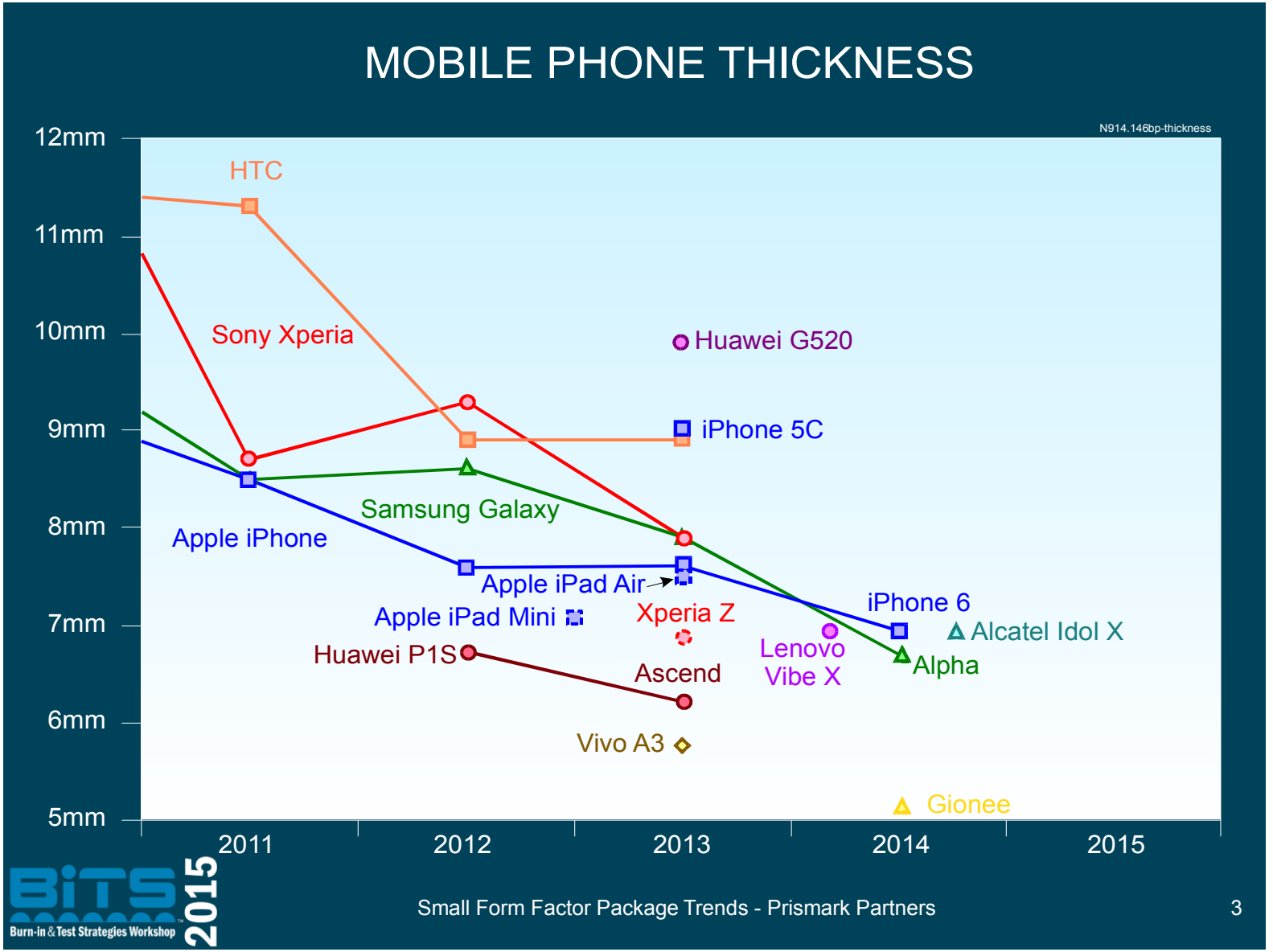
SMALL FORM FACTOR PACKAGE TRENDS TO 2020

Brandon Prior
Prismark Partners LLC

2015 BiTS Workshop
March 15 - 18, 2015

SMALLER, THINNER AND INCREASED FUNCTIONALITY

- These three requirements have not changed
  - Quality, reliability and low cost are givens
- Smaller
  - Sub-0.4mm pitch gaining traction
  - WLCSP becoming mainstream
- Thinner
  - Wafer Level CSP and QFN are already thin
  - Phone/Tablet OEMs asking for package heights down to 0.25mm
- Increased functionality comes in many forms:
  - SiP: MCP, stacked die, 3D TSV, PoP, passive integration
  - Increased I/O and routing capability: wide I/O, silicon interposer


MOBILE PHONE THICKNESS
N914.146bp-thickness
12mm
11mm
10mm
9mm
8mm
7mm
6mm
5mm
2011
2012
2013
2014
2015
HTC
Sony Xperia
Huawei G520
iPhone 5C
Samsung Galaxy
Apple iPhone
Apple iPad Air
Apple iPad Mini
Xperia Z
iPhone 6
Alcatel Idol X
Lenovo Vibe X
Alpha
Huawei P1S
Ascend
Vivo A3
Gionee
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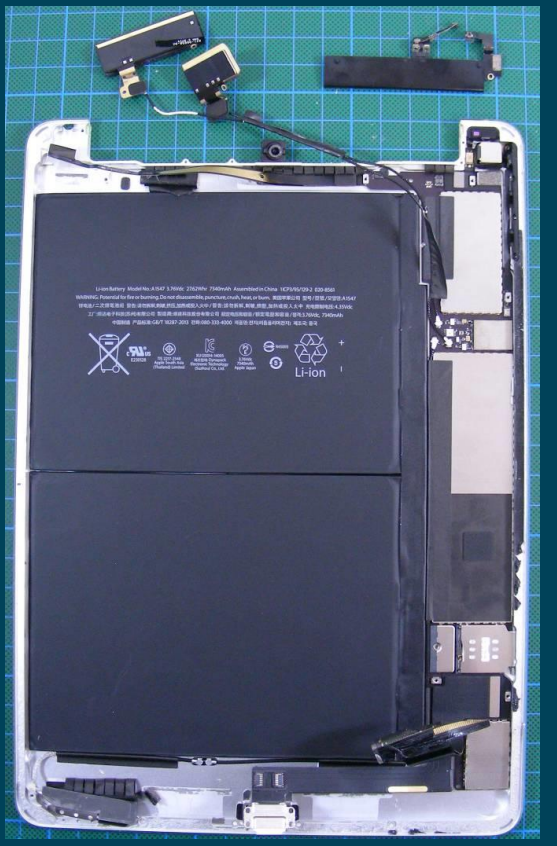
Small Form Factor Package Trends - Prismark Partners
3

1114.10/360.bp

APPLE iPad AIR 2 (1)

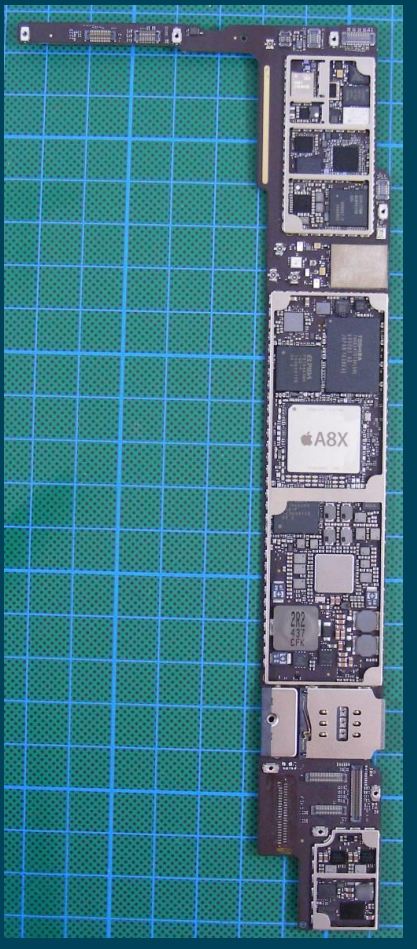
- Overall construction and feature sets remain similar to smartphones
  - "L-shape" PCB off to side of battery
  - Extremely thin: total board assembly <2mm, total system 6.1mm
  - No active thermal management
- PCB/SMT technology more conservative than iPhone lineup
  - 0.4mm pitch, but with more spacing between the forty semiconductor components
  - EMI shields on top of PCB, but require spacers between some packages
  - PCB is 65cm^2 ten layer any-layer, but with relaxed L/S versus iPhone



1114.10/360.bp

APPLE iPad AIR 2 (2)

- Package technology nearly same as iPhone 6
  - Over fifteen WLCSP including power management, transceiver, audio, WLAN, etc
  - No PoP but lidded A8X and power manager
  - EMI shielded packages for Murata, Skyworks, TriQuint
- Package and SMT still beyond most low cost tablet and notebooks
  - Ten layer HDI at 60µm L/S compared to 2-6-2 at 75µm L/S
  - 0.4mm pitch for all components except memory
- 128GB NAND at 11 x 14 x 1mm versus SSD card at 50 x 30 x 4mm



APPLE iPhone 6 PLUS MAIN BOARD (Side A)

1114.4/411bp

1. NXP LPC18B1 ARM Cortex-M3 Microcontroller – aka M8 (WLCSP)
2. SK Hynix 128Gb (16GB) NAND Flash (WB CSP) – Package EMI
3. USI WiFi/Bluetooth Module (LGA with WLCSP) – Package EMI
4. Qualcomm WTR1625L RF Transceiver (WLCSP)
5. Qualcomm WFR1620 RF Receiver (WLCSP)
6. Qualcomm PM8019 Power Management IC (WLCSP)
7. Apple/Dialog 338S1251 Power Management IC (FC CSP w/IPD?)
8. Broadcom BCM5976 Touch Controller (WLCSP)
9. Texas Instruments 343S0694 Touch Controller (WLCSP)
10. NXP 65V10 NFC controller (WB CSP)
11. AMS AS3923 NFC Booster IC (WLCSP)
12. Apple/Cirrus Logic 338S1201 Audio Codec (WLCSP)
13. Apple/Cirrus 338S1202 Audio Amplifier (WLCSP)
14. Skyworks (GPS Front End?) – Package EMI

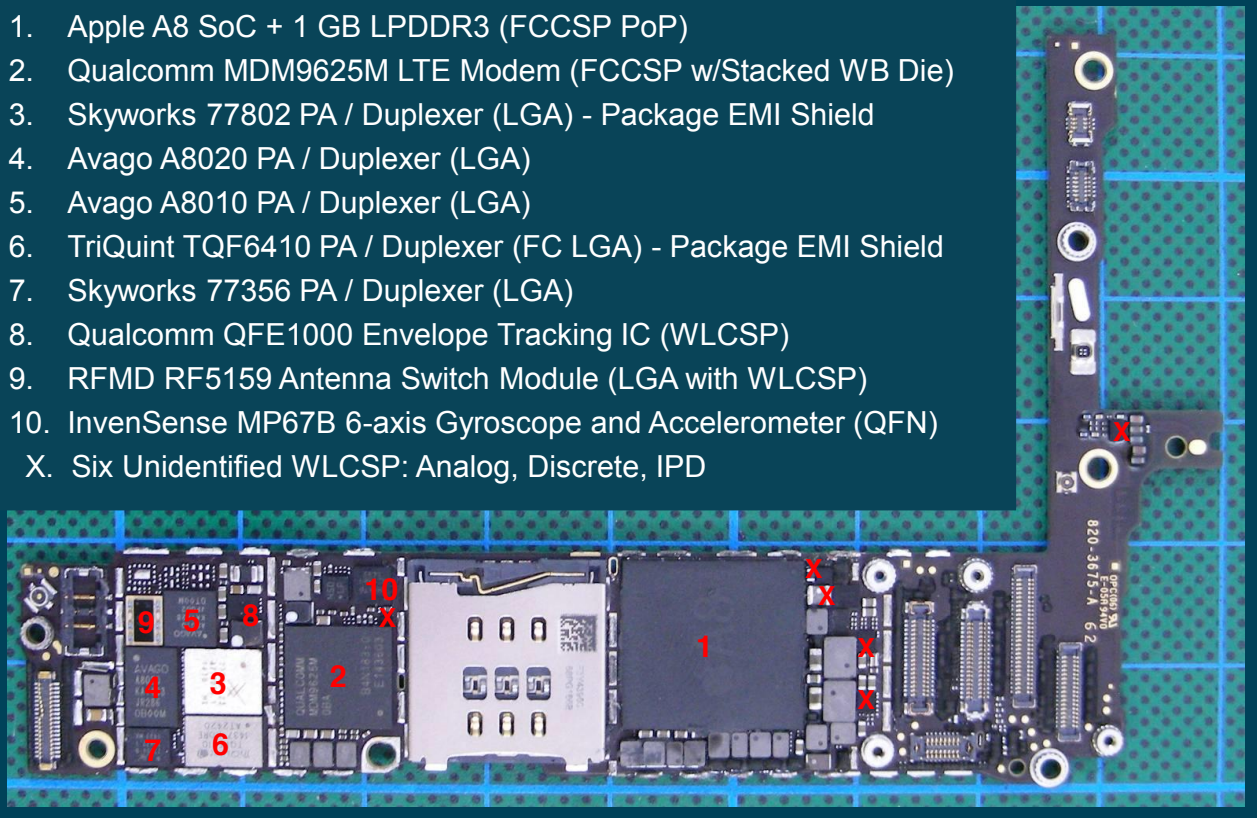
X. Eight unidentified WLCSP: Analog, EEPROM, Discrete

APPLE iPhone 6 PLUS MAIN BOARD (Side B)

1114.4/411bp

1. Apple A8 SoC + 1 GB LPDDR3 (FCCSP PoP)
2. Qualcomm MDM9625M LTE Modem (FCCSP w/Stacked WB Die)
3. Skyworks 77802 PA / Duplexer (LGA) - Package EMI Shield
4. Avago A8020 PA / Duplexer (LGA)
5. Avago A8010 PA / Duplexer (LGA)
6. TriQuint TQF6410 PA / Duplexer (FC LGA) - Package EMI Shield
7. Skyworks 77356 PA / Duplexer (LGA)
8. Qualcomm QFE1000 Envelope Tracking IC (WLCSP)
9. RFMD RF5159 Antenna Switch Module (LGA with WLCSP)
10. InvenSense MP67B 6-axis Gyroscope and Accelerometer (QFN)

X. Six Unidentified WLCSP: Analog, Discrete, IPD



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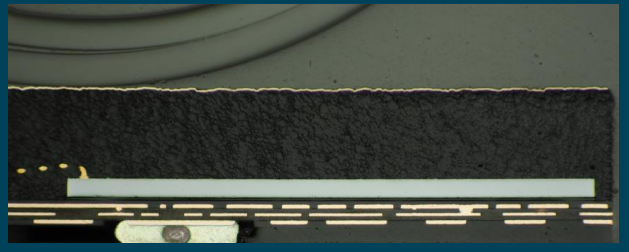
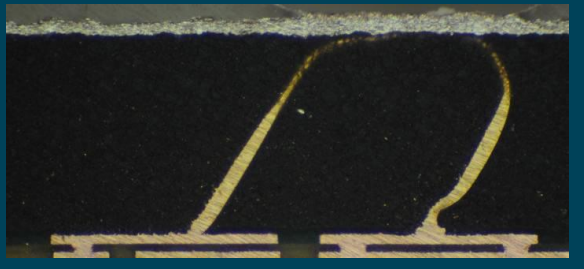
PACKAGE LEVEL EMI SHIELDING IN iPHONE 6 PLUS

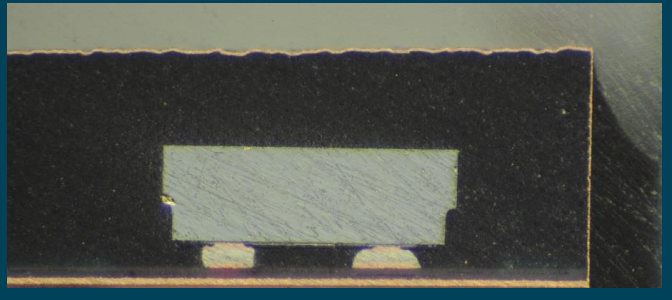
- SK Hynix NAND
  - 14µm Cu using PVD
  - Top and edge of package



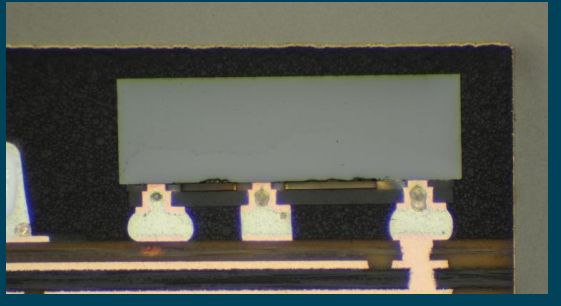
- Skyworks PA module
  - Ag paste is 50µm thick
  - Wire bonds around package edge



- USI WLAN module
  - 14µm Cu thickness
  - Top and edge of package



- Triquint PA module
  - 5µm metal thickness
  - Cu, Ni, Cr, PVD

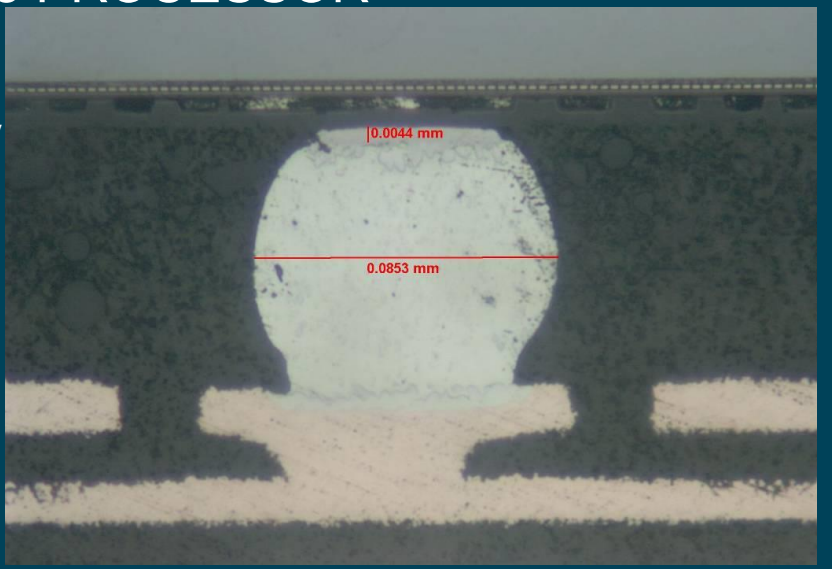


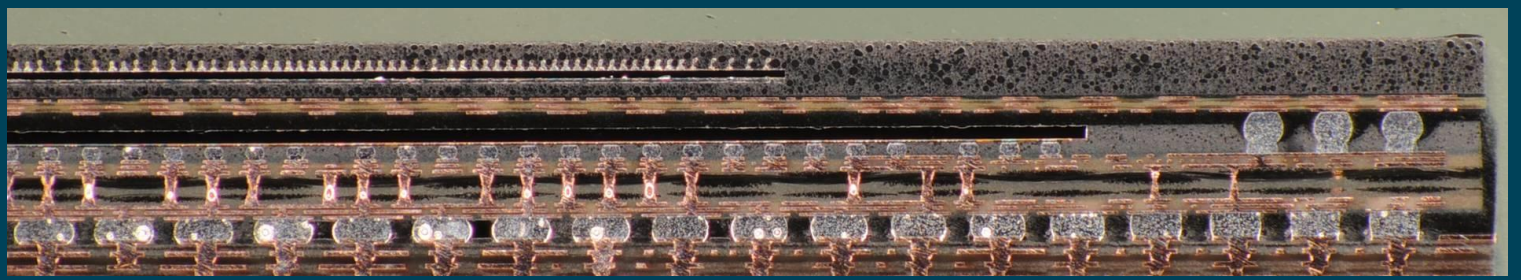
Photos source: Prismark/Binghamton University

1014.6/193bp

APPLE A8 PROCESSOR

- 14.5 x 12.7 x 1.0mm PoP
  - 1,155 balls @ 0.4mm pitch
  - 426 balls @ 0.35mm pitch for top memory
  - Two stacked LPDDR3 die using Ag wire
- 8.5 x 10.5mm die
  - 85µm thick
  - SnAg bumps @150µm pitch
  - 70µm bump height
  - Molded underfill
- 2-2-2 ABF substrate
  - 190µm core, 315µm total thickness
  - 65µm microvias, 80µm LTH





Photos source: Prismark/Binghamton University

0115.3/023bp

LENOVO YOGA 3 PRO PCB

- Double-sided Assembly
  - Mostly passives, discretes, and connectors on back side
  - 01005 passives, one WLCSP
  - Intel CPU has 1,234 balls at 0.5mm pitch
  - 67cm^2
- Fourteen-Layer Construction
  - 940µm thick
  - 100µm via diameter
  - 75µm L/S
  - 25 – 35µm copper thickness
  - 35 – 50µm dielectric thickness

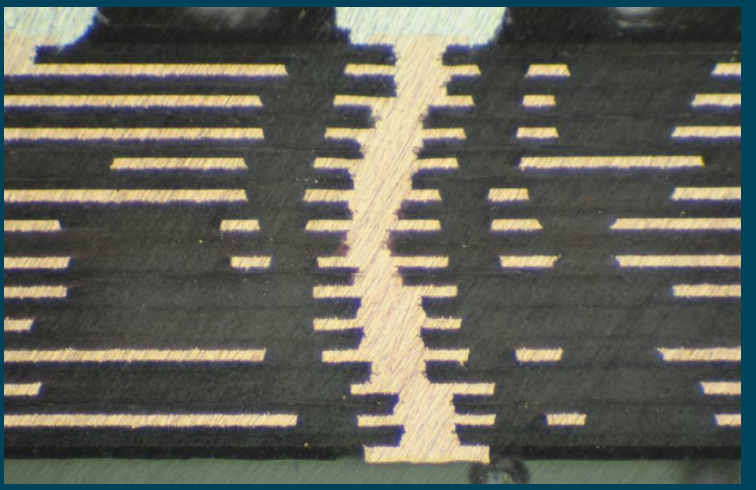
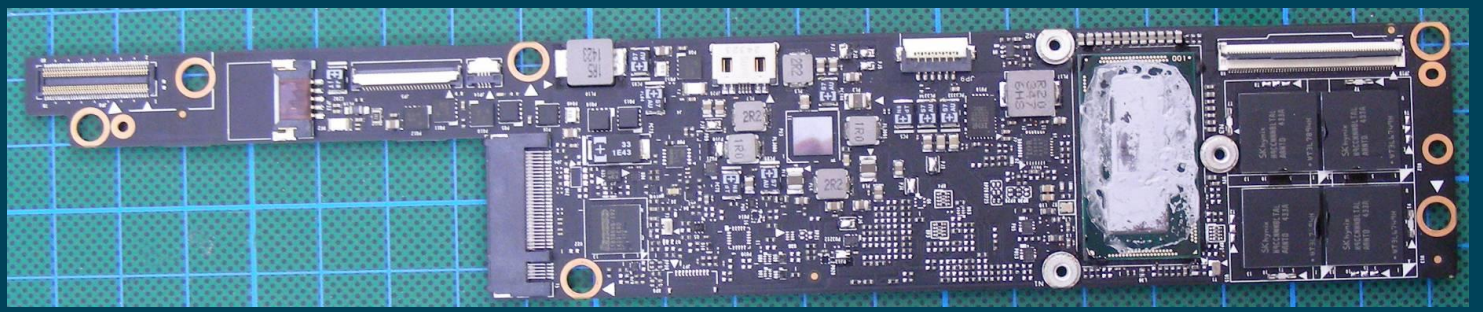


Photo source: Prismark/Binghamton University



514.6/193bp

APPLICATION PROCESSOR TRENDS: SAMSUNG

- Currently uses single die lidded FCCSP for Chromebook and similar, and top PoP with 0.35mm and 450 balls for smartphone
  - Expects to keep this structure for a few years; technology, supply chain, and processing capability/capacity are well developed.
  - Top PoP ball count to increase to 500 or more to support LPDDR4 and pitch reduction
  - Top PoP pitch will be reduced to 0.3mm
- Will continue to use embedded passives for high-end processor
- Working on two-layer substrates for low cost devices
- Main advantage of FO-WLP is thickness reduction.
  - TSV only for low volume HMC, not for mobile products anytime soon

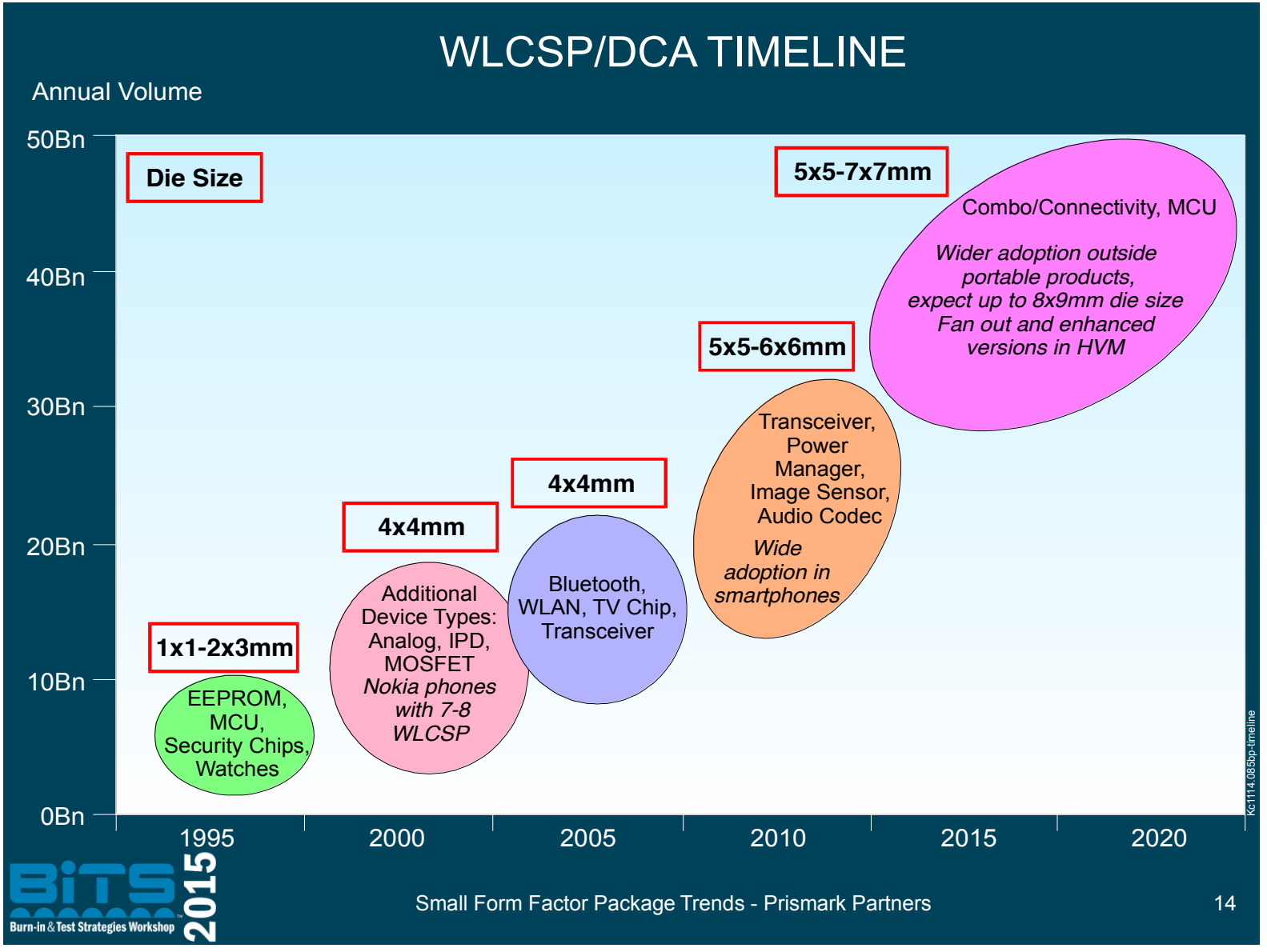
1014.6/193bp

APPLICATION PROCESSOR TRENDS: MediaTek

- MediaTek is shipping >30M/month of application processors; >35% use FCCSP
  - All FCCSP to date use Cu pillar with SnAg cap and mass reflow/bump on trace with two-layer substrate
  - Molded underfill in all products to date
- MT 6595 AP/baseband released in October 2014 is a PoP
  - 1-2-1 substrate with embedded passive
  - Assembly by SPIL/ASE
- Looking into fan-out WLCSP, including TSMC and SPIL versions
  - Main driver is increasing to >500 balls on top PoP interface
  - Also offers reduced height and ability to include multiple die side-by-side

"NEW" PACKAGES CURRENTLY IN THE SPOTLIGHT

- Fan Out Wafer Level CSP (FO-WLCSP or FO-WLP).
  - Production started in 2009/2010, but lost momentum through 2014
  - Renewed interest at mobile players and manufacturing partners
  - TSMC is most aggressive to serve customers, including Apple
- Molded Interconnect Substrate (MIS or MIS BGA)
  - Alternative to QFN and BGA/CSP, perceived as lower cost
  - Uses EMC as dielectric (as with QFN) but manufactured like BGA/CSP substrate to allow advanced routing
- 3D TSV, Silicon Interposer, and Alternatives
  - 3D TSV finally getting into HVM for DRAM
  - Many companies developing lower cost alternatives with never ending acronyms: EMIB, SLIT….


WLCSP/DCA TIMELINE
Annual Volume
50Bn
40Bn
30Bn
20Bn
10Bn
0Bn
Die Size
1x1-2x3mm
EEPROM, MCU, Security Chips, Watches
4x4mm
Additional Device Types: Analog, IPD, MOSFET
Nokia phones with 7-8 WLCSP
4x4mm
Bluetooth, WLAN, TV Chip, Transceiver
5x5-6x6mm
Transceiver, Power Manager, Image Sensor, Audio Codec
Wide adoption in smartphones
5x5-7x7mm
Combo/Connectivity, MCU
Wider adoption outside portable products, expect up to 8x9mm die size
Fan out and enhanced versions in HVM
1995
2000
2005
2010
2015
2020
Kc1114.085bp-timeline
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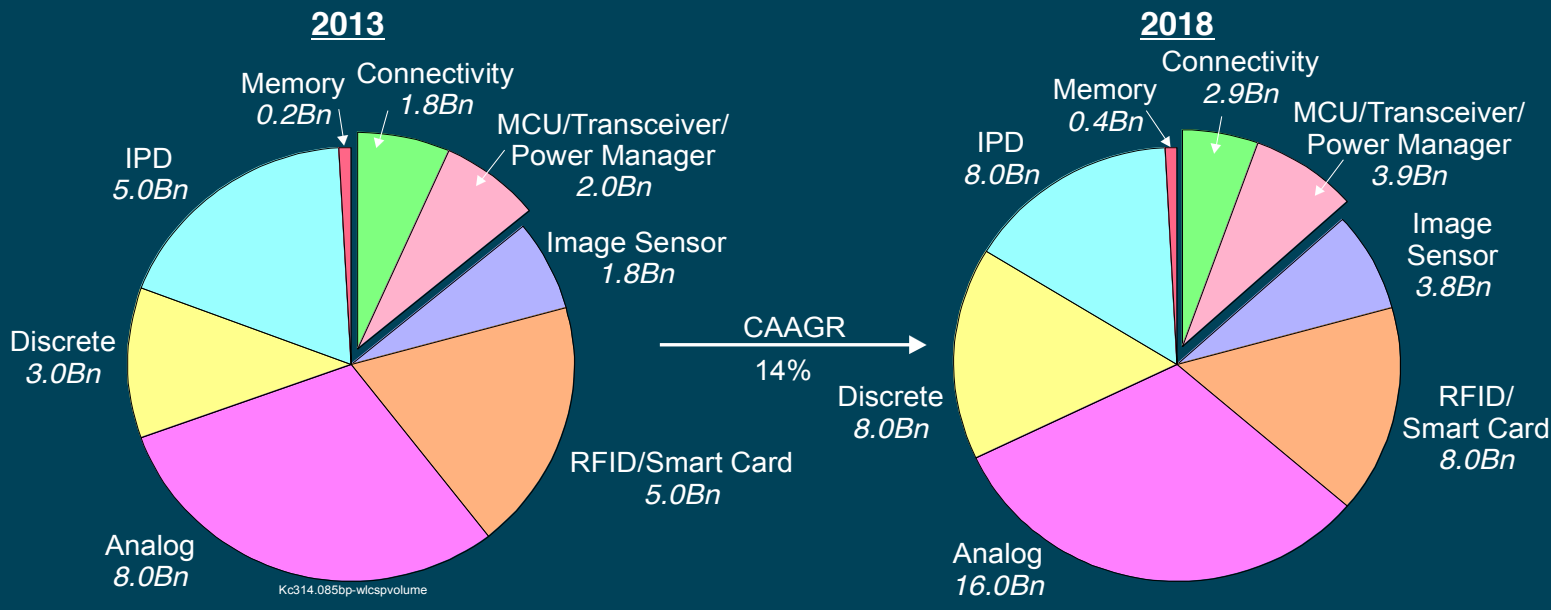
14

WLCSP MARKET AND GROWTH FORECAST
(Includes ICs, Discretes, Opto, Passives)
Unit Volume



Total: 27Bn Units

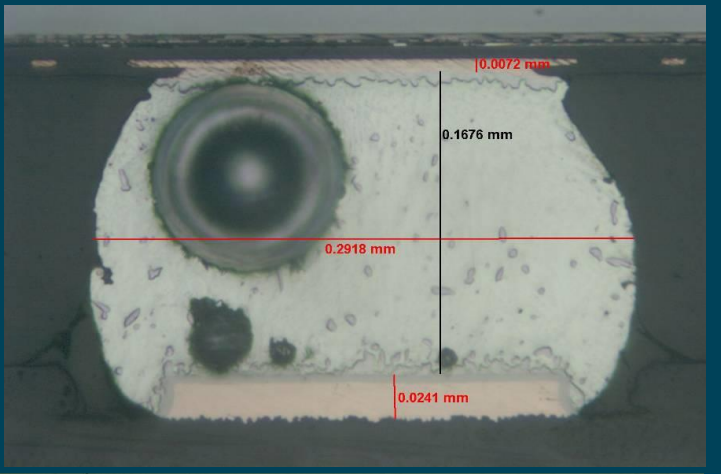
Total: 51Bn Units

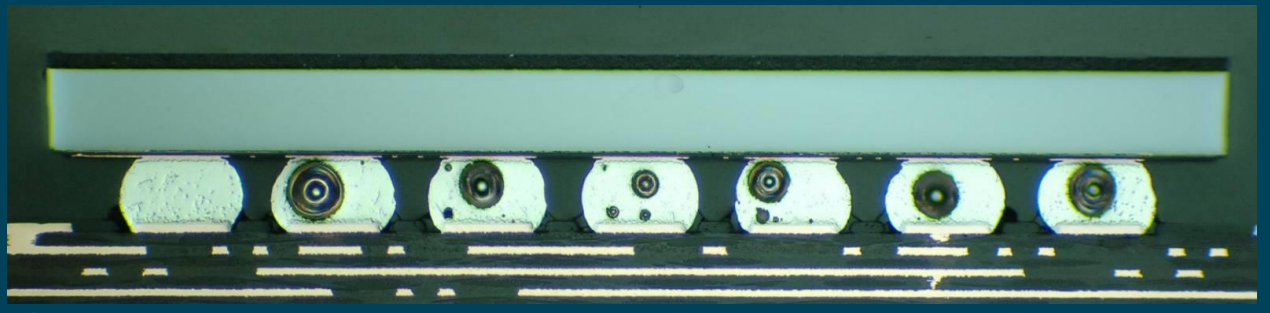
Note: Many devices do not have RDL - RFID/smart cards, some analog discretes, and IPD.

914.1/085bp

ATMEL SAM53G ARM-BASED MCU

- Found in Samsung Galaxy S5
- 3.2 x 3.1mm
  - <0.5mm mounted height
  - 200µm die thickness
  - 49 balls at 0.4mm pitch
- One metal layer RDL
- 30µm back side lamination
- No underfill

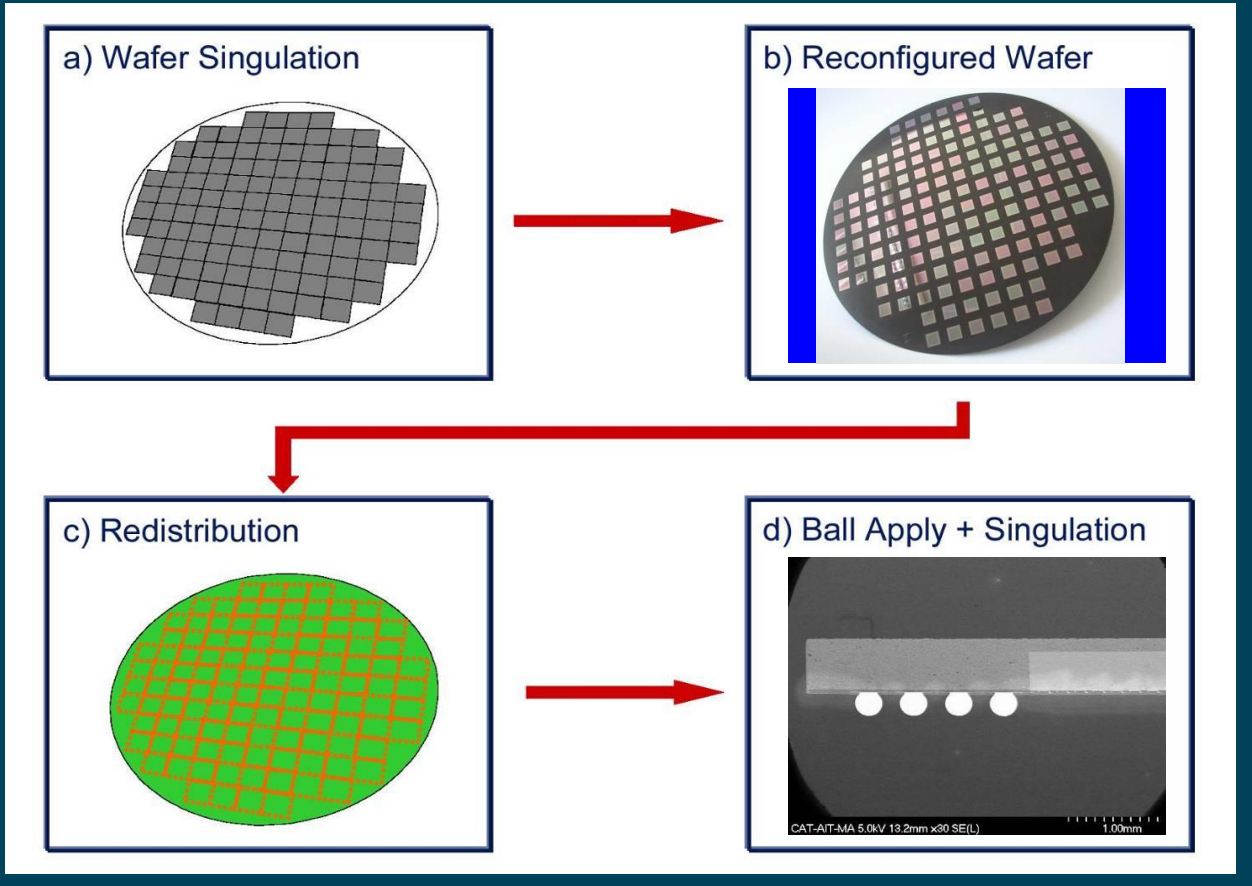




Photos source: Prismark/Binghamton University

37.9/085bp

INFINEON FAN-OUT WAFER LEVEL PACKAGE



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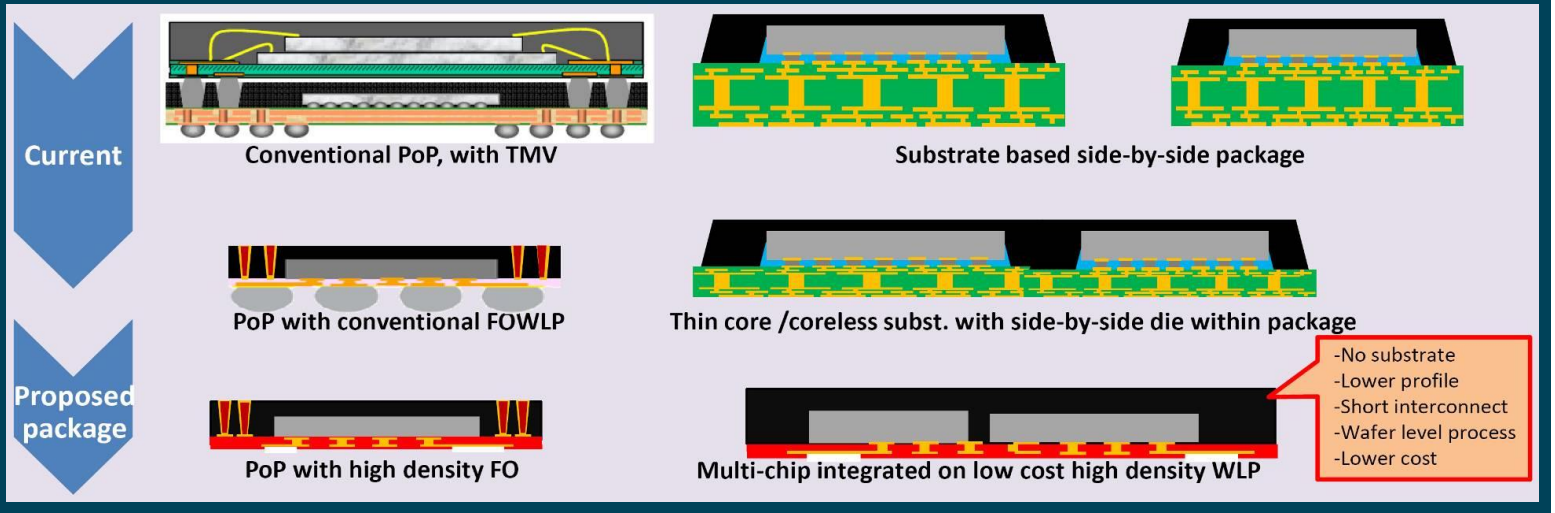
MULTI-DIE PACKAGE OPTIONS



*Source: A*STAR Institute of Microelectronics*

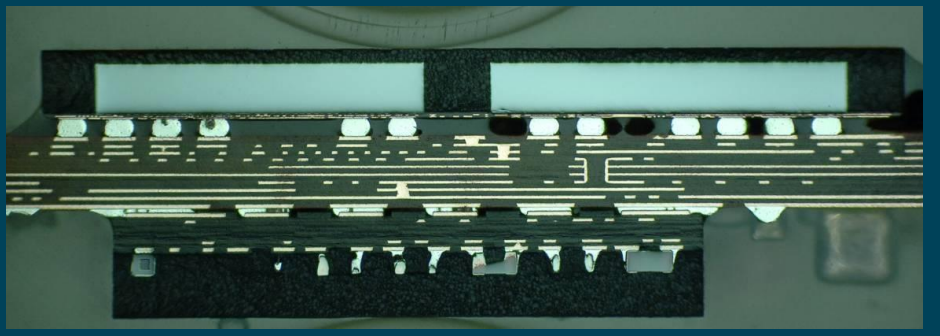
FAN-OUT WAFER LEVEL PACKAGES

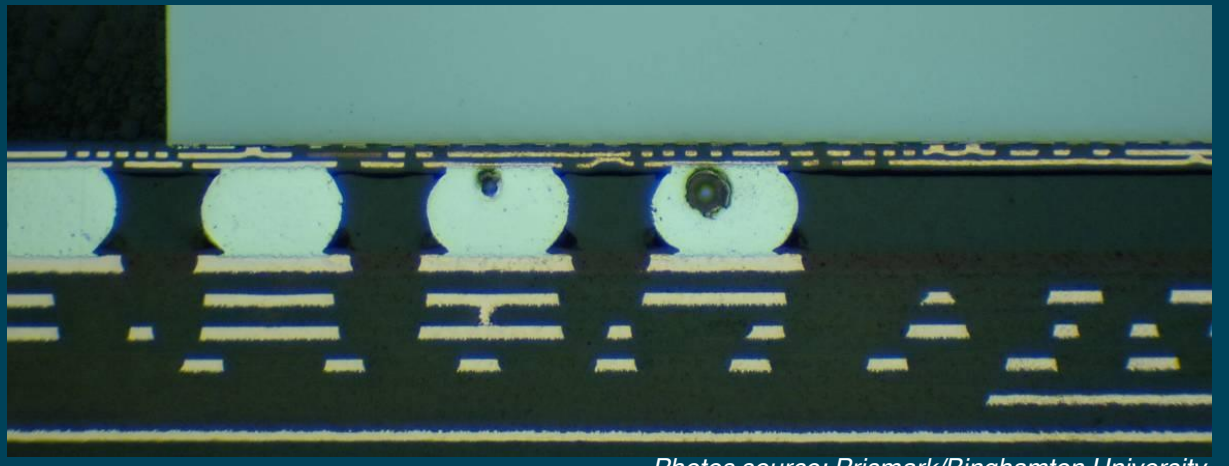
- FO-WLP packaging is currently used for <5mm die with <200 I/O
  - Baseband, automotive radar chipsets, and similar in production
  - Power management, transceivers, MCU under development.
- 2014 Market shipments down below 100M, after peaking in 2012 at over 200M
  - Renewed interest and cost reductions may drive demand to 800M units by 2018
- Use of FO-WLP for larger die (application processors) remains unclear
  - TSMC is pushing this technology
  - Several die suppliers showing interest: Apple, MediaTek, Qualcomm, Marvell, and NVIDIA
- Key concerns of large size FO-WLP
  - Cost
  - Yield: “substrate” and assembly
  - Reliability: Warpage

1214.6/193bp

SPREADTRUM SC8502

- 7.4 x 7.4 x 0.71mm FO-WLP
  - 230 balls @ 0.4mm pitch
- 2.8 x 2.8 and 3.0 x 3.0mm die
  - 430µm die thickness
  - 115µm mold cap over die
- Two metal layer RDL
  - 7 – 9µm metal thickness
  - 6 – 7µm dielectric layers
  - 20µm L/S (measured)





Photos source: Prismark/Binghamton University

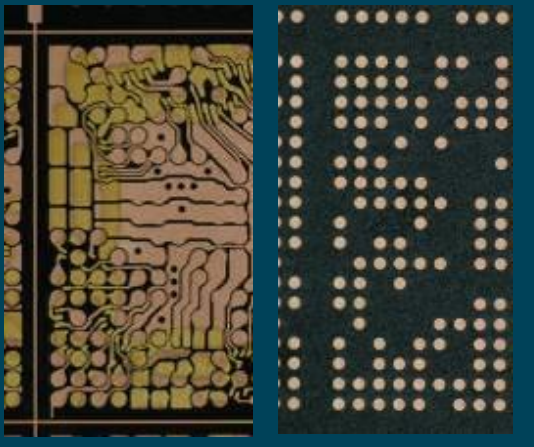
FO-WLP OUTLOOK

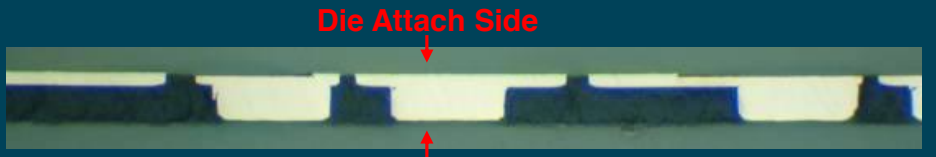
- TSMC is the most aggressive promoter of large size FO-WLP, with Apple a possible target user. Advantages of FO WLP
  - Package height reduction
  - Smaller body size
  - Better tolerance control of conductor traces
- Others are more cautious due to:
  - Yield: 99% yield is definitely required.
  - Cost: FCCSP still has a cost advantage
  - Reliability and performance: Warpage, delamination, adhesion and component movement are all challenges for larger die
- For 2015/2016, TSMC is planning to expand production capacity

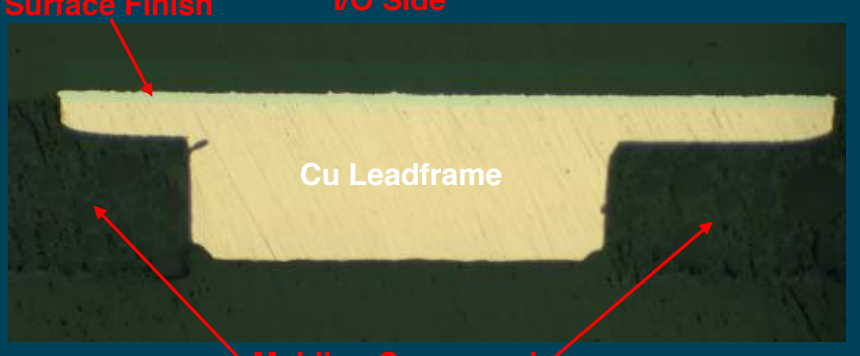
214.1/115mvc

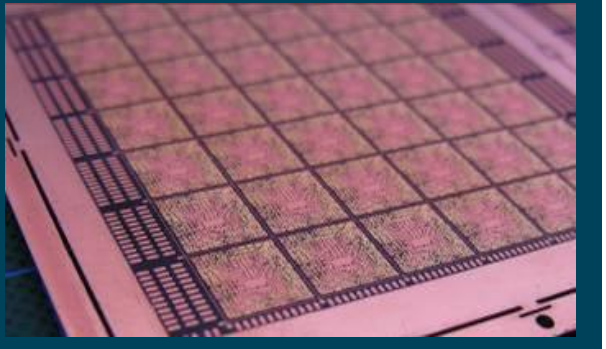
MOLDED INTERCONNECT SUBSTRATE

- Pre-molded leadframe substrate
  - Supports wire bond or flip chip die
  - Die or package stacking possible
  - 15µm line/space for fan-in/fan-out
  - LGA or BGA designs, up to 500 I/O
  - Multi-row or full-array designs
  - Wide range of package size
  - Package thickness 0.4mm min









Photos source: Prismark/Binghamton University

MOLDED INTERCONNECT SUBSTRATE (MIS)

- Initially developed by Advanpack Solutions Pte. Ltd. (APS) in Singapore with licensed to:
  - Microcircuit Technology in Singapore
  - JCET in China
  - Phoenix Pioneer Technology (PPT) in Taiwan: C2iM (Copper Connection in Molding)
- Currently used for low I/O (<200) using single metal layer, but suppliers claim
  - 2 and 3 metal layer substrates can be produced
  - 20% lower cost
  - Low profile: (15 um thinner for 2L substrates)
  - Fine line (15 um or less) and better reliability (less moisture concerns)
- MIS substrate made by transfer molding or compression molding processes

1214.057kh

MOLDED INTERCONNECT SUBSTRATE (MIS)

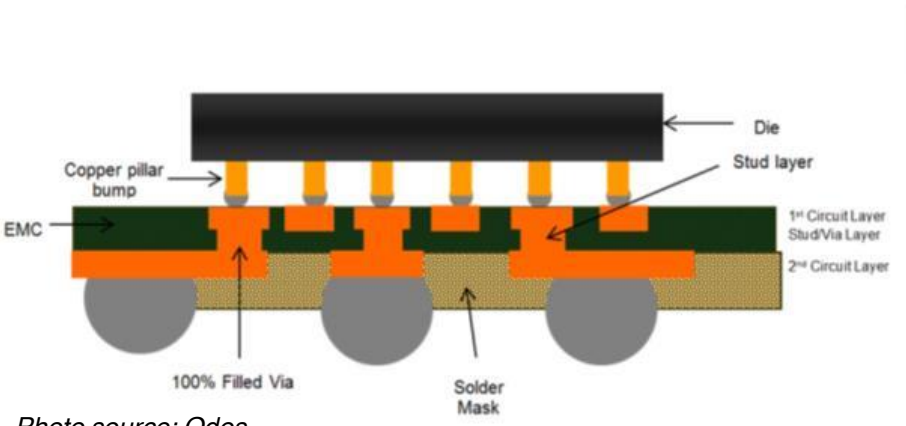


Photo source: Qdos

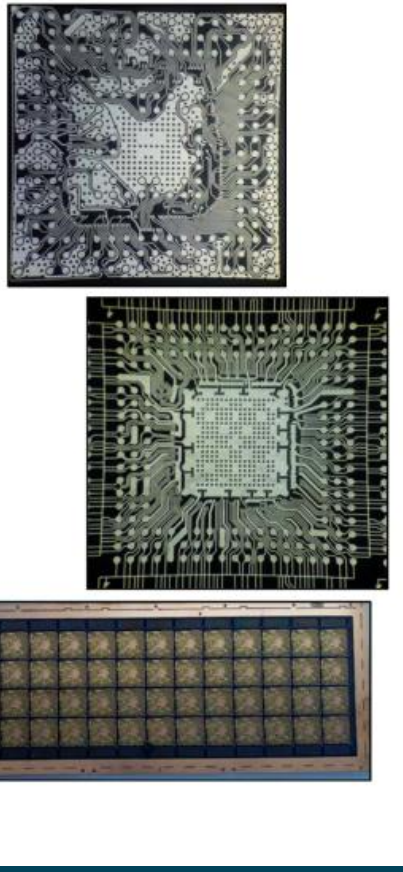


Photo source: APSi

MIS MARKET STATUS

- MIS substrates in production or are in qualification process
  - JCET and PPT shipping with plans to expand notably in 2015
  - Numerous IDMs interested or in qualification stages
- Successful for lower I/O devices
  - Targeting at mid I/O (500 to 800) FC CSP packages for mobile applications
- Technical challenges include:
  - Warpage
  - Adhesion
  - Brittleness
- Low cost is claimed by MIS suppliers, but issues remain:
  - Yield
  - Grinding
  - Photolithography processing
  - Metal carrier and thick dry film

0115.417skc

FCCSP SUBSTRATE COMPARISON

	2L STD Substrate	2L ETS Substrate	2L C²iM*
			
Process	Double Laser Patterning	Single Laser Buried Trace	No Laser Buried Trace
Fine Line	L/S=25/25	L/S=15/15	L/S=15/15
High Density (Via Size)	∅=80um	∅=80um	W≥40um
Material	BT with Glass Fiber	BT with Glass Fiber	Molding Compound
Cost	1.0	0.95	0.78
Extension	Easy but Expensive for **EPS**	Hard for **EPS**	Easy and Cheap for **EPS**

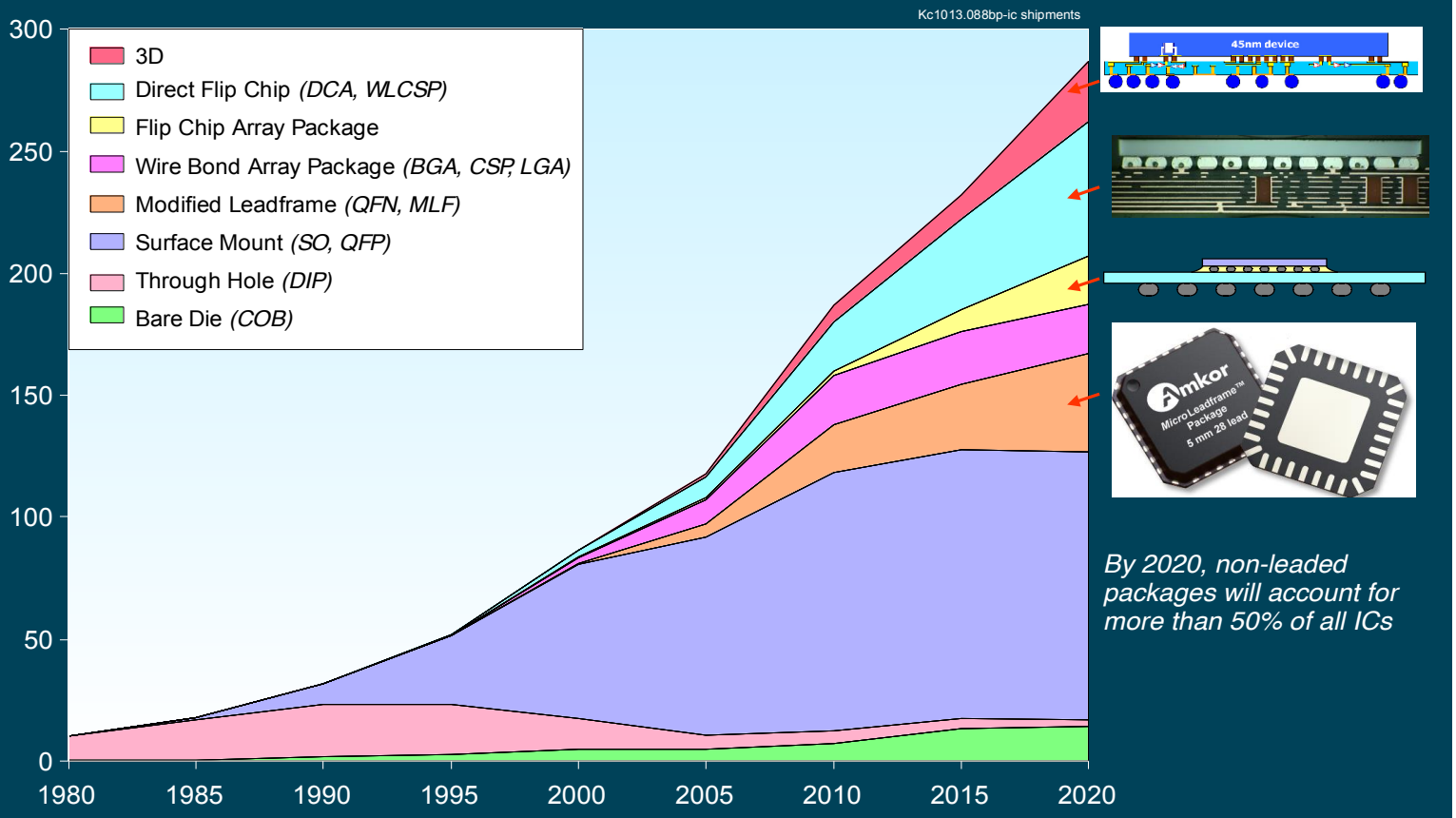
* C²iM: **C**opper **C**onnection in **M**olding

Source: PPt

PACKAGING TECHNOLGY FOR WEARABLE ELECTRONICS

- WLCSP and QFN are thin and low cost
- PoP and stacked die also widely available
- SiP: Integrating sensor, logic, and memory in single package
- Mature technology for low cost and high reliability
- Innovations in packaging still to come from smartphones:
  - Wearables can adopt these developed technologies
  - Expect more advanced modules and packages for sensors and processors in products to ship in 2015

IC SHIPMENTS BY PACKAGE CATEGORY



By 2020, non-leaded packages will account for more than 50% of all ICs

SAMSUNG TSV ANNOUNCEMENT

914.5/294bp

- August 2014 announcement by Samsung to produce DDR4 packages using TSV
  - Backed by actual part numbers on datasheet (e.g. M393A8G40D40)
  - Engineering samples now, with mass production in 2015
- Will go into 64GB modules for server applications
  - Stacks four 4Gb die at 2xnm; small die size (<7 x 7mm)
  - 128GB modules initially posted on datasheet now removed
  - Claims 50% power reduction versus current 64GB DDR3 modules using wire bond stacks
- Prismark forecast for 2015 remains near 100,000 total DRAM wafers for DRAM TSV
  - Samsung is a $1,000 RDIMM for servers, aligned with Intel Haswell-EP processors priced near $5,000 each
  - Intel Knights Landing (Xeon Phi) to use Micron HMC by mid-2015
  - SKHynix DDR4 datasheets also shows similar options for two- and four-die TSV DRAM packages

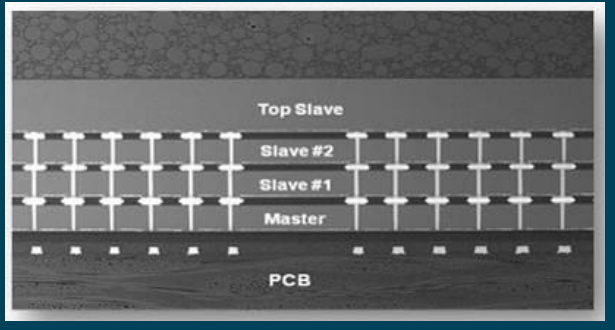


Photo source: Samsung

SUMMARY

- Package size and pitch reduction is ongoing, but a few new technologies have emerged
  - Fan-Out Wafer Level CSP
  - Molded Interconnect Substarte (MIS)
- The needs for miniaturization have not slowed
  - Fine Pitch (0.5 → 0.4 → 0.35 → 0.3/0.25mm)
  - Wafer Level CSP getting traction outside portables
  - Reduced Z- height packages (0.25 to 0.5mm) in portables
- 3D TSV and Silicon Interposer approaches continue long path to mainstream
  - Some companies looking for alternative options to deliver similar results