FIFTEENTH ANNUAL BiTS 2014
Burn-in & Test Strategies Workshop

Session 7

Wednesday 3/12/14 10:30am

FEEL THE BURN-IN

Burn-in is used to ensure a device's reliability and lifetime. The two papers in this final session look at parallel burn-in methods. The first presents an overview of built-in IC test and monitoring methods and describes the access buses for these test and monitor methodologies. It will also describe a hardware and software framework that exploits these test technologies for the massively parallel burn-in and test of 100's of complex ICs. The second presents some interesting challenges along the road to parallel burn-in test. It will include design requirements and rules to optimize the overall device power consumption; and go one step further on managing the unexpected challenges.

Massively Parallel Burn-in Test Using IC Serial Buses

Billy Fenton—OLAS Consulting
Pat Mitchell—Accutron

This Paper

Challenges of Increasing Parallelism in Burn-in Testing

Low Yeow Hock—Infineon Technologies Asia Pacific

Challenges of Increasing Parallelism in Burn-in Testing

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Infineon Technologies Asia Pacific

2014 BiTS Workshop
March 9 - 12, 2014

Content

- Background
- Design of high parallelism boards
- Early results
- Challenges in production
- Summary

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Background

- As to increase the throughput in a high volume testing environment, high parallelism on burn-in boards (BIB) is one of the solutions to achieve low operating cost
- There are a lot of factors to be considered, including: oven, controller board, BIB, product, production, etc
- Beyond the technical know how, managing the unexpected challenges is the key to success
- We present challenges encountered with high parallelism BIBs in production

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Design high parallelism boards

- How to optimize the parallelism with a predefined BIB dimension?

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Design high parallelism boards

- Mechanical aspects:
  - Smaller, “standardized” socket footprint
  - Components: size and specs
  - Less test points, debug features
  - Less connections
  - Increase the number of PCB layers
  - PCB material selection based on temperature cycling requirement

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Design high parallelism boards

- Electrical aspects:
  - Signal integrity
  - Product testing requirement
  - Overall power consumption for devices
  - Heat dissipation
- Capabilities of ovens and controller boards
- Good manufacturing practice:
  - know what is the best fit for production

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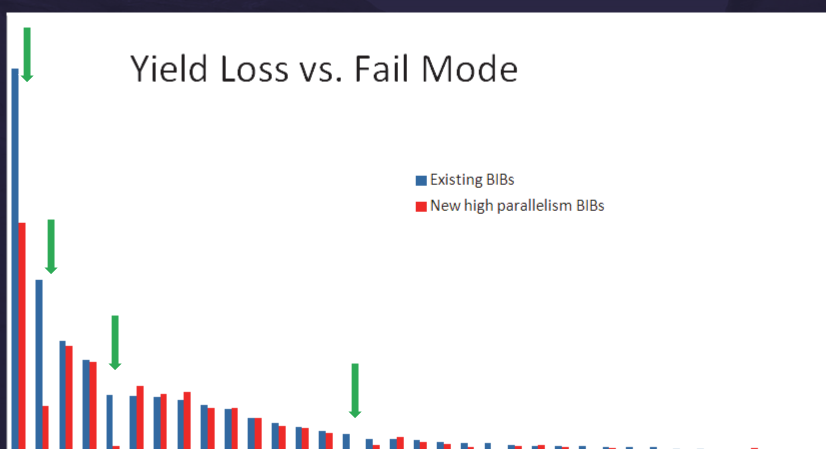
Early results

- Throughput and yield have met expectations
- There has not been any sudden change in the failure mode on specific tests that is not supposed to be influenced by hardware changes
- But there is some yield gain coming from improvements on test stability as well as new hardware

Early results



Challenges in production

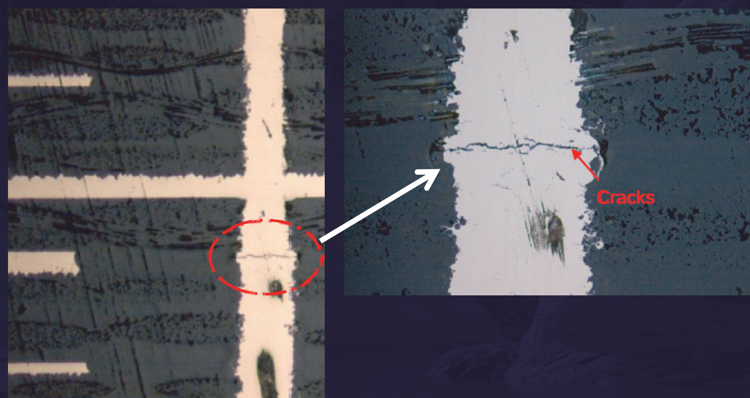
- While we were confident of the implementation, however, after some time problems have started to surface…

Challenges in production

- Problem #1: intermittent device detection on the sockets
- This causes lower socket utilization and hence affecting output

Challenges in production

- Cross-section examination of the BIB PCB reveals via cracks underneath the PCB layer



Challenges in production

- Problem #2: process driven board level failures
- Failure rate increases by a factor of three without any pre-warning
- Finding: broken molded socket guides cause misalignment on the device pin
- There is temperature dependency
- Additional procedure was introduced in production to locate those sockets

Challenges in production

- We observed that broken socket mold guide(s) mainly happened on one side of the socket
- Damaged socket locations show some correlation to the loader machine. Loader placement accuracy of >99% must be fulfilled
- Experiments from vendor suggest that the force to break the mold guide is considerably high

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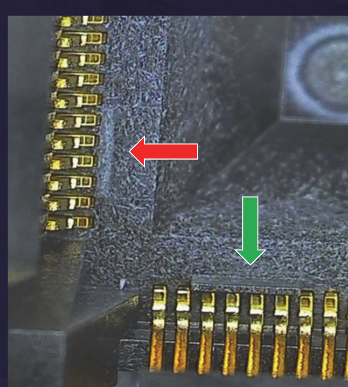
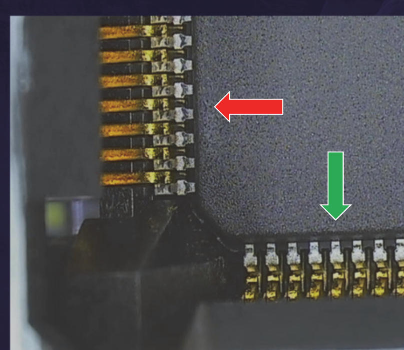
Challenges in production

- Broken socket mold guide (red arrow)





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Challenges in production

- Problem #3: complete board shutdown
- As the parallelism increases, the impact of a complete board shutdown is getting larger
- As a result, it increases the retest rate

Challenges in production

- Temperature dependency: Almost half of the shutdown appears after superhot to cold temperature transition
- Package dependency: it affects QFP packages more than BGA packages
- Some relaxation in test program helps, but not really effective

Challenges in production

- Possible root causes:
  - We are getting closer to the power supply limits (hardware limitation) with elevated stress and temperature
  - Hardware maintenance becomes harder with dense sockets and smaller components
  - Test stability at VDDmin

Summary

- The problems we have seen were more complex in nature, and there is no single solution for those problems
- We need to specify the use patterns and life expectancy for BIBs
- Vendors are supportive in strengthening the mold guide structure
- We need continuous improvement to ensure the robustness of our manufacturing process