FIFTEENTH ANNUAL BiTS 2014
Burn-in & Test Strategies Workshop

Session 7

Wednesday 3/12/14 10:30am

FEEL THE BURN-IN

Burn-in is used to ensure a device's reliability and lifetime. The two papers in this final session look at parallel burn-in methods. The first presents an overview of built-in IC test and monitoring methods and describes the access buses for these test and monitor methodologies. It will also describe a hardware and software framework that exploits these test technologies for the massively parallel burn-in and test of 100's of complex ICs. The second presents some interesting challenges along the road to parallel burn-in test. It will include design requirements and rules to optimize the overall device power consumption; and go one step further on managing the unexpected challenges.

Massively Parallel Burn-in Test Using IC Serial Buses

Billy Fenton—OLAS Consulting
Pat Mitchell—Accutron

Challenges of Increasing Parallelism in Burn-in Testing

Low Yeow Hock—Infineon Technologies Asia Pacific

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Massively Parallel Burn-in Test Using IC Serial Buses

Billy Fenton, OLAS Consulting
Pat Mitchell, Accutron

2014 BiTS Workshop
March 9 - 12, 2014

Content

- Background
- Architecture overview
- Built-In Test (BIT) approaches
- Built-in Test in detail
- Accessing BIT using IEEE 1149.n
- Other types of serial access buses
- A Configuration for Parallel Burn-in Test
- Programming and Configuration
- Summary

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Background

- Complex ICs require alternative test approaches.
- A continuing move to BIT.
- BIT can often be accessed using a low-pin count serial bus (e.g. IEEE 1149.1).
- Burn-in driver cards can leverage BIT and a driver with 24, 48, 96, etc., channels can be used for parallel test during burn-in

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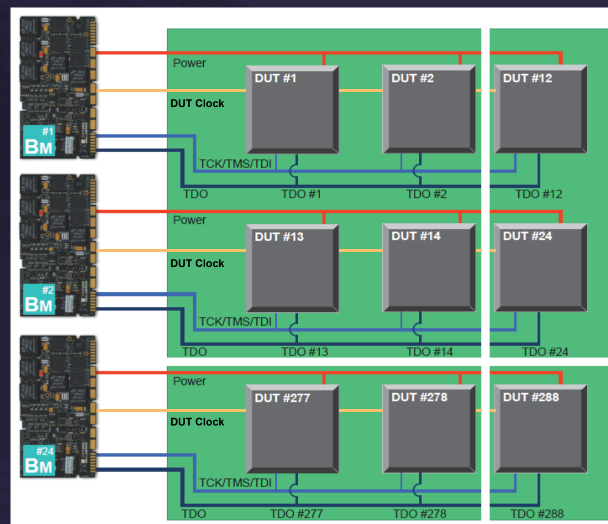
Architecture Overview



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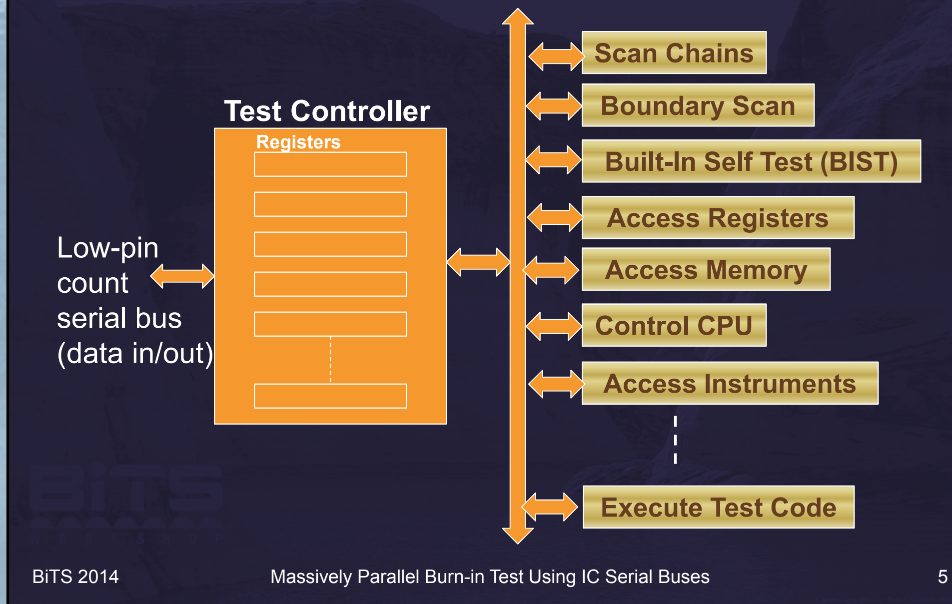
Built In Test Approaches
Test Controller
Registers
Low-pin count serial bus (data in/out)
Scan Chains
Boundary Scan
Built-In Self Test (BIST)
Access Registers
Access Memory
Control CPU
Access Instruments
Execute Test Code
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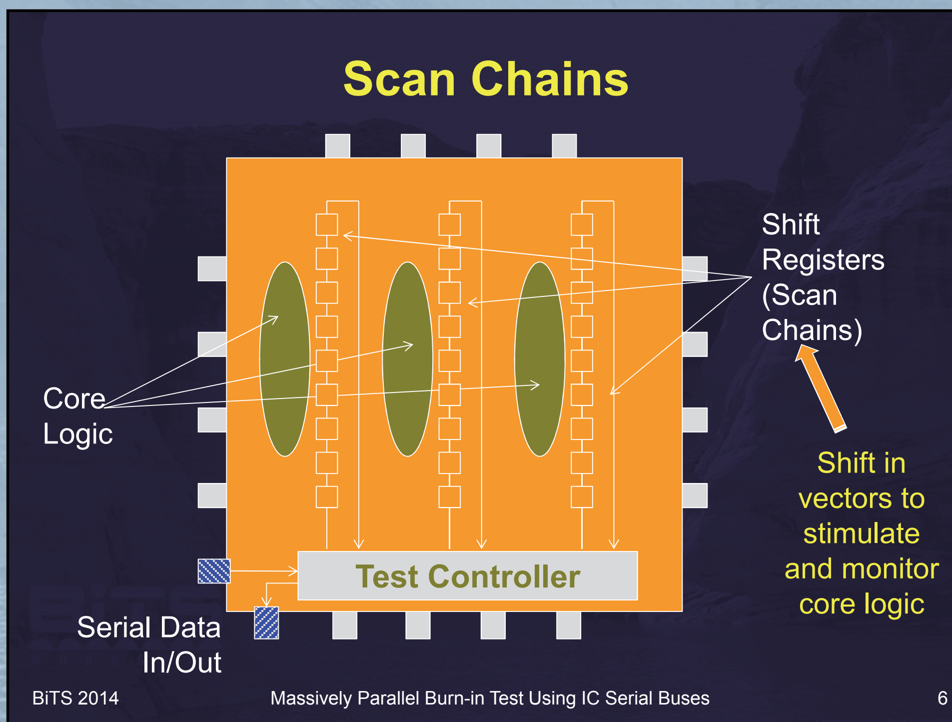
5


Scan Chains
Shift Registers (Scan Chains)
Core Logic
Shift in vectors to stimulate and monitor core logic
Test Controller
Serial Data In/Out
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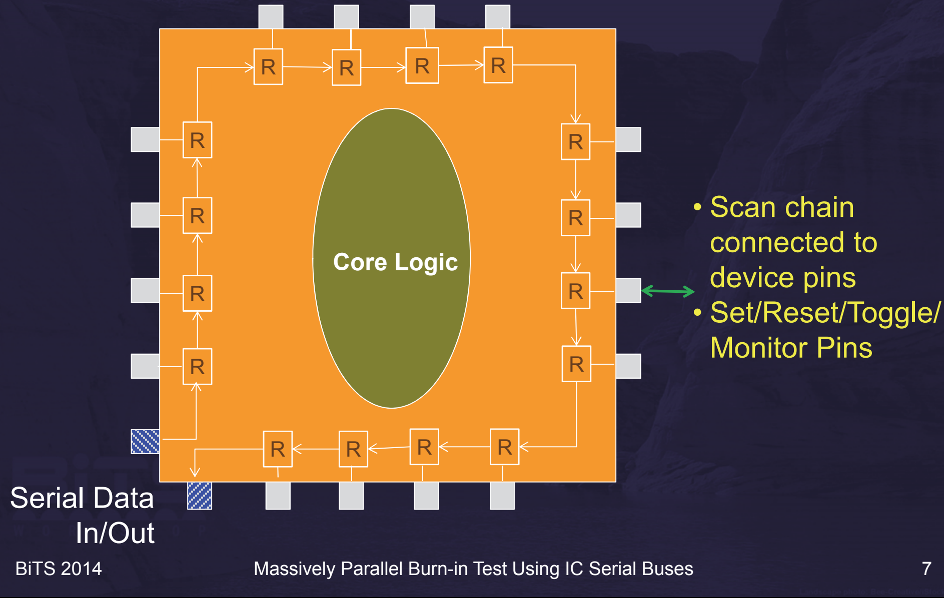
6


Boundary Scan (A Scan Chain Example)
R
Core Logic
• Scan chain connected to device pins
• Set/Reset/Toggle/ Monitor Pins
Serial Data In/Out
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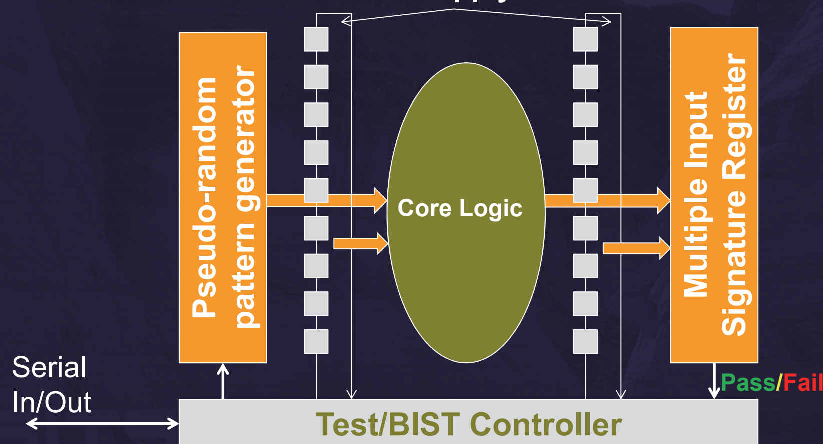
7


Logic BIST
Alternatively Scan Chains may be used to apply vectors
Pseudo-random pattern generator
Core Logic
Multiple Input Signature Register
Serial In/Out
Pass/Fail
Test/BIST Controller
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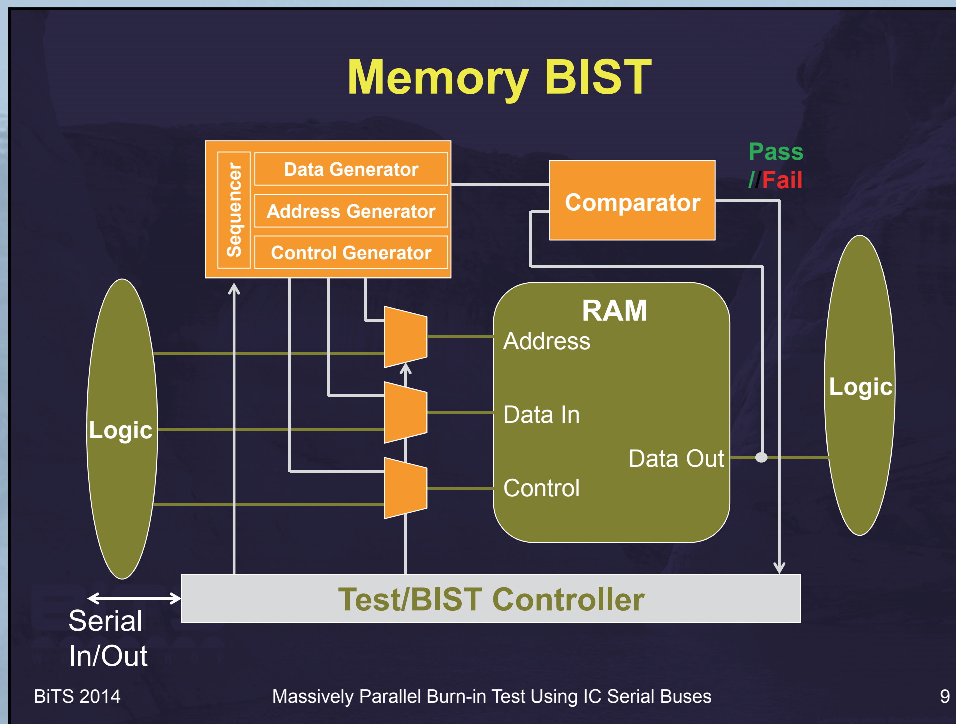
8


Memory BIST
Data Generator
Address Generator
Control Generator
Sequencer
Comparator
Pass
/Fail
RAM
Address
Data In
Data Out
Control
Logic
Logic
Test/BIST Controller
Serial
In/Out
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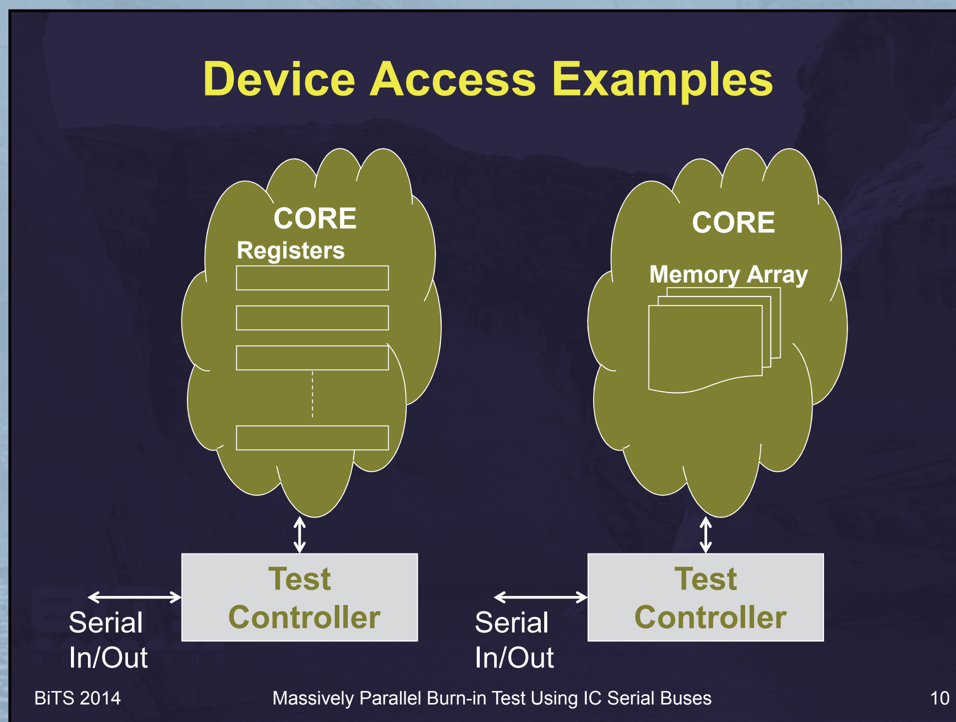
9


Device Access Examples
CORE
Registers
CORE
Memory Array
Test
Controller
Test
Controller
Serial
In/Out
Serial
In/Out
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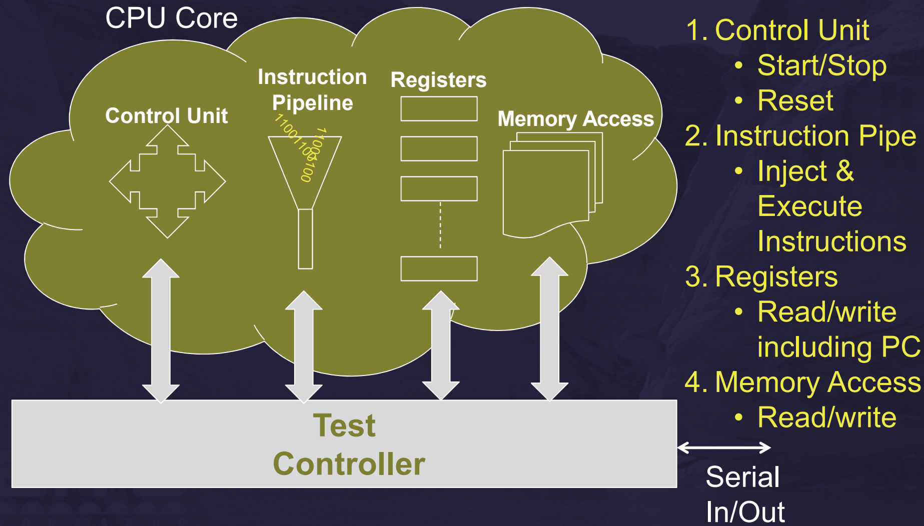
10


Control CPU Operation
CPU Core
Control Unit
Instruction Pipeline
Registers
Memory Access
Test Controller
Serial In/Out
1. Control Unit
• Start/Stop
• Reset
2. Instruction Pipe
• Inject & Execute Instructions
3. Registers
• Read/write including PC
4. Memory Access
• Read/write
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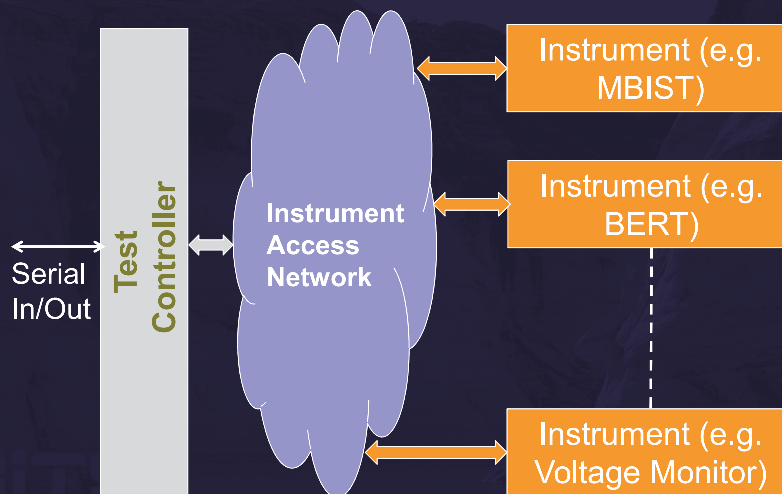
11


Embedded Instruments
Serial In/Out
Test Controller
Instrument Access Network
Instrument (e.g. MBIST)
Instrument (e.g. BERT)
Instrument (e.g. Voltage Monitor)
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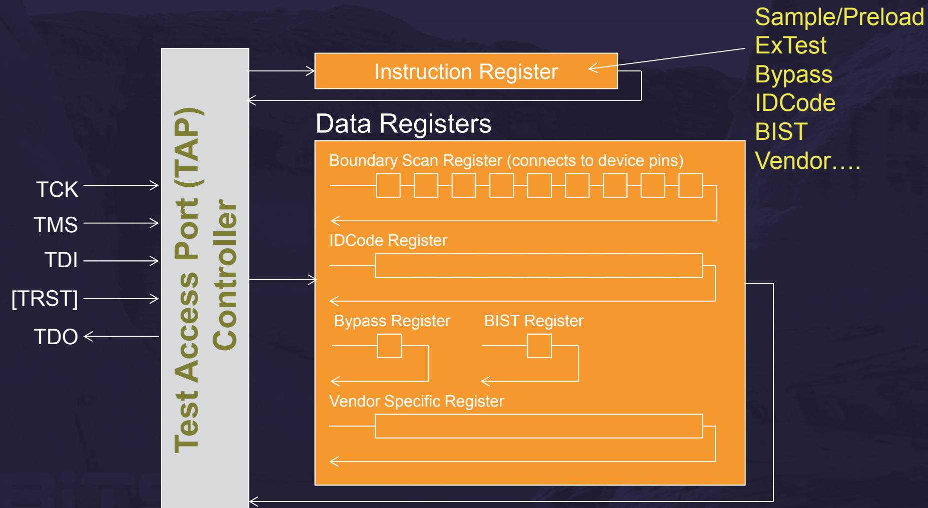
12



Some JTAG Data Formats

```
-- ***************************************************
-- *                PIN MAPPING                      *
-- ***************************************************

attribute PIN_MAP of CHIPx : entity is PHYSICAL_PIN_MAP;
constant TQFP64 : PIN_MAP_STRING :=
--I/O Pins
" D0:          1       ,"&
" D1:          2       ,"&
" D2:          3       ,"&
" D3:          4       ,"&
" CS:          5       ,"&
" RD:          6       ,"&
" WR:          7       ,"&

-- ***************
-- *     INSTRUCTI
-- ***************

attribute INSTRUCT
attribute INSTRUCT
  "BYPASS
  "EXTEST
  "SAMPLE
  "PRELOAD
  "IDCODE
  "VENDOR
  "HIGHZ
```

```
!Begin Test Program
TRST OFF;                                    !Disable Test Reset line
ENDIR IDLE;                                  !End IR scans in IDLE
ENDDR IDLE;                                  !End DR scans in IDLE
HIR  8  TDI (00);                            !8-bit IR header
HDR 16  TDI (FFFF) TDO (FFFF) MASK (FFFF);   !16-bit DR header
TIR 16  TDI (0000);                          !16-bit IR trailer
TDR  8  TDI (12);                            !16-bit DR trailer
SIR  8  TDI (41);                            !8-bit IR scan
SDR 32  TDI (ABCD1234) TDO (11112222);       !32-bit DR scan
STATE   DRPAUSE;                             !Go to stable state DRPAUSE
RUNTEST 100 TCK ENDSTATE IRPAUSE;            !RUNBIST for 100 TCKs
!End Test Program
```

- BSDL (device definition)
- SVF (test sequence)
- STAPL
- IEEE 1532

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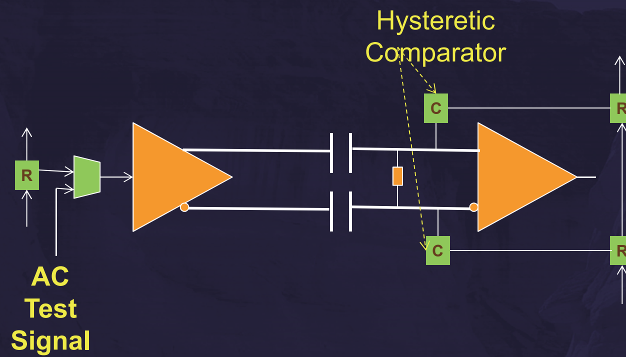
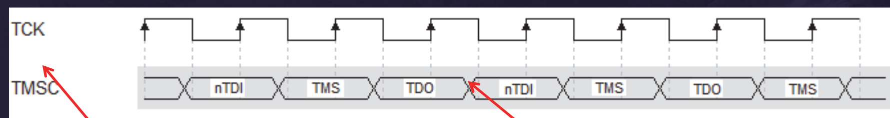
Differential JTAG: IEEE 1149.6



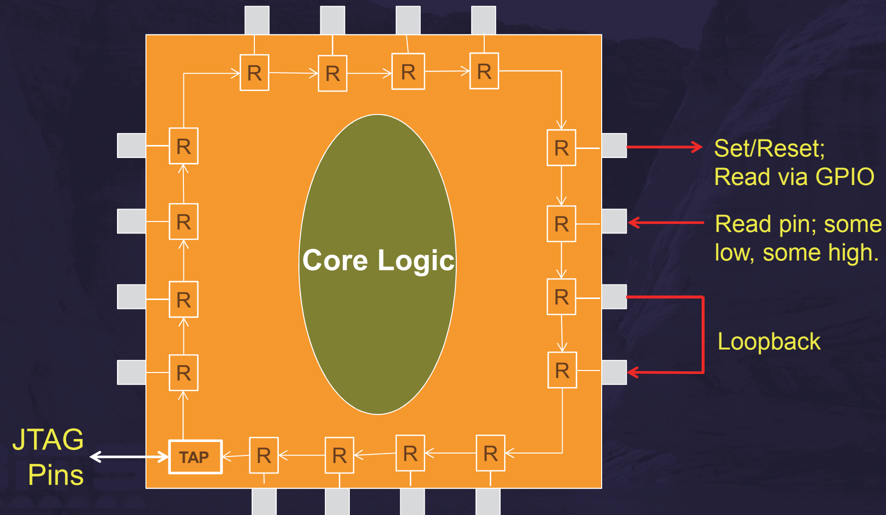
Additional Instructions: EXTEST_PULSE; EXTEST_TRAIN

JTAG: IEEE 1149.7



- From 5 pins to 2
- Useful for low pin count parts

- TDI/TDO/TMS share a pin.
- Various modes of operation


JTAG: Pin Stimulus/Monitor Example
R
Core Logic
Set/Reset; Read via GPIO
Read pin; some low, some high.
Loopback
JTAG Pins
TAP
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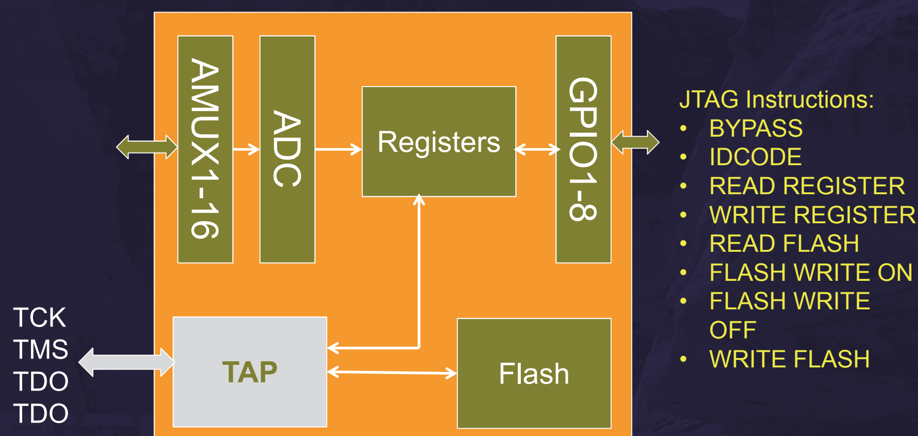
17


JTAG: Internal Access Example
AMUX1-16
ADC
Registers
GPIO1-8
TAP
Flash
TCK
TMS
TDO
TDO
JTAG Instructions:
• BYPASS
• IDCODE
• READ REGISTER
• WRITE REGISTER
• READ FLASH
• FLASH WRITE ON
• FLASH WRITE OFF
• WRITE FLASH
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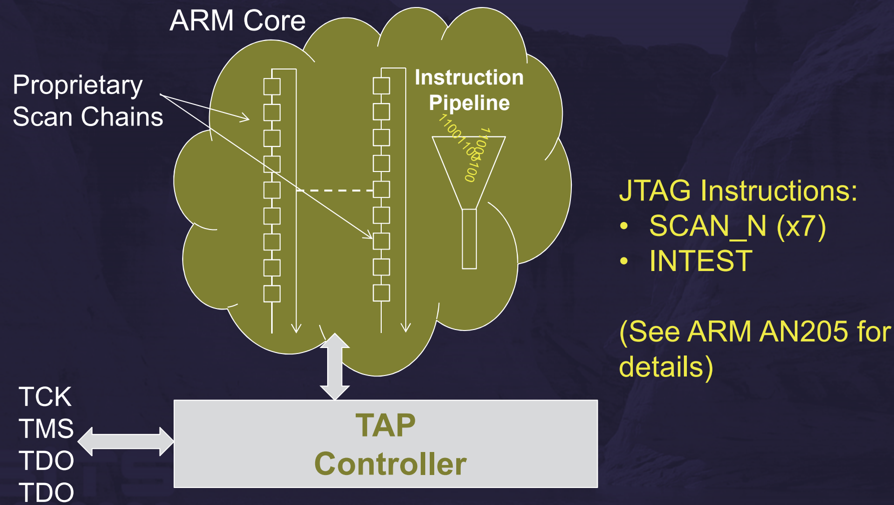
18


JTAG: CPU Control Example (ARM9)
ARM Core
Proprietary
Scan Chains
Instruction
Pipeline
JTAG Instructions:
• SCAN_N (x7)
• INTEST
(See ARM AN205 for details)
TCK
TMS
TDO
TDO
TAP
Controller
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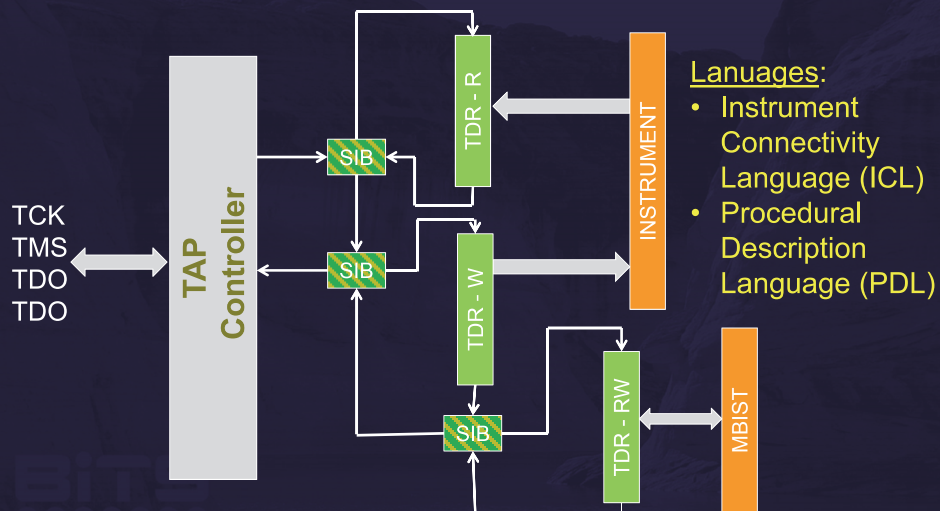
19


P1687 - I(nstrument)JTAG
Lanuages:
• Instrument Connectivity Language (ICL)
• Procedural Description Language (PDL)
TCK
TMS
TDO
TDO
TAP
Controller
SIB
SIB
SIB
TDR - R
TDR - W
TDR - RW
INSTRUMENT
MBIST
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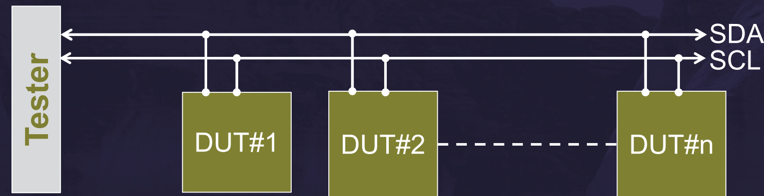
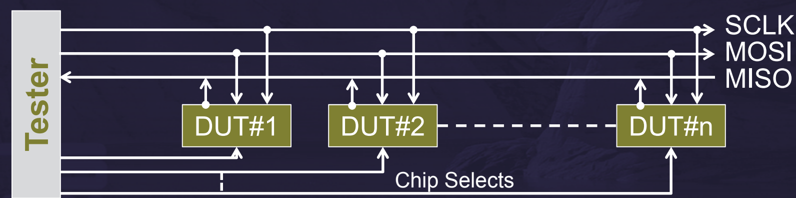
20

Other Serial Buses (I2C, SPI)

I2C



SPI



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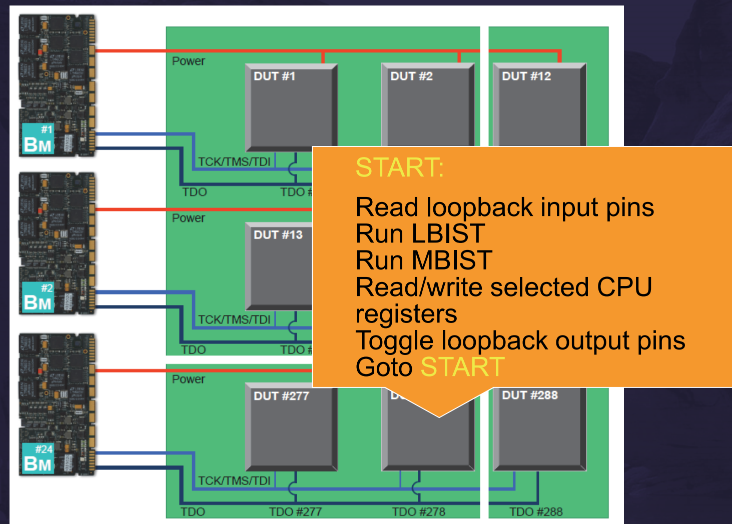
A JTAG Configuration for Parallel Test



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Code Compilation for Parallel Test

SVF Program (or similar) for single

```
!Begin Test Program
TRST OFF;                                  !Disable Test Reset line
ENDIR IDLE;                                !End IR scans in IDLE
ENDDR IDLE;                                !End DR scans in IDLE
HIR  8  TDI (00);                          !8-bit IR header
HDR 16  TDI (FFFF) TDO (FFFF) MASK (FFFF);!16-bit DR header
TIR 16  TDI (0000);                        !16-bit IR trailer
TDR  8  TDI (12);                          !16-bit DR trailer
SIR  8  TDI (41);                          !8-bit IR scan
SDR 32  TDI (ABCD1234) TDO (11112222);     !32-bit DR scan
STATE   DRPAUSE;                           !Go to stable state DRPAUSE
RUNTEST 100 TCK ENDSTATE IRPAUSE;          !RUNBIST for 100 TCKs
!End Test Program
```

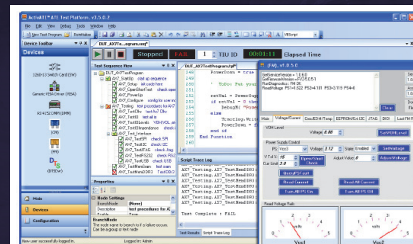
COMPILE

Parallel vectors for multiple devices
[TCK;TMS;TDI;TRST;TDO1;TDO2; etc.]

```
11010000000000000000
01010000000000000000
10011111111111111111
01110000000000000000
Etc.
```


High Level Code for Parallel Test

- API's
  - Driver Board
    - Download compiled vectors to vector memory.
    - Execute selected vector sequences.
    - Collect and log results.
  - Oven Controller
    - Set temperature cycle etc.



Summary

- Many ICs now include various forms of BIT.
- BIT can be controlled and accessed using low pin-count serial buses such as JTAG.
- JTAG only requires a small number of vector channels.
- This means that many devices can be tested using a burn-in driver card.
- Some additional compilation tools are required.

BiTS 2014 Massively Parallel Burn-in Test Using IC Serial Buses 25

References & Acknowledgments

- IEEE 1149.1 JTAG and Boundary Scan Tutorial by Dr. Ben Bennetts.
- ARM application note AN205.
- Adam Ley for his comments on IEEE 1149.7
- Al Crouch for his explanations of IJTAG.

BiTS 2014 Massively Parallel Burn-in Test Using IC Serial Buses 26