Session 6

Wednesday 3/12/14 8:00am

INTERCONNECTOLOGY: IT'S WHAT WE DO

Last Year's BiTS workshop introduced the benefits from the Interconnectology approach of collaboration across the supply chain from device design to test. This session focuses on interconnect designs and advancements. As contactor design has had to evolve to address shrinking pads and decreasing pitches, there's lower contact force. The first presenter then asks whether contact pressure has become more meaningful than contact force. The second presentation details the development of long-life stamped spring probes in response to challenging technology roadmaps, all at a cost that includes maintenance and replacement costs. Next up is a paper on validations sockets (used for post-silicon validation and are quite different from test sockets). This paper brings awareness to these sockets and their challenges to encourage industry collaboration for solving future post-silicon validation interconnect challenges. The session concludes with an exploration of crosstalk sources and discusses solutions and emerging technologies, including costs, to reduce crosstalk. See? It's all about Interconnectology.

Long Life / Stamped Spring Probe Development
Samuel Pak, A.J. Park—IWIN Co. Ltd.

Validation Interconnect Socket – Application and Future Challenges
Ashok Kabadi—Intel Corporation

This Paper

Crosstalk Mitigation in ATE Socket-Device Interface Boards
Thomas P. Warwick—R&D Altanova, Inc.

Crosstalk Mitigation in ATE Socket-Device Interface Boards

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2014 BiTS Workshop
March 9 - 12, 2014

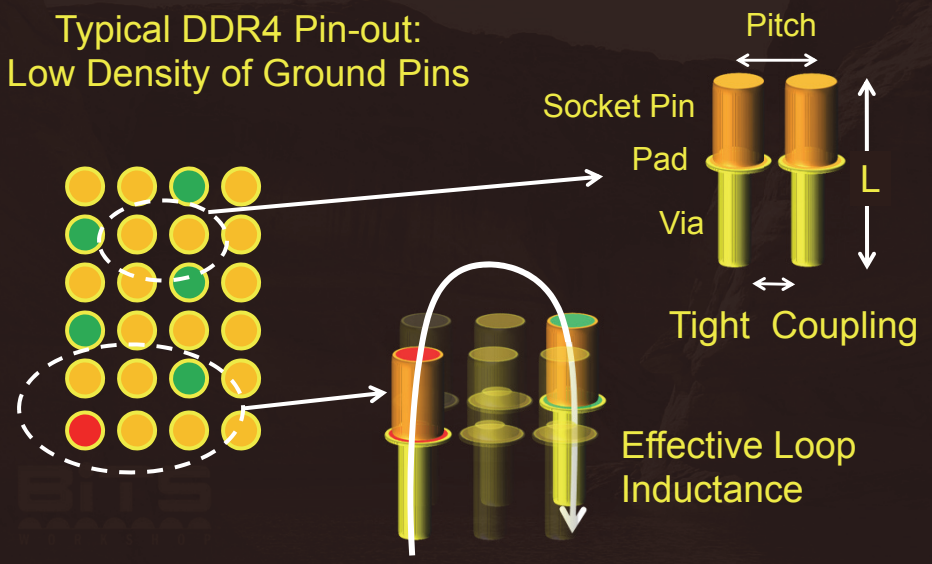
Content

- Purpose
- Crosstalk Effects: Digital, Analog, and Supply
- Crosstalk Mitigation Methods
- Application of Methods and Results: A Working Example
- Concluding Comments

Purpose

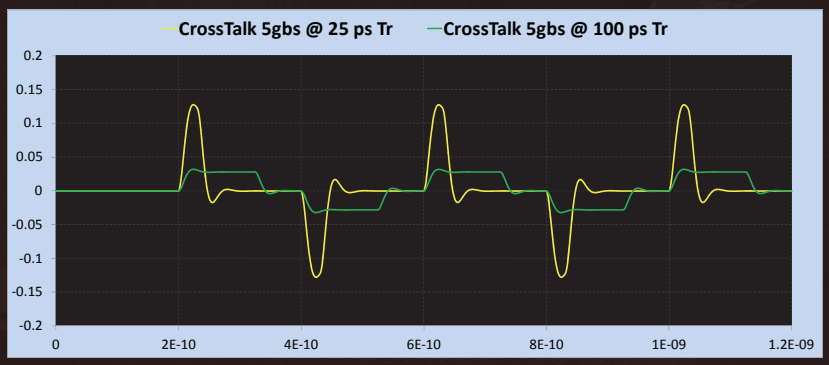
As device pin-count increases and package sizes decrease, crosstalk design in the package must often be compromised on account of market-driven cost pressures. This presentation discusses growing concerns with isolation and crosstalk relative to the socket and connecting via, given this reality. It discusses a series of methods to mitigate the effects of socket / via crosstalk and concludes with a working example.

The Problem: An Example



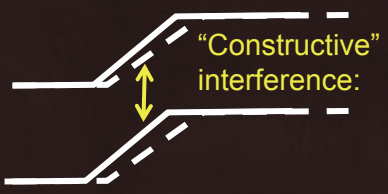
Crosstalk Effects: Digital Signal

Crosstalk is primarily a function of dv/dt of the aggressor at lower data rates



Crosstalk Effects: Digital Signal

"Even" Mode



Coupling Advances Timing

"Odd" Mode

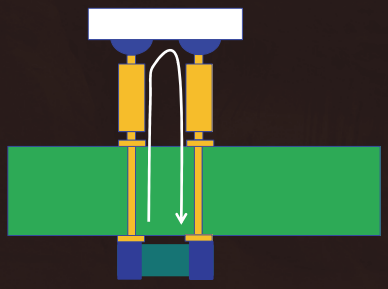
Coupling Delays Timing

Net Effect:

- Higher Jitter
- Poorer Setup and Hold Time Measurements
- Lower Yield Margins

Crosstalk Effects: Supply

SOCKET/ VIA EXAMPLE:



Loop Inductance: 3nh (measured)

Some Simple Estimating Math:

$\Delta V = L/(\#\ pins) \times \Delta i/\Delta t$

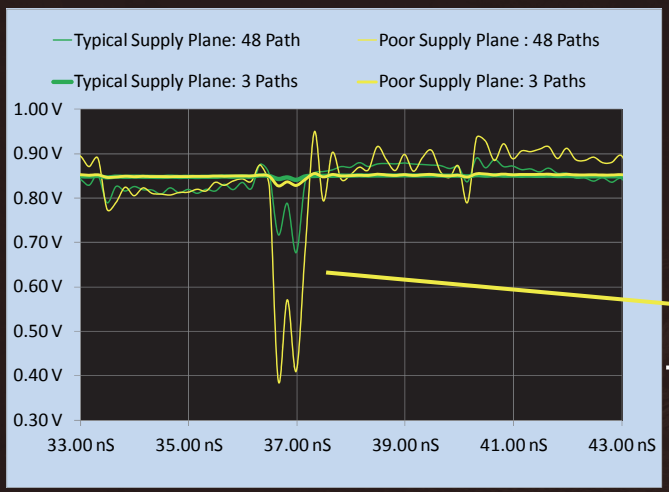
@ 10.2 amp/ns[1] and 100 Supply / Ground Pins

ΔV = 306 mV

1: (48 pins @ 80 ps edge rate / 0.85v)

Crosstalk Effects: Supply

Supply Droop in Time Domain



Higher Transition Load on supply Causes Timing Delay.

Crosstalk Mitigation: Shielding

Coaxial Structure

- Difficult in the PC board, under the device
- Difficult at Fine Pitch
- Less effective when GND is open on one end
- Drives Supply loop inductance higher

Add Surrounding Ground

- Only works in PC board
- Difficult below 0.65mm

Crosstalk Mitigation: Shielding

A relative comparison @ 10GHz:

4 GND Via + Short Socket pin	→	-26dB
4 GND Via + Coax Socket pin, Open, One End	→	-27dB
Coax Via + Coax Socket pin, Open, One End	→	-30dB
(Only if Device Pin-Out Allows)		
Coax Via + Coax Socket pin, Fully Terminated	→	-80dB

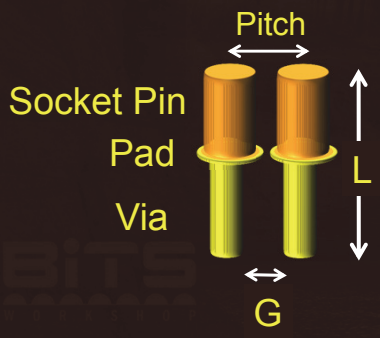
LOW

Relative Cost

HIGH

Crosstalk Mitigation: Gap and Coupling Length

We usually think of crosstalk in traces….

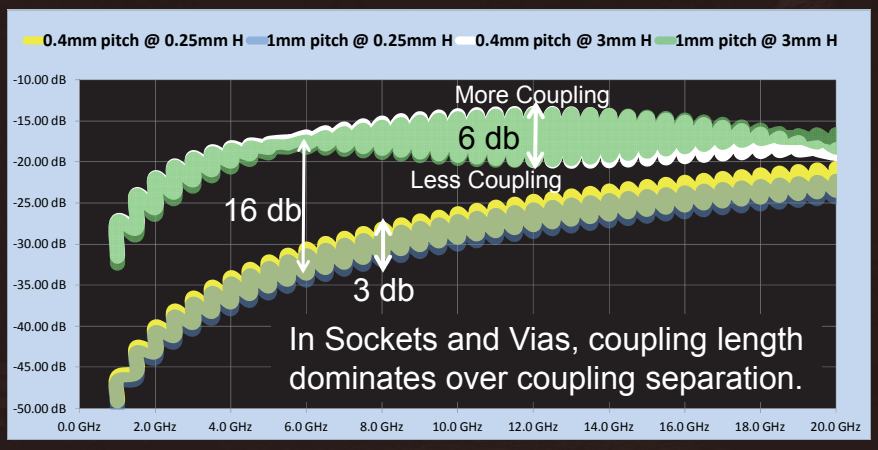


The socket / via combination is far more restrictive in adjusting the Gap and the Length.

Socket Gap/Pitch Ratio:
0.2 to 0.5 @ 0.4mm
0.1 to 0.8 @ 1.0mm

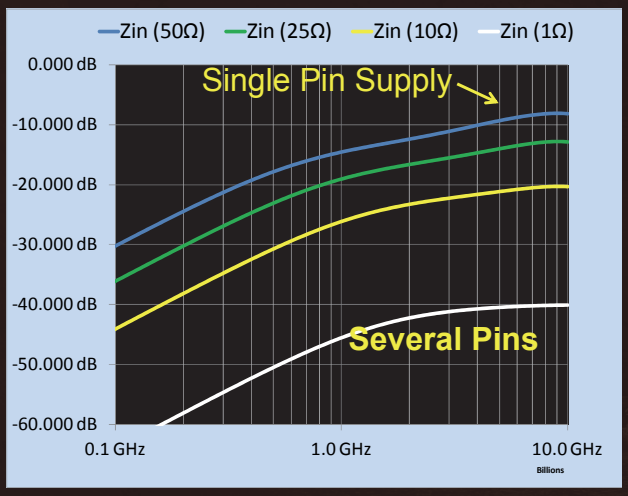
Crosstalk Mitigation: Separation and Coupling Length

Crosstalk as a Function of Spacing and Length



Crosstalk Mitigation: Low Impedance

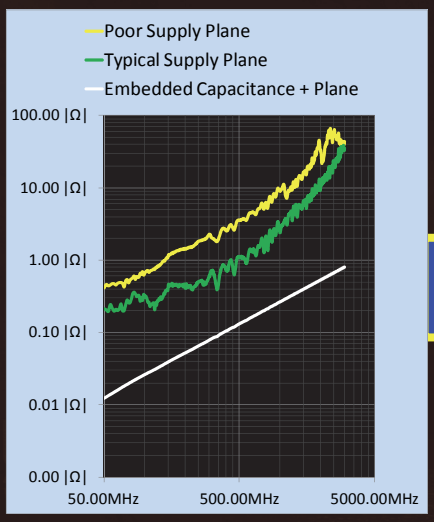
Crosstalk for Different Impedances



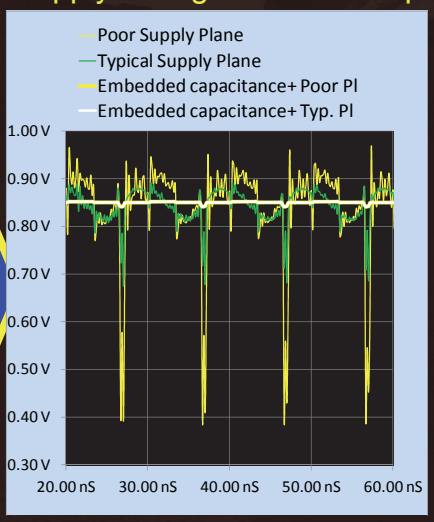
- Mainly a Supply issue (Signal impedances are fixed.)
- Low impedance needs to be on both sides, but one side helps.

Crosstalk Mitigation: Low Impedance

Supply |Z| vs. Frequency

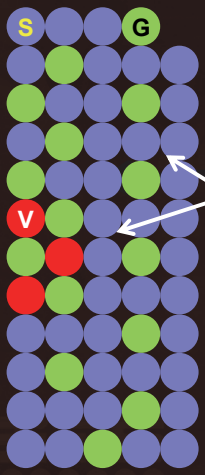


Supply Voltage Noise/ Droop

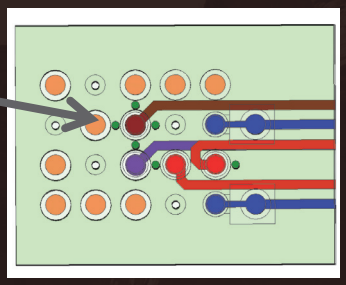


A Working Example (1 of 5)

DDR4 Pin-Out

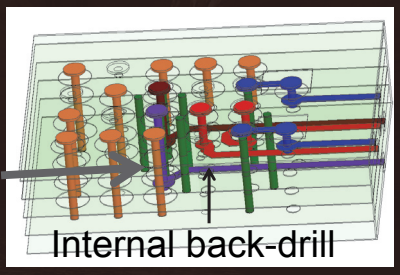


Added Ground Via, small Dia.



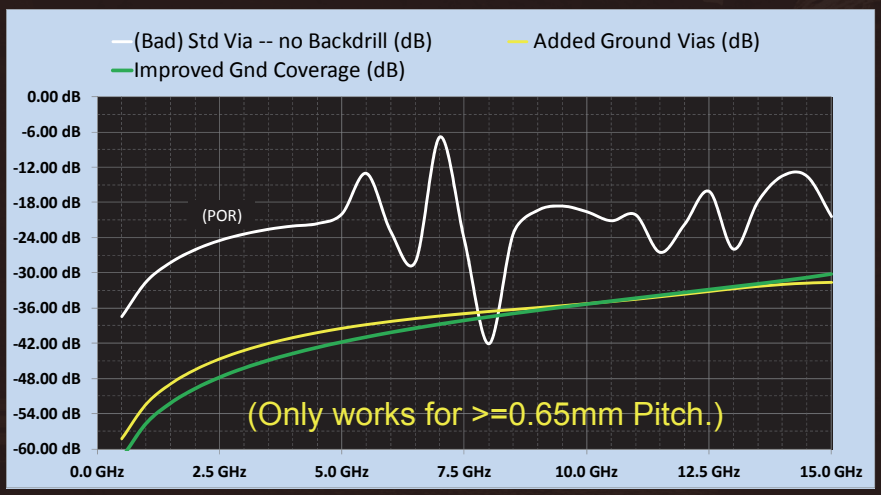
Ground Pins Compromised!

Staggered layers with smaller via

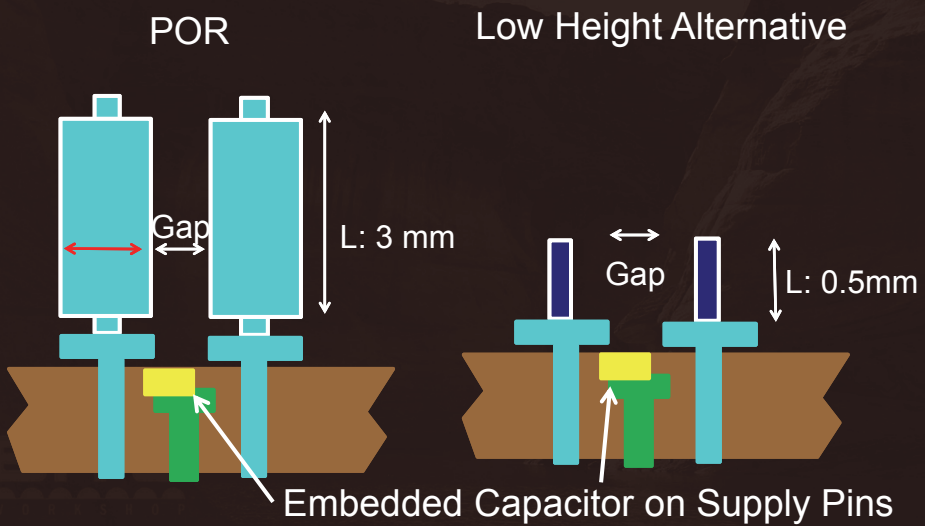


A Working Example (2 of 5)

Addition of Ground Vias Between Signals

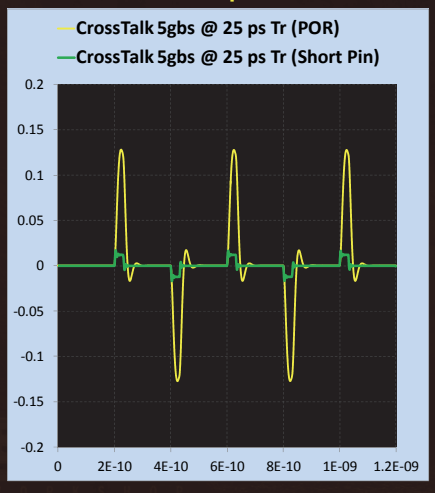


A Working Example (3 of 5)

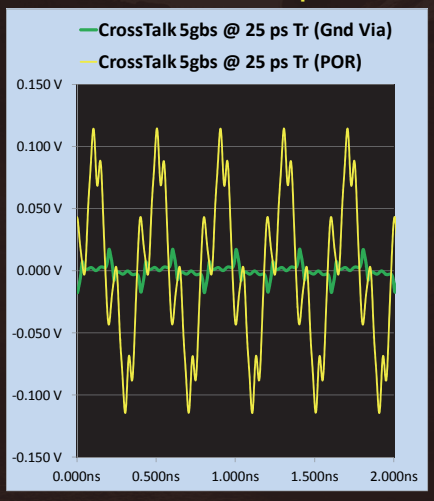


A Working Example (4 of 5)

Socket Comparison

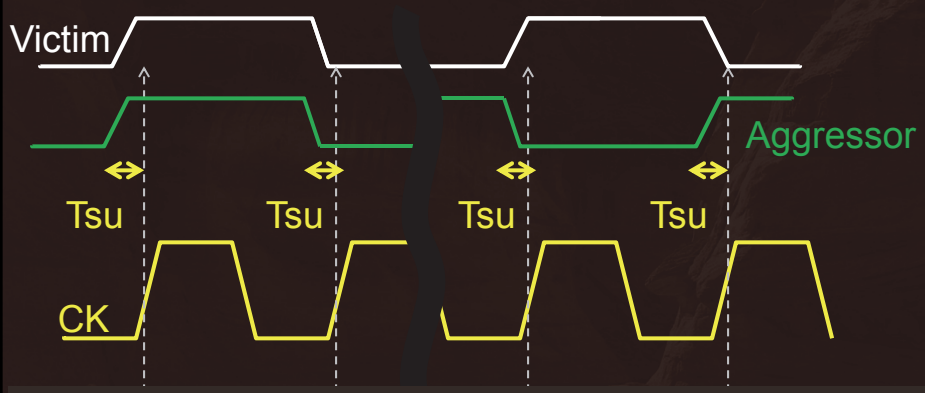


PC Board Comparison



A Working Example (5 of 5)

Results:



Measured ΔTsu matches Simulation over Distribution!

Concluding Comments

- Correcting High Speed Crosstalk in the device interface requires rework of both the socket and the connecting via.
- Both sockets and vias are far more constrained as to how to correct crosstalk, when compared to traces and launches.
- Mitigation Choices have to balance signal crosstalk (shielding, length) and power related "crosstalk" (length, low impedance).
- Working solutions are possible but requires special loadboard features as well as very short pin sockets.

Acknowledgements

R&D Altanova would like to graciously thank Freescale Semiconductor, Inc., especially: Emmanuel Del Rio, Kassem Hamze, Archana Jain, and George Ross for their patience and assistance in collecting the supporting test data for this presentation.