

**Wednesday 3/12/14 8:00am**

## **INTERCONNECTOLOGY: IT'S WHAT WE DO**

Last Year's BiTS workshop introduced the benefits from the Interconnectology approach of collaboration across the supply chain from device design to test. This session focuses on interconnect designs and advancements. As contactor design has had to evolve to address shrinking pads and decreasing pitches, there's lower contact force. The first presenter then asks whether contact pressure has become more meaningful than contact force. The second presentation details the development of long-life stamped spring probes in response to challenging technology roadmaps, all at a cost that includes maintenance and replacement costs. Next up is a paper on validation sockets (used for post-silicon validation and are quite different from test sockets). This paper brings awareness to these sockets and their challenges to encourage industry collaboration for solving future post-silicon validation interconnect challenges. The session concludes with an exploration of crosstalk sources and discusses solutions and emerging technologies, including costs, to reduce crosstalk. See? It's all about Interconnectology.

### **Long Life / Stamped Spring Probe Development**

Samuel Pak, A.J. Park—IWIN Co. Ltd.

### **Validation Interconnect Socket – Application and Future Challenges**

Ashok Kabadi—Intel Corporation

### **Crosstalk Mitigation in ATE Socket-Device Interface Boards**

Thomas P. Warwick—R&D Altanova, Inc.



This Paper

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# Validation Interconnect Socket – Application and Future Challenges

**Ashok Kabadi**



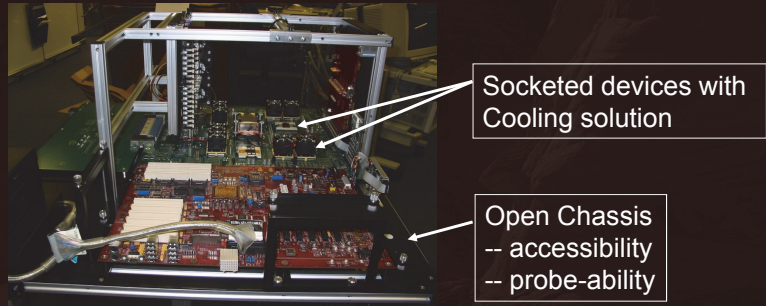
2014 BiTS Workshop  
March 9 - 12, 2014

## Content

- Validation Socket Definition
- Validation Socket Application
- Validation Socket – Key Parameters
- Future Socket Challenges
- Summary

## Validation Socket Definition

- Socket used on the “Validation Platform” to validate silicon
- Example of a typical “Validation Platform”:



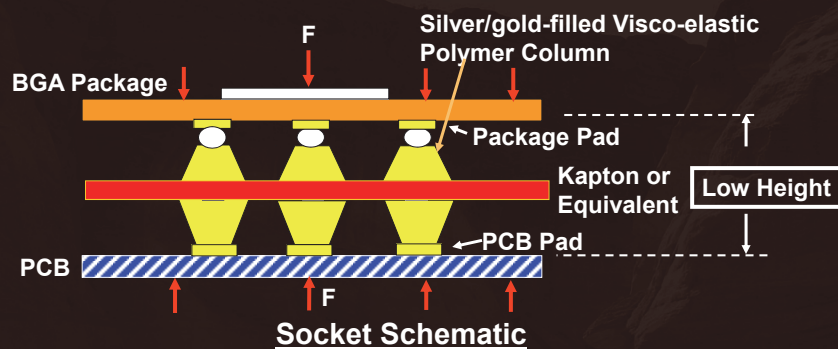
Typical Validation Platform

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## Example of Validation socket



Typical polymer-based socket

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## Application of Validation Socket

- Primarily used for internal Silicon and Platform Power-on /Volume Validation
- Highly efficient during stepping (revision) changes
- Support OEMs/ODMs for early power-on and validation

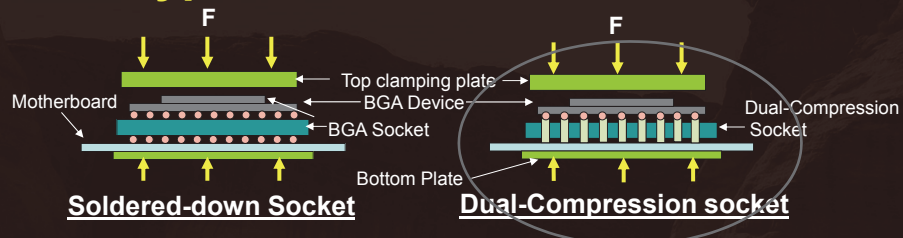
**Validation sockets save significant amount of validation time**

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## Types of Validation Socket



-- **Faster** assembly time

**Cons**

- Difficult to rework socket
- Potential **damage to expensive PCB** during socket rework
- **Damage to solder joint** during Heatsink/thermal tool attachment

**Pros**

-- **Easier** to rework  
 -- **Electrically shorter**

-- **Elaborate socket/heatsink attachment**

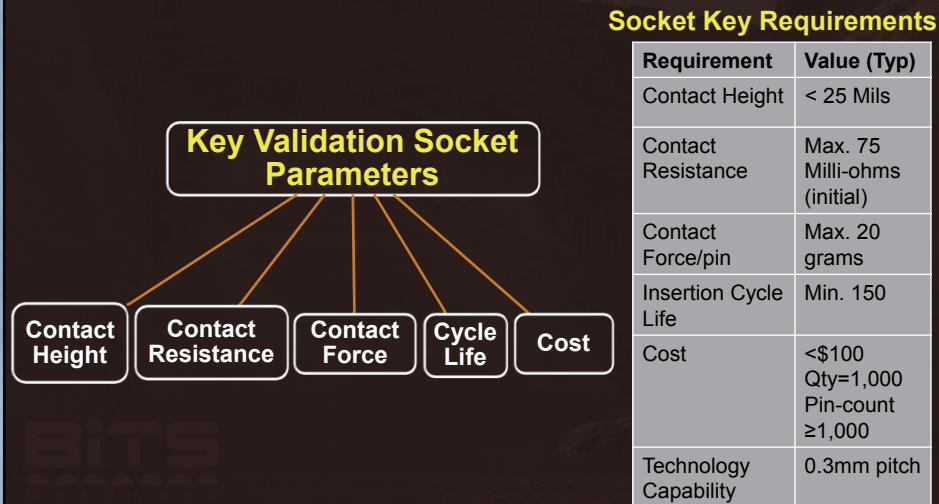
**Dual-compression socket is preferred socket for validation**

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## Socket Contact Selection Parameters



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## Validation Socket Design Challenges

1. Ball pitch at 0.4mm and trending to 0.3mm
2. Ultra thin substrates and multiple dice
3. Multiple solderball dimensions on the same package
4. PoP and M-PoP (Multi-PoP)
5. Use of sockets with “Zero Keep-out” on the board
6. High/Low temperature testing and resistance stability
7. Validation socket scope

**Significant challenges in socket design, manufacture and implementation**

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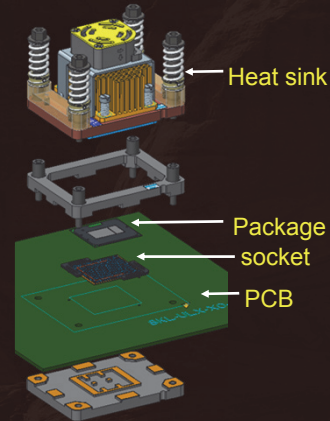
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## 1. Ball Pitch less than 0.4mm

### Challenges

- Alignment of package to socket
- Alignment of socket to PCB
- Tolerances of the features on PCB
  - Hole diameter, pad diameter, hole to pad distance, etc.
- PCB plating requirements
- Manufacture of the socket with reduced cost



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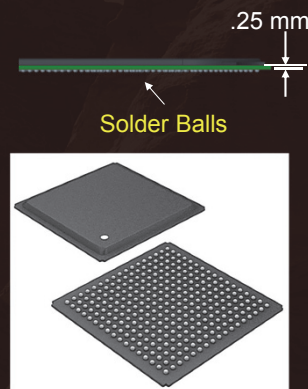
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## 2. Ultra Thin Substrate and Multiple Dice

### Challenges

- Substrate thickness reduced to .010" (.25mm)
  - Package warpage issues under load
    - Potential connectivity issues
- Multiple Dice on the same package
  - Challenges in distributing the load evenly



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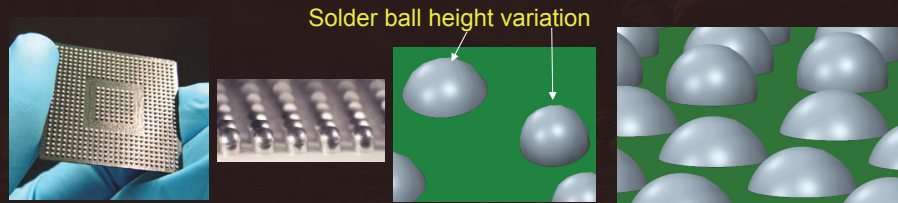
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### 3. Multiple Solder Dimensions on the Same Package

#### Challenges

- ❑ Mixed Solder Resist Openings (SROs) on the same package
  - Ball height along the outer perimeter is taller than the inner one
  - Polymer socket contact working range is small (<5mils) – potential reliability issues



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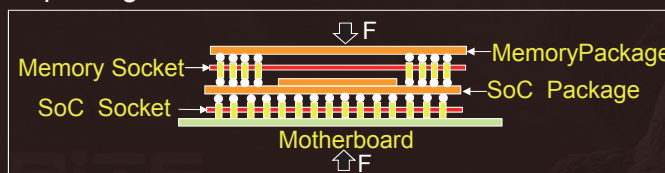
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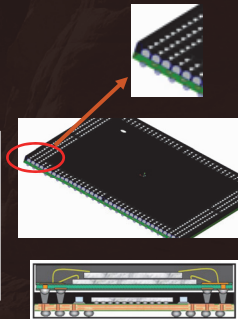
### 4. Sockets for PoP Packages

#### Challenges

- ❑ Memory socket on top of SoC socket
- ❑ Through-Mold-Interconnect (TMI) challenges
- ❑ Socket contacts that connect to balls on the bottom and top
- ❑ Pitch scaling down to .35mm for memory packages



PoP Package/Socket Schematic



Through-Mold-Interconnect

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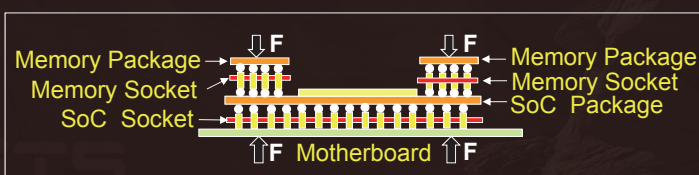
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## 4. Multi-PoP Packages

### Challenges

- Multiple sockets on top of the main socket with over 2,000 solder balls
- Alignment of memory package sockets on top of the substrate (0.4 mm pitch)
- Large force required to make connectivity



Multiple PoP Package/Socket Schematic

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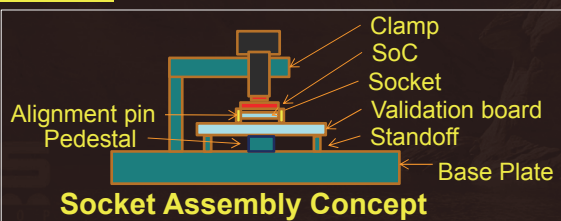
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## 5. Use of Sockets with Zero Keep-out

### Challenges

- Thickness of the board is 0.8mm – subject to warpage and deflection
- No alignment and mounting holes in the validation board due to routing constraint

#### Design Concept:



**Socket Assembly Concept**

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## 6. High Temperature Testing

### Challenges

- ❑ Socket reliability at high temperature (>70°C) and thermal cycling (0°C to 100°C)
- ❑ Polymer properties change with temperature change
- ❑ The contact resistance becomes unstable at extreme temperatures and during thermal cycling
  - Max contact resistance can go up to 250 milliohms (for 0.4mm pitch socket)
  - Need to reseat the package into the socket to achieve lower contact resistance

## 7. Validation Socket Scope

### Challenges

- More and more devices are soldered down in the final product -- Need for more validation socket designs
- Number of validation socket designs growing due to increased number of derivative products
- Validation to move to more “real world devices” (Form-Factor-Designs -- FFDs) and away from “artificial boards” (Debug and Validation Platform -- DVP)
  - Need for more innovative socket designs and hit a price point with “Zero Keep-out” sockets

## Summary

- ❑ Validation sockets play a critical role in reducing validation time
  
- ❑ Validation sockets have significant technology challenges for socketing SoC devices
  
- ❑ Need Industry help to meet challenging future validation socket requirements
  - Low height
  - “Zero Keep-out” (X and Y) – Same size as the package
  - Low cost
  - Low force
  - Dense ball pitch up to 0.3mm
  - Shorter lead time