Session 5

Tuesday 3/11/14 1:30pm

SOCKETS WITH INTEGRITY

High frequency signal and power integrity with sockets are essential to successful package testing. The opening presenter shares first-hand experience pairing the design of a high-speed load board with sockets of the desired bandwidth to avoid significantly reduced system performance. The second paper assesses power and ground performance through an examination of signal and power routings and the corresponding ground return paths for a PCB/socket combination. The next presenter looks at how ever shrinking devices with more functionality and higher density I/Os bring sensitive signal lines closer together, contributing to signal integrity issues. The paper closing this session discusses the impact on test hardware with the high-speed digital device world's leap to 28 Gbps Serdes. The presenter will describe what worked at 10 Gbps, what still works for 28 Gbps, and what might be changed and/or optimized to reach test speeds of 28 Gbps.

High Bandwidth Sockets For SERDES Applications On ATE Load Boards
Don Thompson—R&D Altanova

This Paper

Signal and Power Integrity Impact of Ground Slugs in Sockets
Gert Hohenwarter—GateWave Northern, Inc.

Building Blocks and Predictors for Good Contactor Signal Integrity
Jeff Sherry—Johnstech International

Signal and Power Integrity Impact of Ground Slugs in Sockets

Gert Hohenwarter
GateWave Northern, Inc.

2014 BiTS Workshop
March 9 - 12, 2014

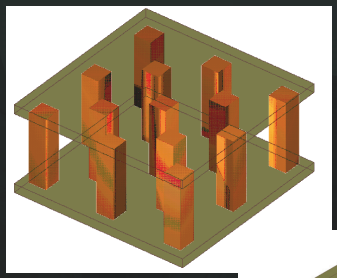
Objectives

- Examine impact of ground slugs on RF performance
  - Insertion loss
  - Return loss
  - Eye diagram
  - Crosstalk
- Examine impact of ground slugs on PDS performance
  - Loop inductance
  - Noise

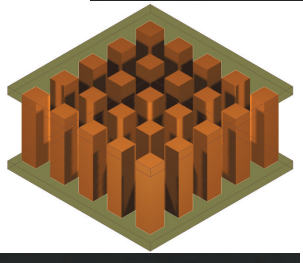
Approach

- Provide slug example
  - Inductance
  - Resistance
- Use 3D field simulations (HFSS) to generate relevant parameters for PCB/socket/slug combined circuit analysis (HyperLynx)
  - S21, S11, crosstalk, noise
- Use SPICE for PDS noise and impedance performance assessment

A slug ?

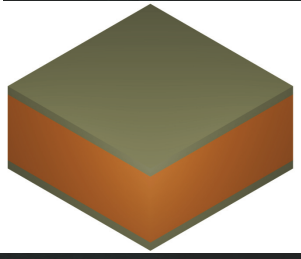


'reduced'



'5x5' - 0.5 mm pitch

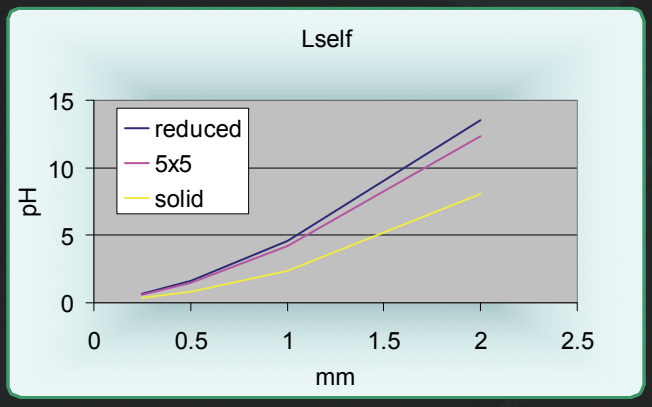
'solid'



Slugs can be composed in many ways…

Self-inductance

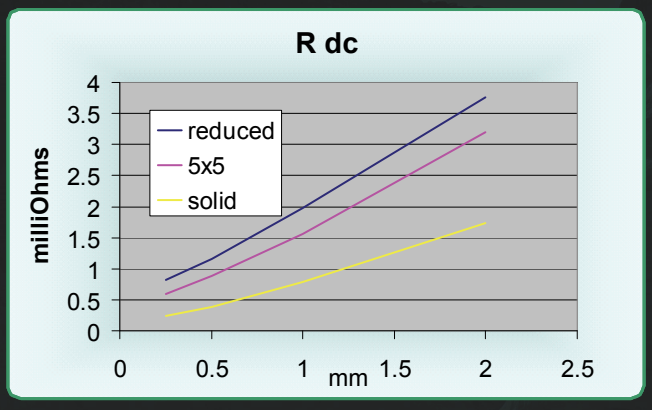
as a function of slug thickness



Is it worth 'stuffing' the socket with pins?

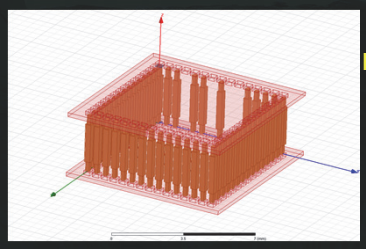
Resistance

as a function of slug thickness



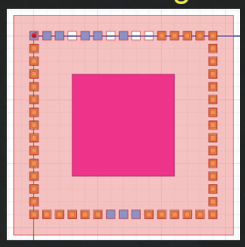
Don't forget R in a PDS analysis…

Socket with slug

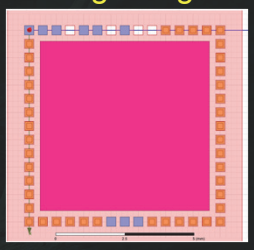


no slug

small slug

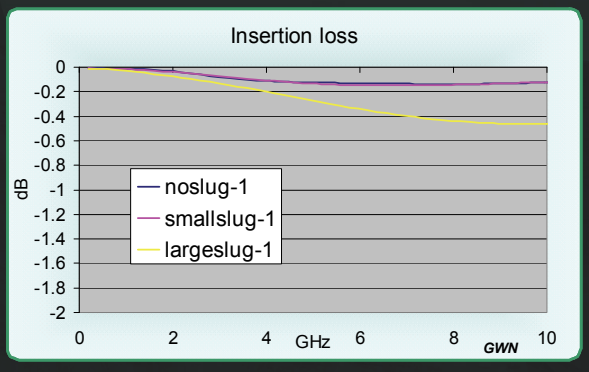


large slug



QFN style socket model

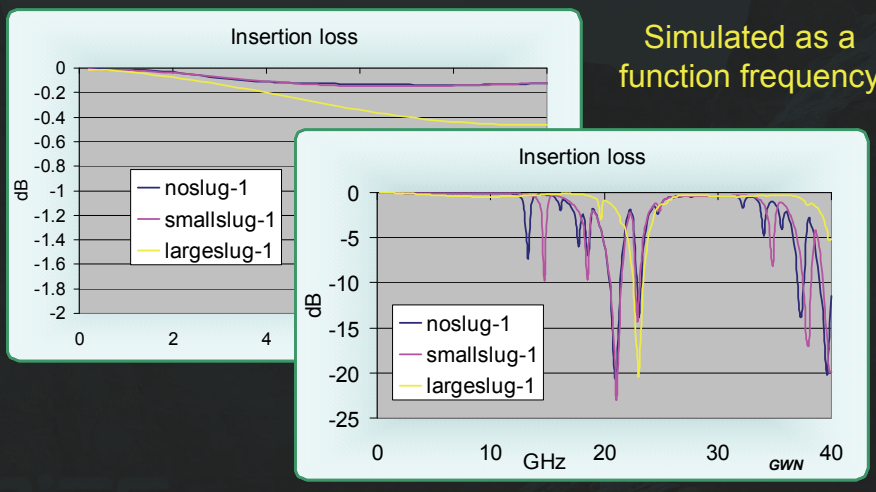
Insertion loss



Simulated as a function frequency

At low frequencies a large slug makes matters worse

Insertion loss



Simulated as a function frequency

At low frequencies a large slug makes matters worse

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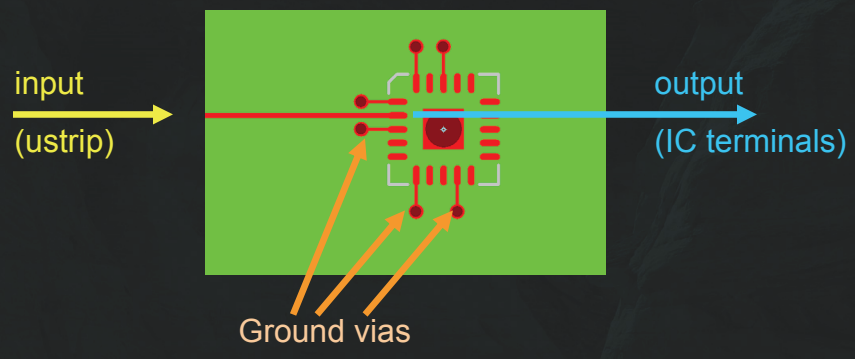
Socket with slug and PCB



Example uses actual QFN style socket on PCB

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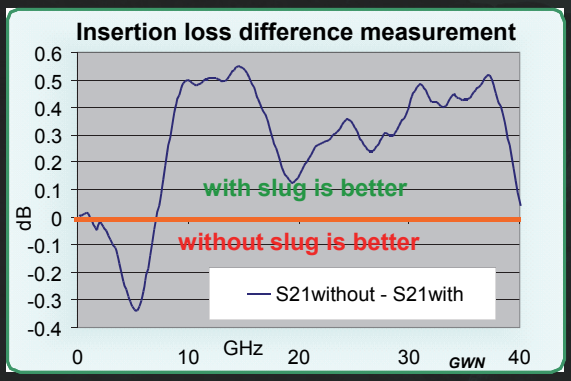
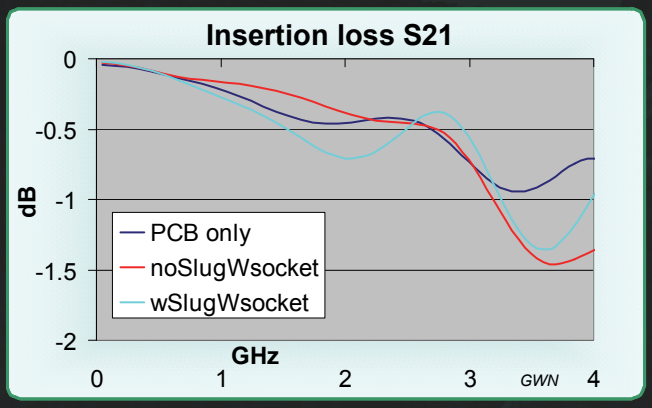
Measured insertion loss difference



Measured on a QFN style socket (without PCB)

Insertion loss

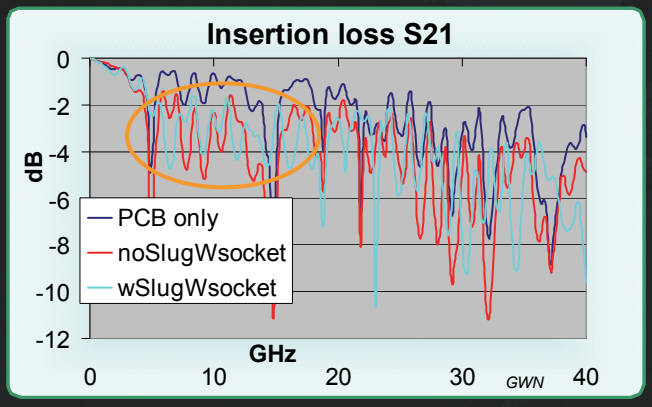
Simulated as a function frequency



PCB with and without socket present

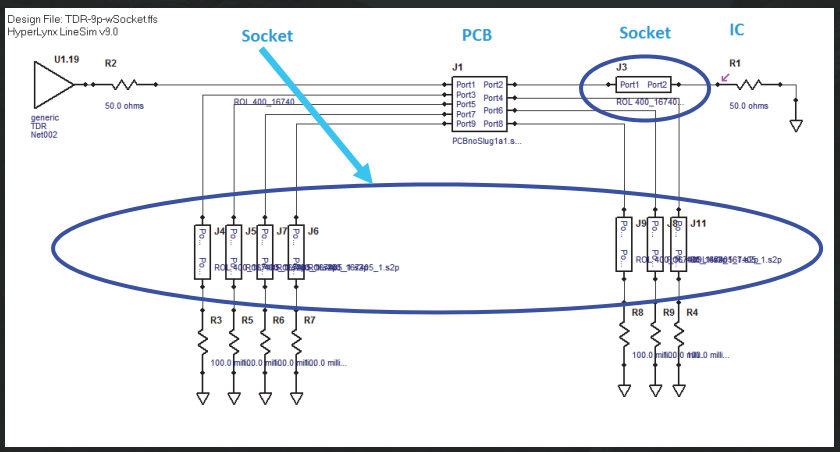
Insertion loss

Simulated as a function frequency



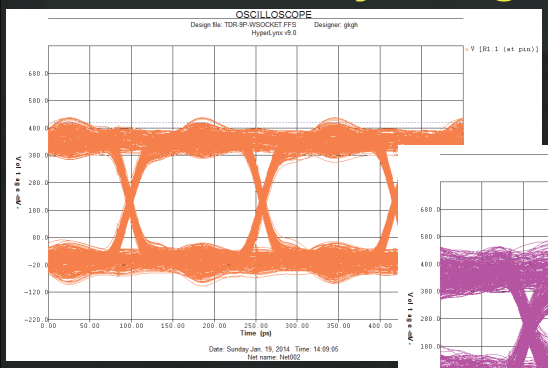
Socket contributions become significant at higher frequencies

Circuit diagram for models



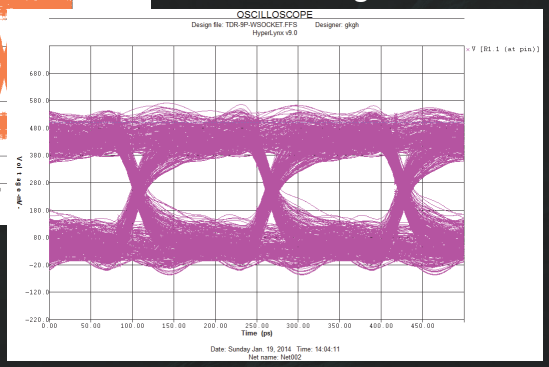
Equivalent circuit used
(measured socket parameters combined with simulated PCB)

Eye diagrams



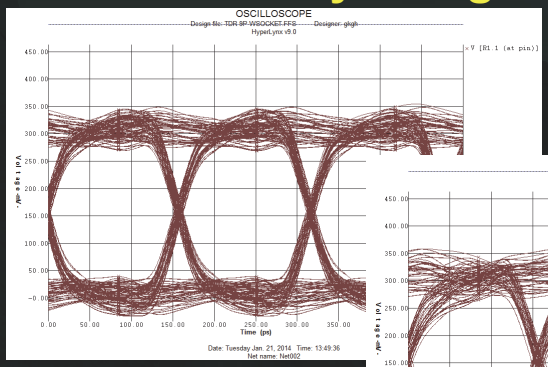
With slug

No slug



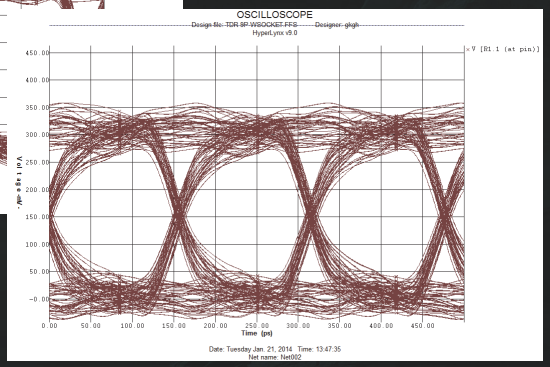
6.25 GB/sec with socket – <45 Ohm ustrip

Eye diagrams



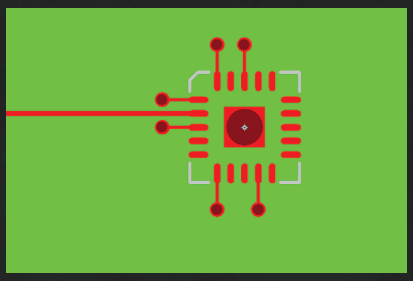
With slug

No slug

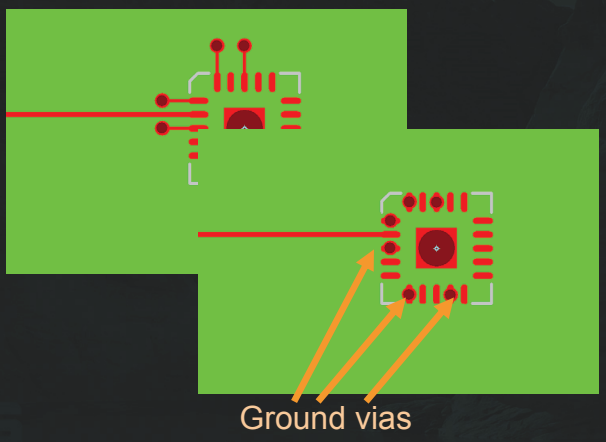


6.25 GB/sec with socket – 50 Ohm ustrip

What can be done to improve design ?

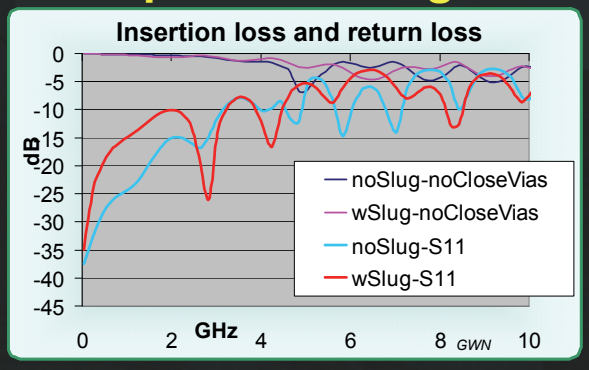


What can be done to improve design ?

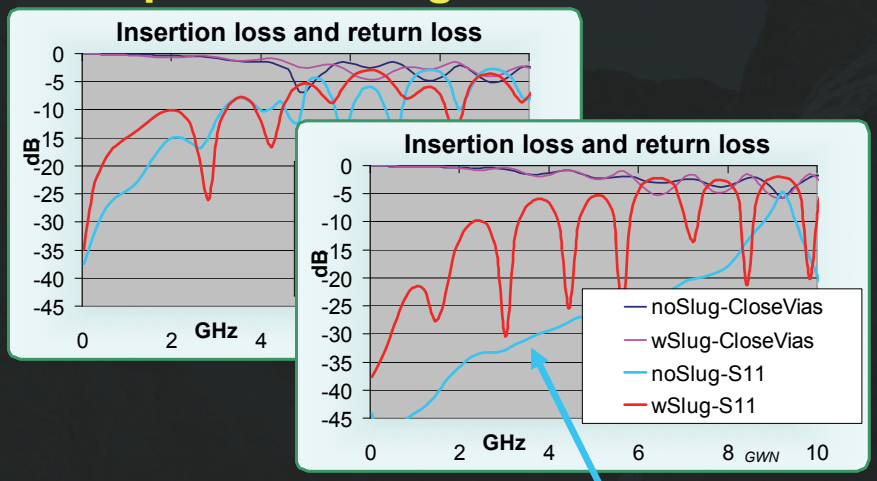


Move ground vias closer to IC pads

Impact of change on return loss

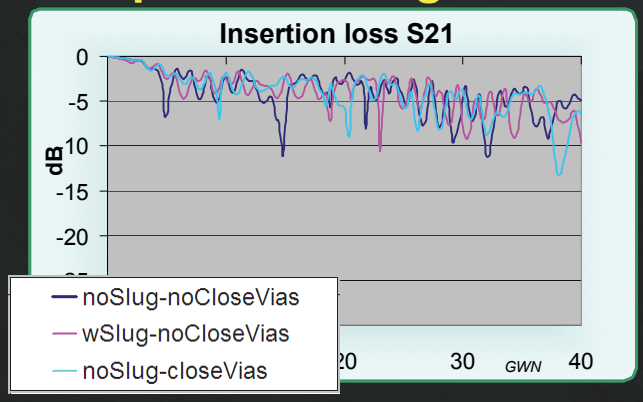


Impact of change on return loss

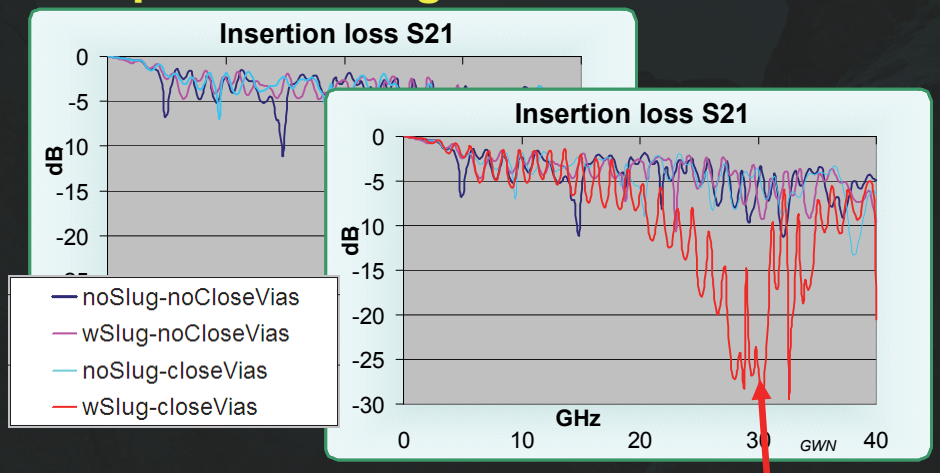


In this case the closer vias improve return loss high frequency performance - best case is 'no slug'

Impact of change on insertion loss



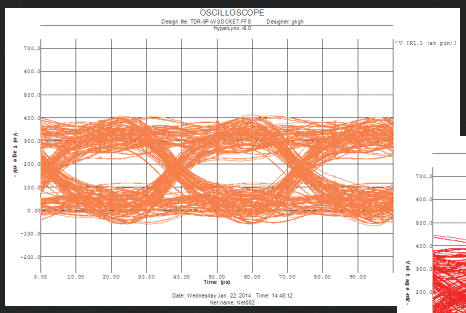
Impact of change on insertion loss



In this case the change negatively impacts insertion loss high frequency performance if a slug is present

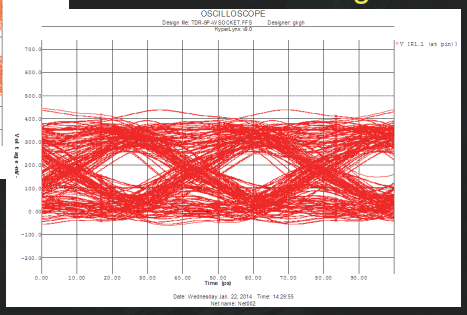
Eye diagrams at 28 GB/s

'close vias'



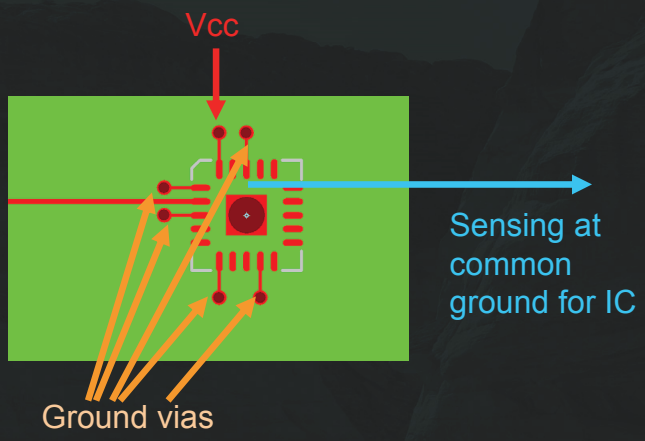
Without slug

With slug



Eye diagram shows how a 28 GB/s PRBS is affected by the insertion loss drop

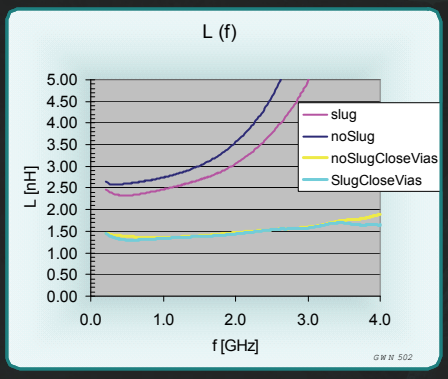
PDS examination



A power plane is assumed right under the ustrip ground plane in the PCB

Loop Inductance

Vcc- Ground

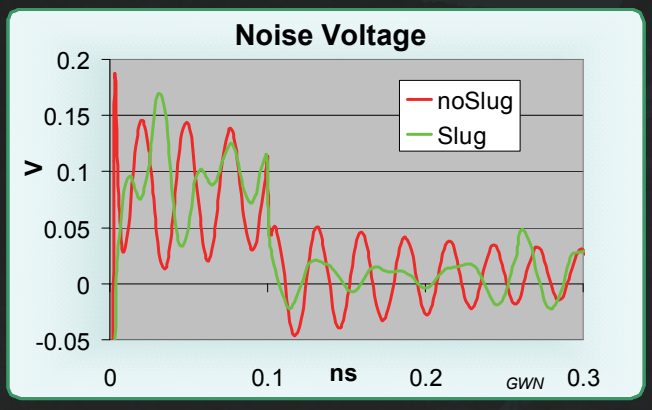


Loop inductance is orders of magnitude above self inductance of the slug

Simulation of PCB plus socket

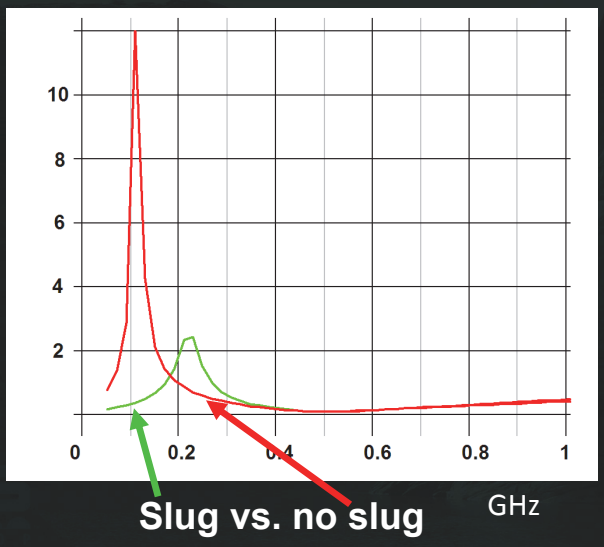
(socket and PCB make a significant contribution to inductance)

AC noise from step current



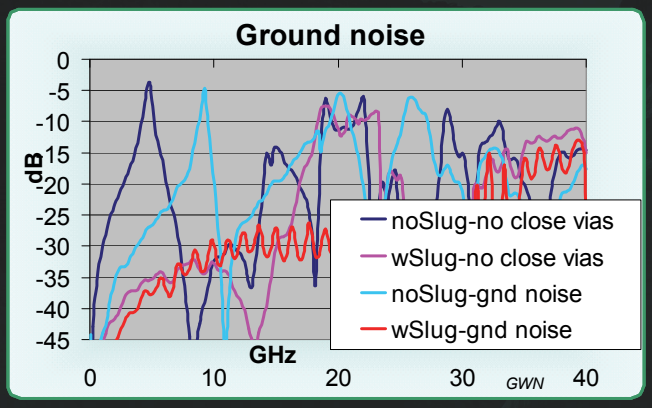
100 mA step excitation at Vcc

Impedance as a function of frequency



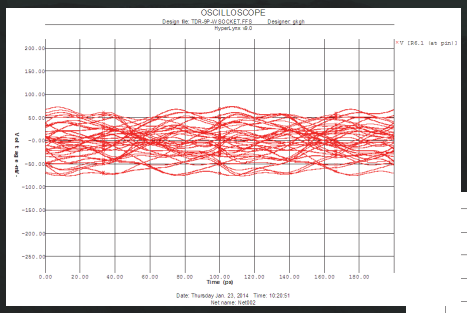
Impact of slug/vias on ground noise

Measured at one of the ground vias

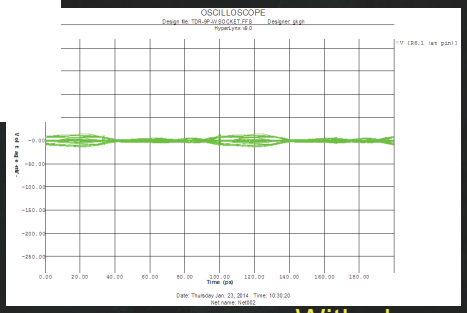


In this case close vias improve ground noise levels at lower frequencies

Noise from PRBS at 10 GB/s



Without slug



With slug

Vcc drive, gnd monitor

Conclusion

- **Ground inserts generally improve power delivery quality and reduce loop inductance**
- **Ultra-low (self-) inductance requirements should be seen in context of overall PCB design and must be carefully assessed to prevent overdesign**
- **Signal integrity should be carefully monitored during the design phase as it will not automatically improve with use of a ground slug**