FIFTEENTH ANNUAL BiTS 2014
Burn-in & Test Strategies Workshop

Session 5

Tuesday 3/11/14 1:30pm

SOCKETS WITH INTEGRITY

High frequency signal and power integrity with sockets are essential to successful package testing. The opening presenter shares first-hand experience pairing the design of a high-speed load board with sockets of the desired bandwidth to avoid significantly reduced system performance. The second paper assesses power and ground performance through an examination of signal and power routings and the corresponding ground return paths for a PCB/socket combination. The next presenter looks at how ever shrinking devices with more functionality and higher density I/Os bring sensitive signal lines closer together, contributing to signal integrity issues. The paper closing this session discusses the impact on test hardware with the high-speed digital device world's leap to 28 Gbps Serdes. The presenter will describe what worked at 10 Gbps, what still works for 28 Gbps, and what might be changed and/or optimized to reach test speeds of 28 Gbps.

This Paper

High Bandwidth Sockets For SERDES Applications On ATE Load Boards
Don Thompson—R&D Altanova

Signal and Power Integrity Impact of Ground Slugs in Sockets
Gert Hohenwarter—GateWave Northern, Inc.

Building Blocks and Predictors for Good Contactor Signal Integrity
Jeff Sherry—Johnstech International

High Bandwidth Sockets For SERDES Applications On ATE Load Boards

Don Thompson
R&D ALTANOVA

2014 BiTS Workshop
March 9 - 12, 2014

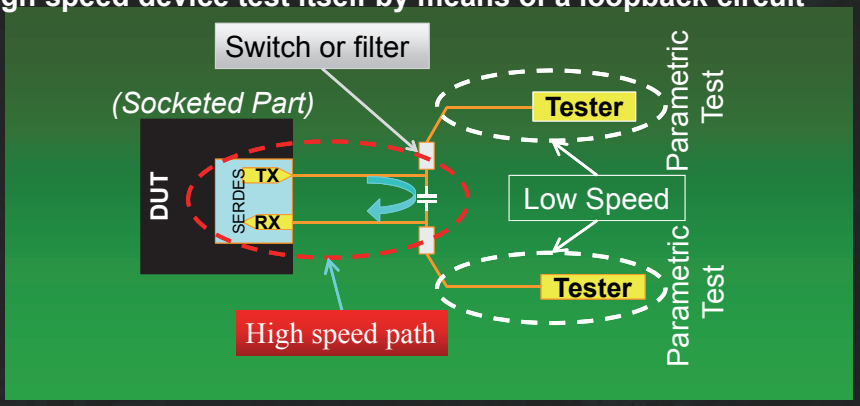
The Story:

While designing a high speed SERDES test circuit, we discovered the most limiting part of the design was not the load board, but the socket

This is a story that shows the importance of good socket performance in a design and dives into understanding the signal integrity aspects of socket design

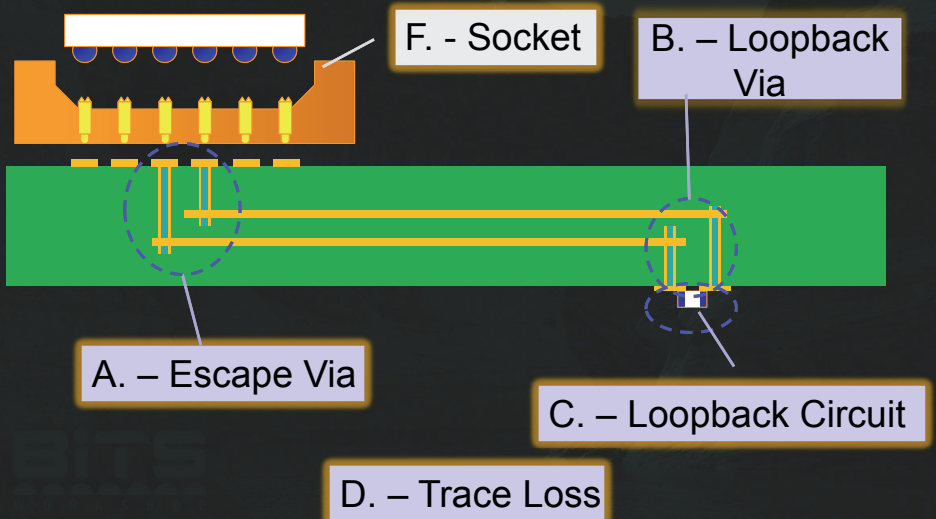
Typical SERDES Test Circuit

Loopback Circuit – Testers can not economically go up to the speeds of today's high speed SERDES, so it is typical to have a high speed device test itself by means of a loopback circuit



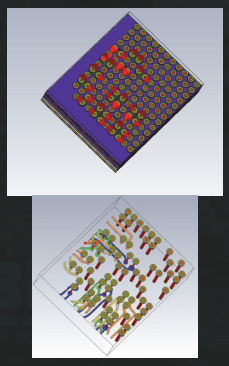
Load Board speeds for SERDES Channels are now often 28Gbps

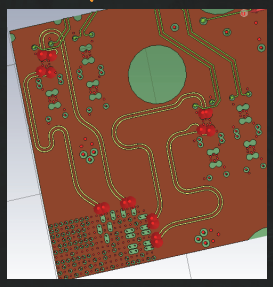
SI Challenges To The SERDES Design

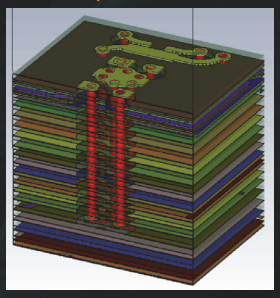


Modeling Snapshot

- Modeling as broken up into different parts, DUT Escape, Trace, and Loopback

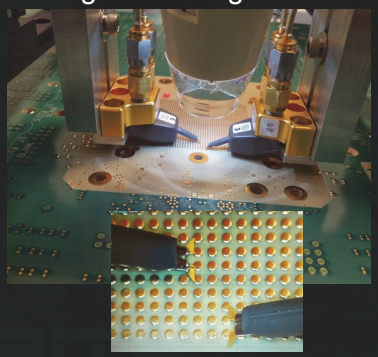




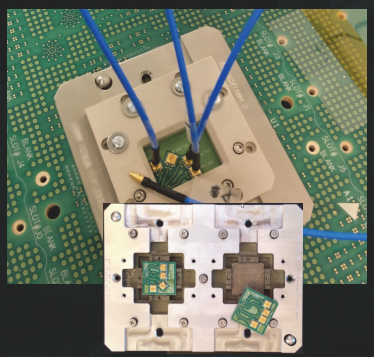


Validating The Design

Once the design is completed we need to verify performance. Using a VNA we have two different methods of measuring the performance of the board:
1.Micropositioner Probe
2.Surrogate Package

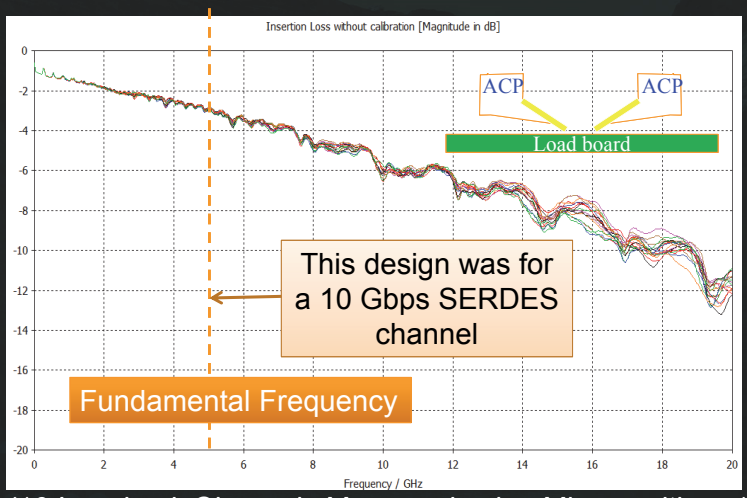


Micropositioner Probe (measures Board only)



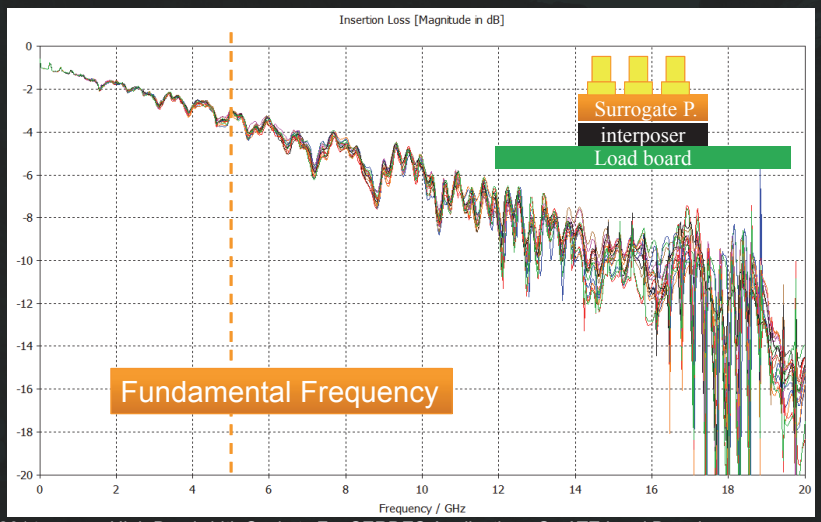
Surrogate Package (measures Board + Socket)

Board Differential Insertion Loss ($S_{dd}21$)

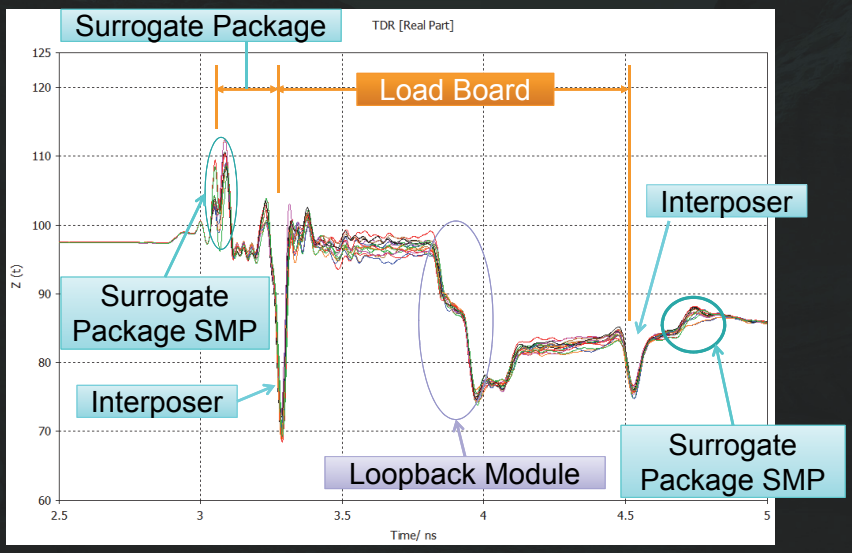


(16 Loopback Channels Measured using Micropositioner)

Board + Socket Differential Insertion Loss ($S_{dd}21$)



TDR from Surrogate Package

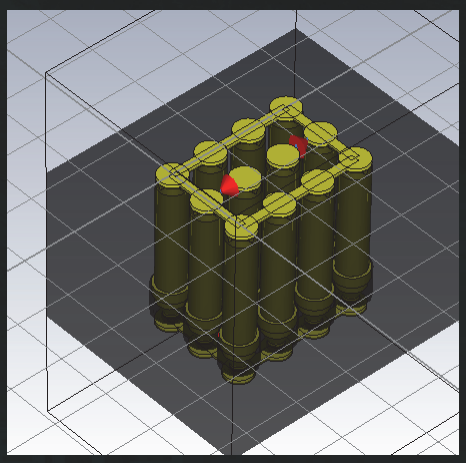


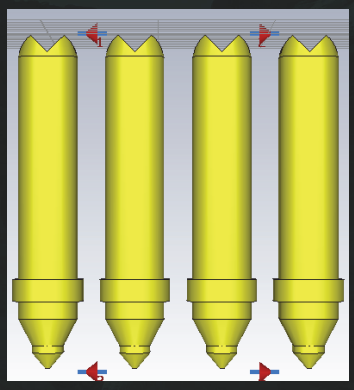
Analysis

- Interposer capacitance causes significant ripples in insertion loss due to it's capacitance

Let's figure out why the socket is causing problems!

Initial Design: 1mm Pitch Interposer





Simulated in Compressed State

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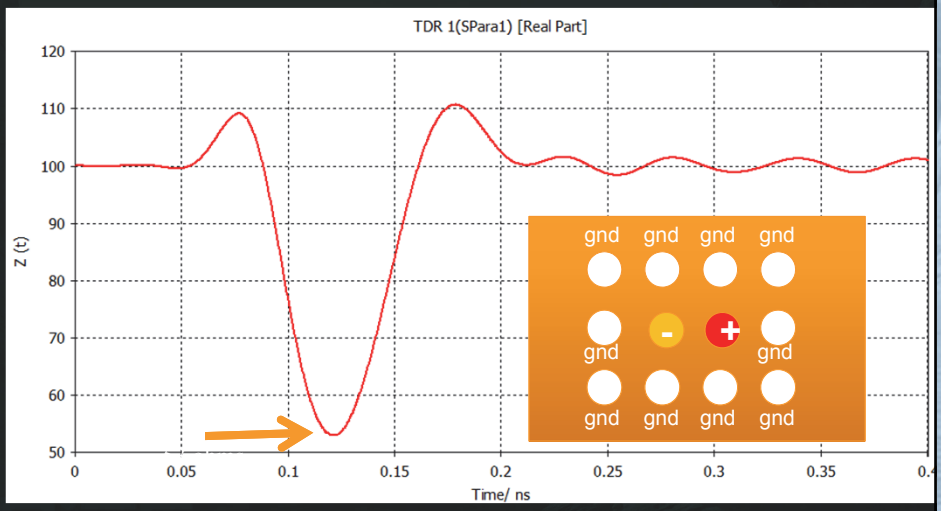
Differential TDR (Simulated)



It's confirmed that the basic design of the socket is causing our impedance problems! We need a new interposer!

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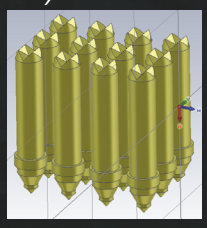
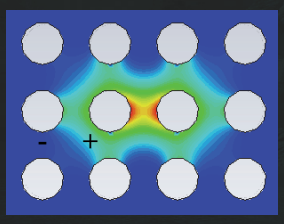
HOW TO GET A 100 OHM INTERPOSER

Interposer Impedance Explained

1. Impedance $= \sqrt{\frac{\text{Inductance}}{\text{Capacitance}}}$
2. Inductance is a function of the pin diameter (inversely proportional)
3. Capacitance is a function of ground metal to signal metal AND dielectric material *(Combination of pitch, pin diameter, and dielectric material)*





Differential impedance in a pin field

Impedance "Tuning" Design Tools

IN A TYPICAL DESIGN:

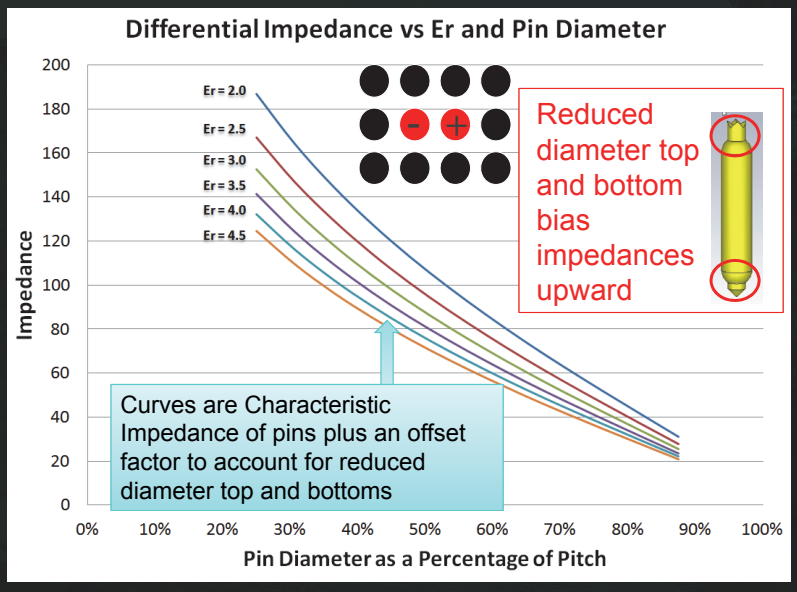
We **can't** change:
- Pin Pitch
- Pin out

We **can** change:
- Pin Diameter (By selecting an alternate pin)
- Dielectric Material of socket

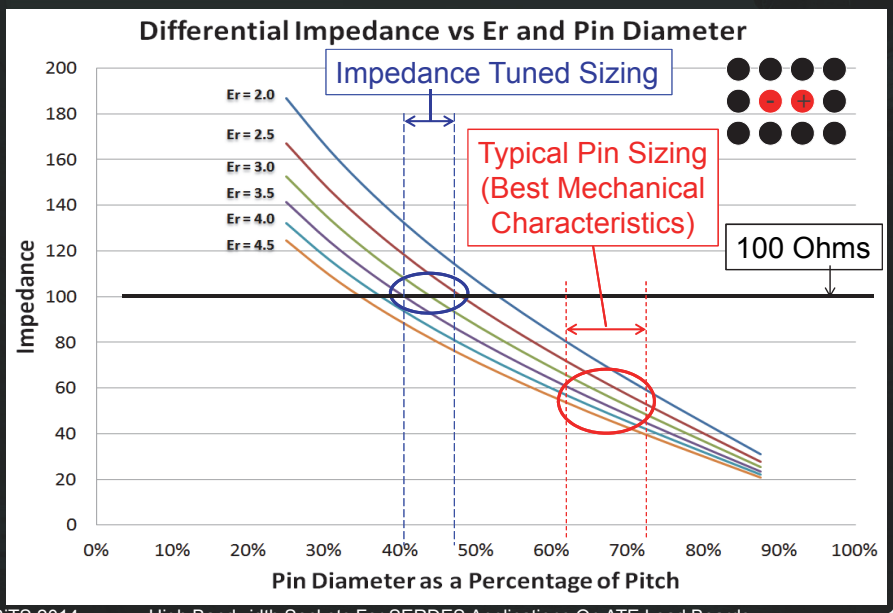
Therefore

If Too Capacitive	If Too Inductive
Reduce Pin Diameter	Increase Pin Diameter
Reduce Dielectric Constant (Er)	Increase Dielectric Constant (Er)

Spring Pin Differential Impedance Chart



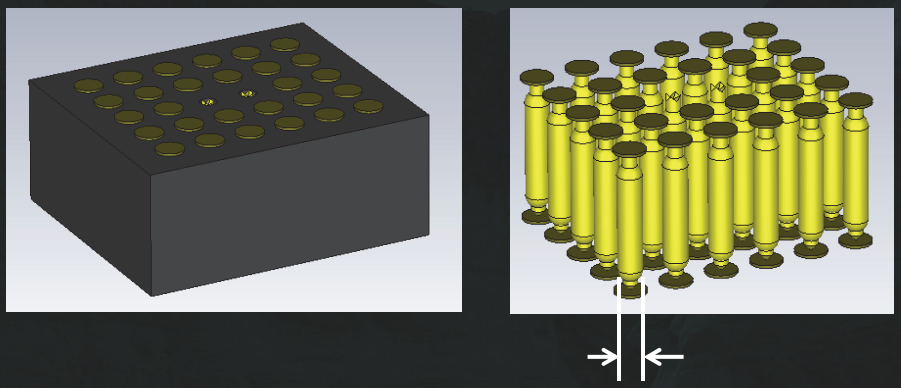
Spring Pin Diff Impedance Tuning



Caveats

- Analysis shown is good to a 1st order approximation. Actual sockets will vary depending on air cavities, geometric nuances, etc. For best results use a 3D field solver.
- Air cavities will affect your dielectric constant. If you have significant air cavities average the dielectric constant of air (Er=1) with the volume of dielectric to determine your socket equivalent dielectric to use the chart.
- When selecting your socket you MUST take into account other design requirements and they must be balanced against your high performance needs. (Low inductance pins for power, crosstalk requirements, etc.)

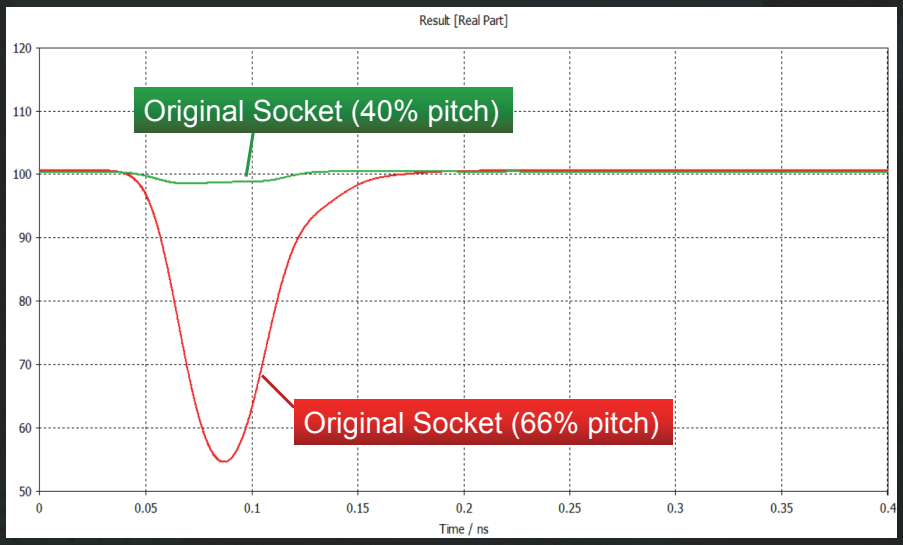
Select An Alternate Pin To Use



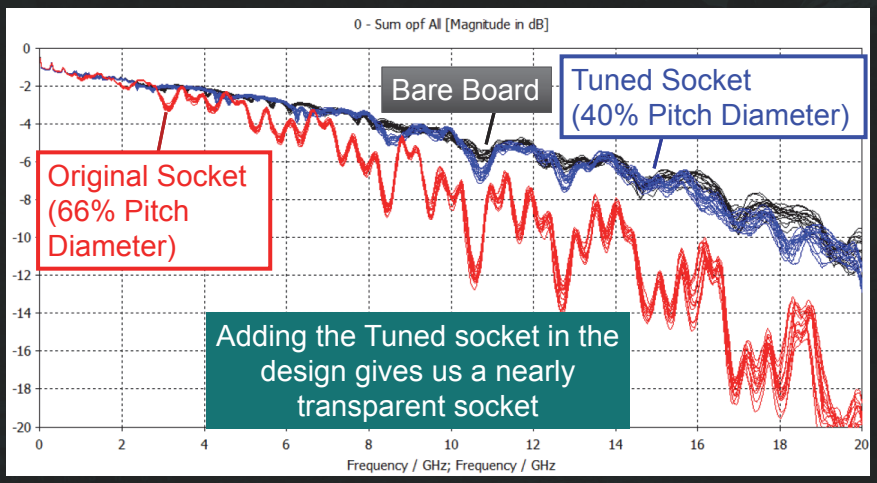
Select a pin diameter that's 40% pitch

And simulate results….

TDR Simulated



Factoring This Back Into The Design



Conclusions

- Sockets must be included in ATE channel performance solutions
- Standard spring pin sockets can be tuned to work at high speeds at the cost of mechanical metrics and electrical metrics (manufacturability, reliability, cycle life, and pin cost)
- Bandwidth is a function of pitch, pin size, and your dielectric material