Session 4

Tuesday 3/11/14 11:00am

THE MARKET IS OPEN

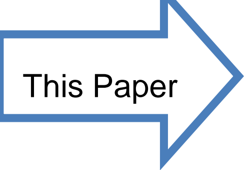
The BiTS Workshop just wouldn't be the BiTS Workshop without at least one presentation on the test and burn-in marketplace. In this year's three presentations, first we'll hear about the technical and market forces that are shaping the future of test and burn-in, particularly the challenges of industry cycles with the never ending quest for reduced costs. Next up will be our own Fred Taber, with his fourth annual Socket Report on the size of the market, whether its shrinking or growing, and companies that are leading the charge. This session's final paper hones in on a market technology trend with one innovative high-density package-on-package (PoP) solution requiring test hardware to accommodate fine pitch wire-tip interconnects. Socket and test hardware development and verification studies are underway to take this technology to high volume manufacturing.

The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets

John West—VLSI Research, Inc.

Socket Marketplace Report

Fred Taber—Taber Consulting



Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

Rajesh Katkar, Rey Co, Wael Zohni—Invensas Corporation

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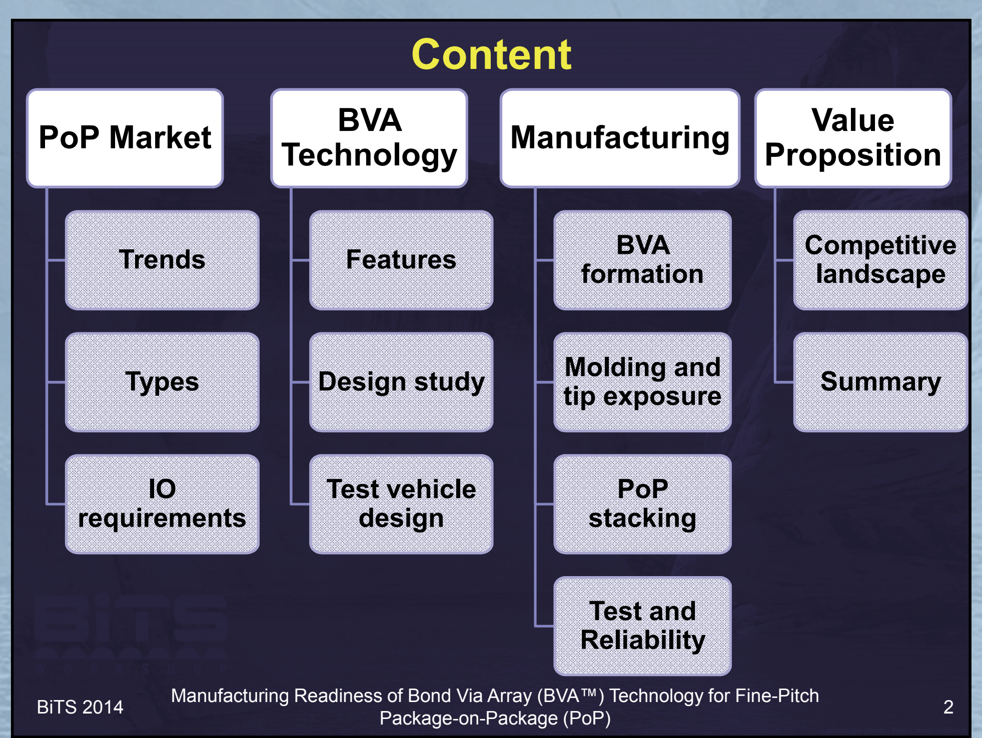
Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

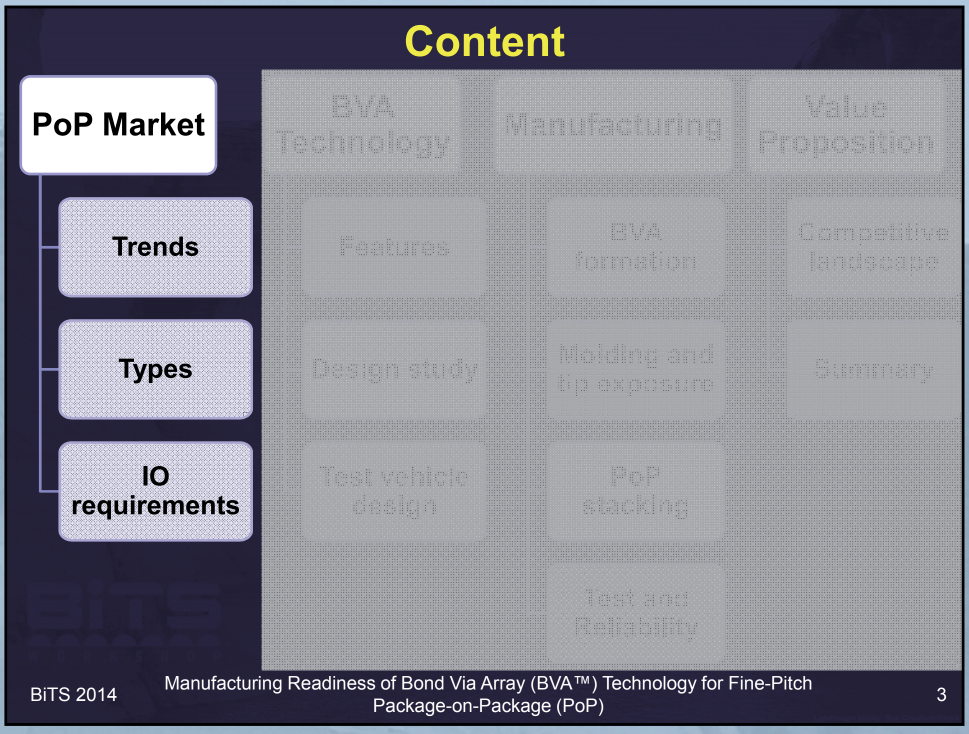
Rajesh Katkar*, Rey Co, Wael Zohni

Invensas

2014 BiTS Workshop

March 9 - 12, 2014

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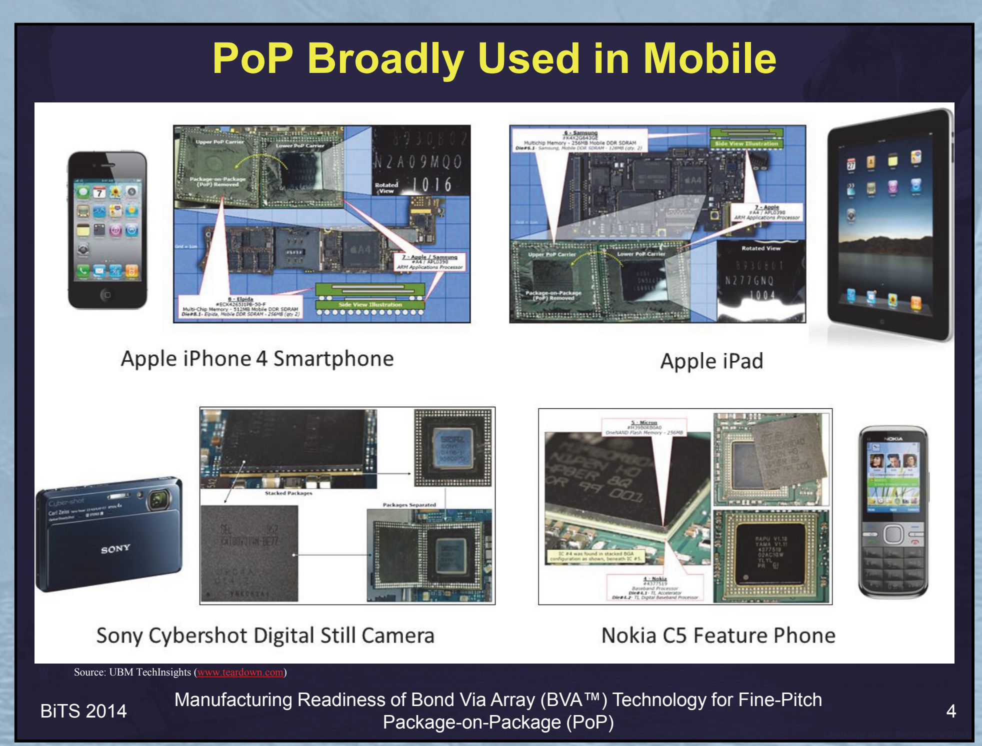
PoP Broadly Used in Mobile
Apple iPhone 4 Smartphone
Apple iPad
Sony Cybershot Digital Still Camera
Nokia C5 Feature Phone
Source: UBM TechInsights (www.teardown.com)
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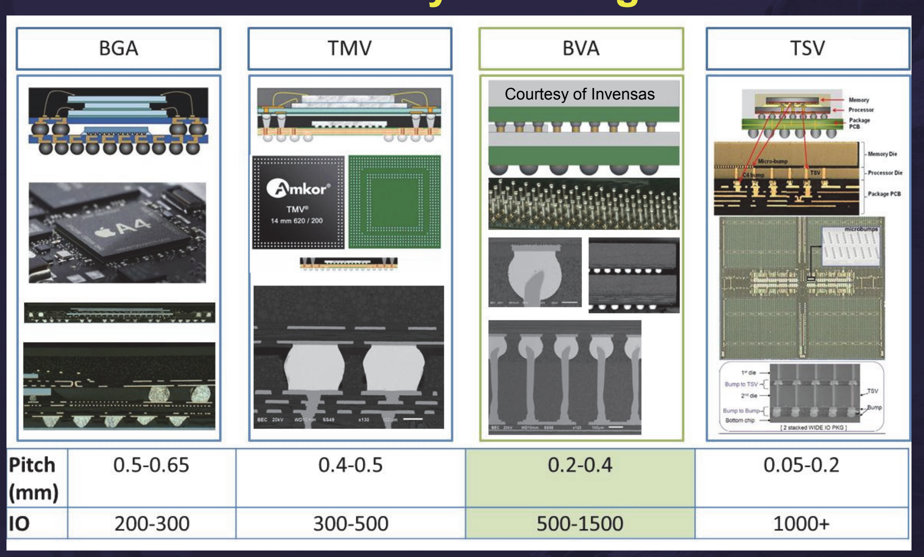
Processor-Memory Stacking Solutions



	BGA	TMV	BVA	TSV
Pitch (mm)	0.5-0.65	0.4-0.5	0.2-0.4	0.05-0.2
IO	200-300	300-500	500-1500	1000+

- BVA offers the advantages of TSV while utilizing existing packaging materials

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BVA PoP: Wide-IO Support without TSV

	2010	2011	2012	2013	2014 2015	2016?
Mobile DRAM	LPDDR	LPDDR2		LPDDR3 Emerging	Wide IO	Wide IO
Packaging	PoP	PoP	PoP	PoP	BVA PoP	TSV
Mobile processor to memory interconnect	168	168	240	240	IO ranging from 200 to 1000+	1200
Clock Speed (MHz)	400	533		800	High IO offers high bandwidth at low speed	200
Power	2X	1X		0.8X	Enables intermediate power reductions	0.5X
# of Channels	Single	Single	Dual	Dual	Quad+	Quad+
Bandwidth (GB/s)	1.6	4.2	8.5	12.8	≥25.6	≥25.6

- Wide IO provides order of magnitude increase in IO
- Wide IO implementation with TSV is not expected soon
- Bond Via Array (BVA) can offer wide IO using current infrastructure

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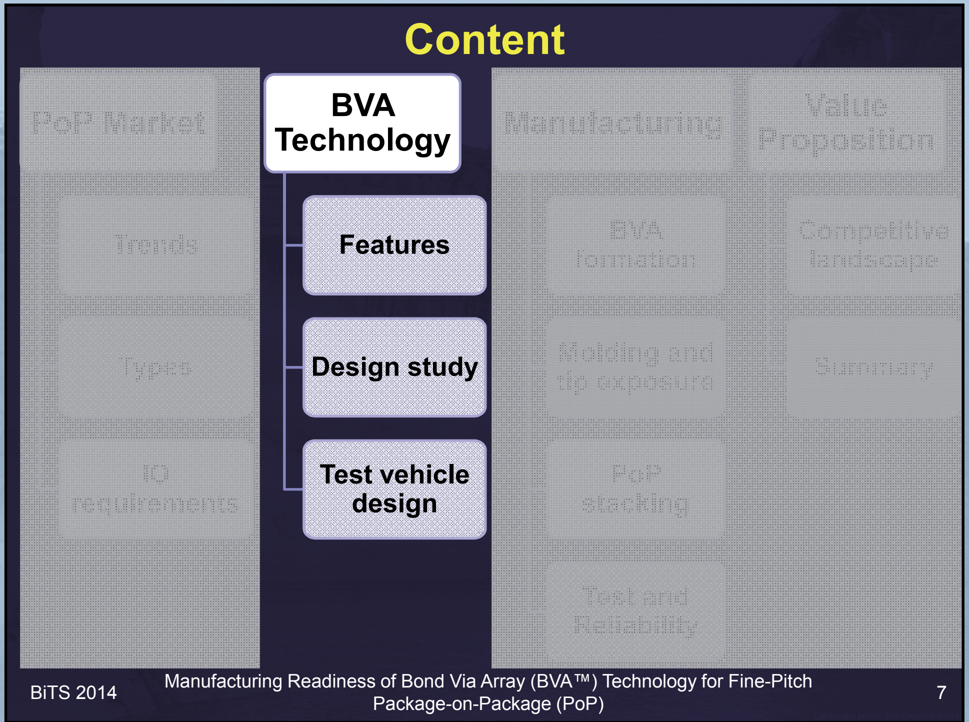
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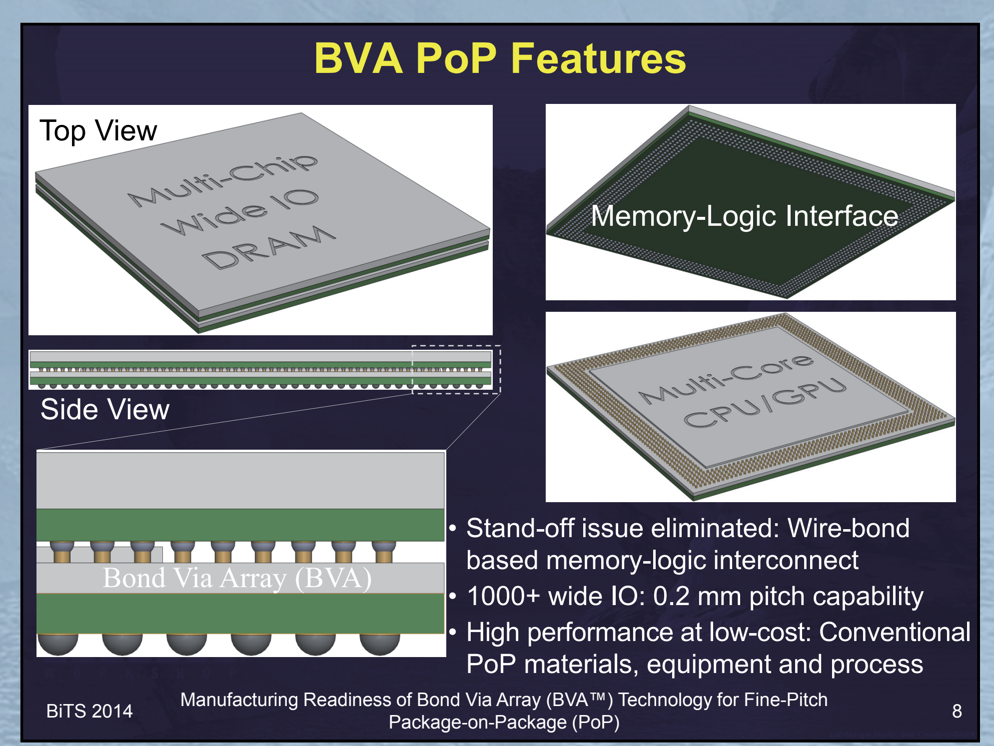
BVA PoP Features
Top View
Multi-Chip Wide IO DRAM
Memory-Logic Interface
Side View
Multi-Core CPU/GPU
Bond Via Array (BVA)
• Stand-off issue eliminated: Wire-bond based memory-logic interconnect
• 1000+ wide IO: 0.2 mm pitch capability
• High performance at low-cost: Conventional PoP materials, equipment and process
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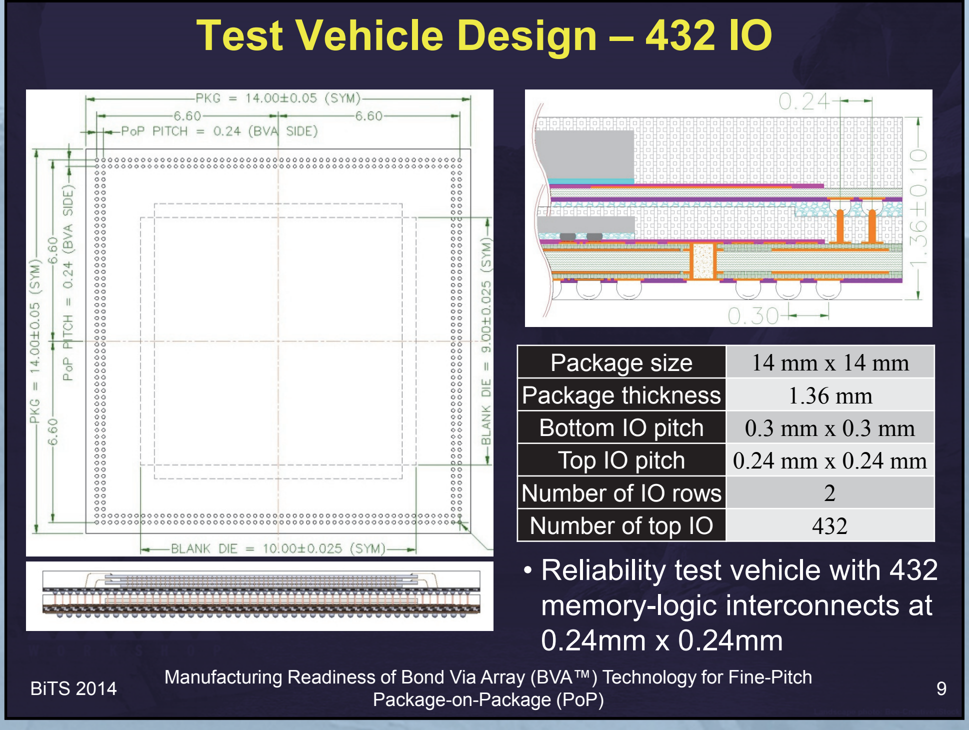
Test Vehicle Design – 432 IO
PKG = 14.00±0.05 (SYM)
6.60
6.60
PoP PITCH = 0.24 (BVA SIDE)
BLANK DIE = 10.00±0.025 (SYM)
BLANK DIE = 9.00±0.025 (SYM)
0.24
0.30
1.36±0.10
Package size
14 mm x 14 mm
Package thickness
1.36 mm
Bottom IO pitch
0.3 mm x 0.3 mm
Top IO pitch
0.24 mm x 0.24 mm
Number of IO rows
2
Number of top IO
432
• Reliability test vehicle with 432 memory-logic interconnects at 0.24mm x 0.24mm
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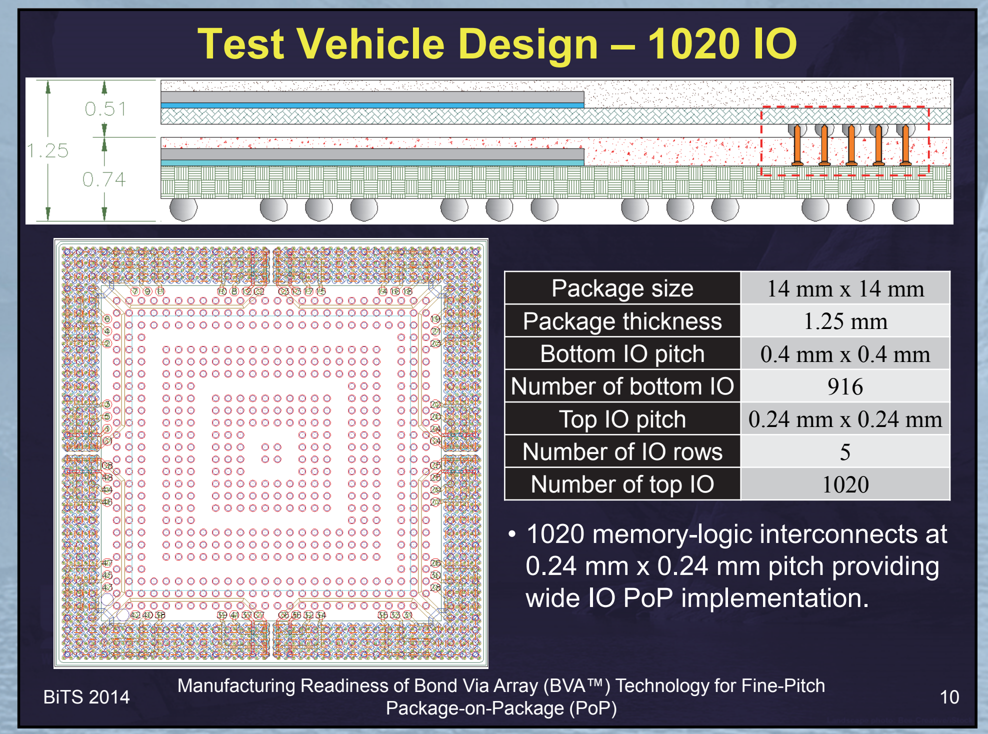
Test Vehicle Design – 1020 IO
0.51
1.25
0.74
Package size
14 mm x 14 mm
Package thickness
1.25 mm
Bottom IO pitch
0.4 mm x 0.4 mm
Number of bottom IO
916
Top IO pitch
0.24 mm x 0.24 mm
Number of IO rows
5
Number of top IO
1020
• 1020 memory-logic interconnects at 0.24 mm x 0.24 mm pitch providing wide IO PoP implementation.
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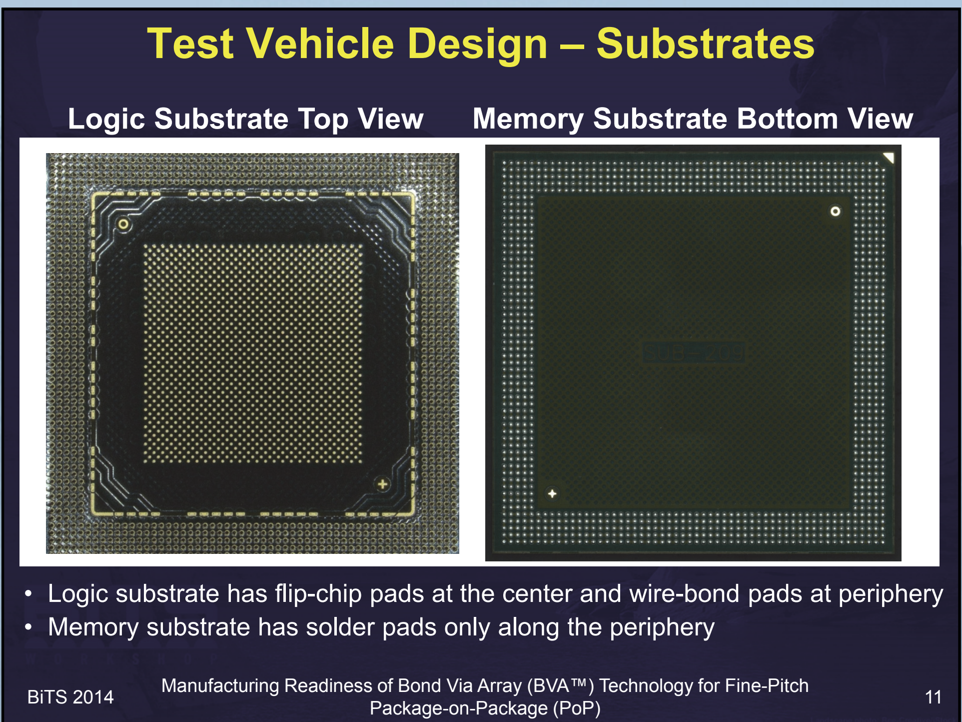
Test Vehicle Design – Substrates
Logic Substrate Top View
Memory Substrate Bottom View
• Logic substrate has flip-chip pads at the center and wire-bond pads at periphery
• Memory substrate has solder pads only along the periphery
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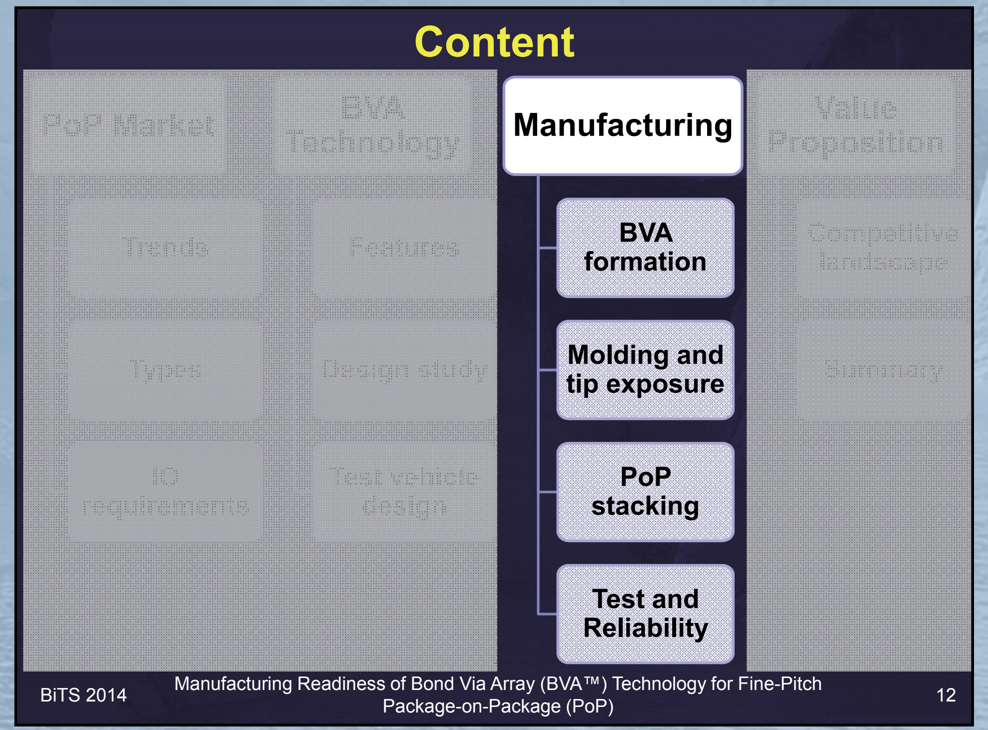
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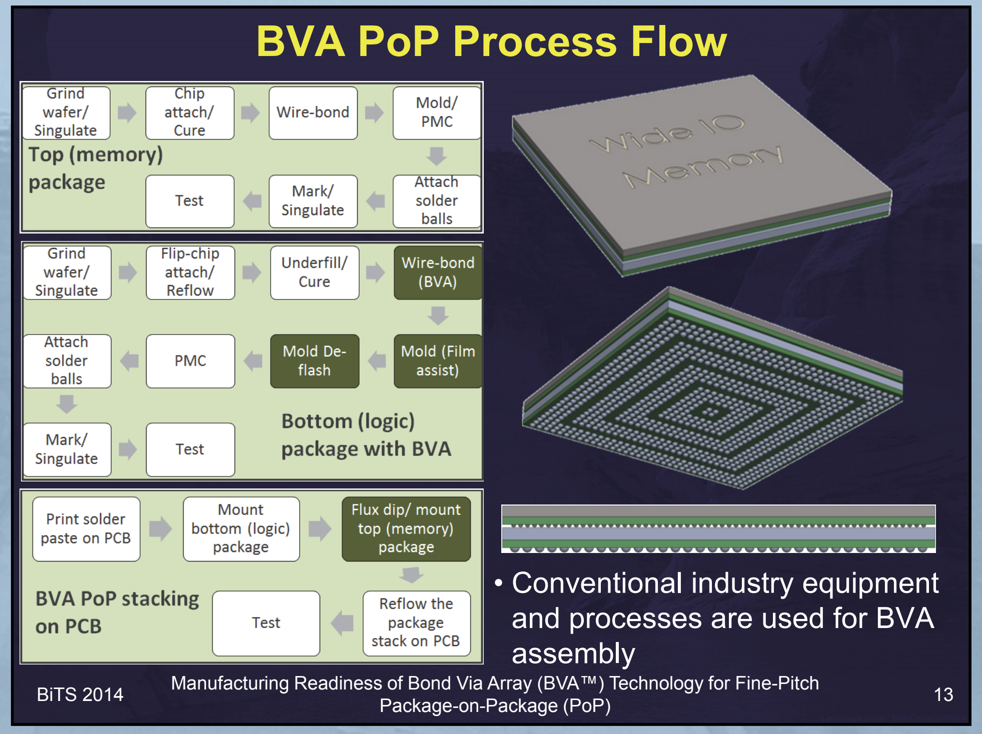

BVA PoP Process Flow
Grind wafer/ Singulate
Chip attach/ Cure
Wire-bond
Mold/ PMC
Attach solder balls
Mark/ Singulate
Test
Top (memory) package
Grind wafer/ Singulate
Flip-chip attach/ Reflow
Underfill/ Cure
Wire-bond (BVA)
Mold (Film assist)
Mold De-flash
PMC
Attach solder balls
Mark/ Singulate
Test
Bottom (logic) package with BVA
Print solder paste on PCB
Mount bottom (logic) package
Flux dip/ mount top (memory) package
Reflow the package stack on PCB
Test
BVA PoP stacking on PCB
Wide IO Memory
• Conventional industry equipment and processes are used for BVA assembly
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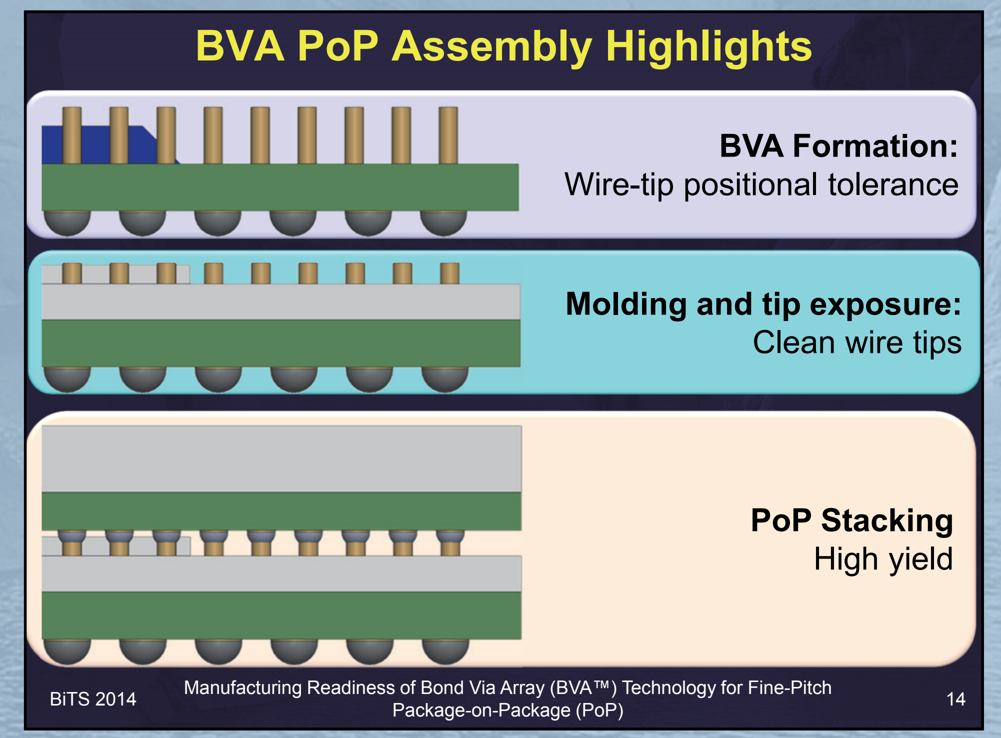

BVA PoP Assembly Highlights
BVA Formation:
Wire-tip positional tolerance
Molding and tip exposure:
Clean wire tips
PoP Stacking
High yield
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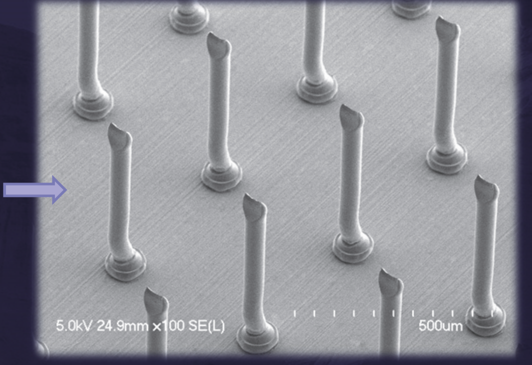
BVA Formation: Process

Photo: Courtesy of Kulicke & Soffa



- Co-developed vertical wirebond process
- Robust process using conventional ICONN
- Verified volume production feasibility
- High positional accuracy and yield

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Molding and Wire-Tip Exposure

Film Assist Mold

Mold Tool

Mold Film

Overmold

Photo: Courtesy of APIC Yamada Corp.

G-Line Mold Machine

- Critical process parameters verified in cooperation with Yamada mold
- Established production process that ensures uniform and clean wire tips

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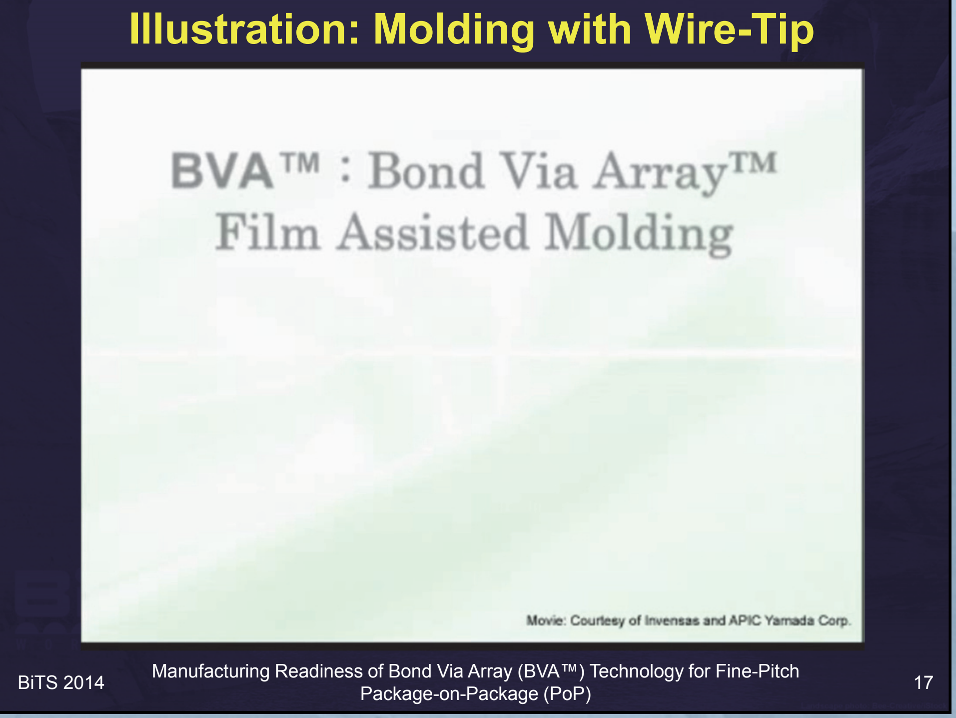
Illustration: Molding with Wire-Tip
BVA™ : Bond Via Array™
Film Assisted Molding
Movie: Courtesy of Invensas and APIC Yamada Corp.
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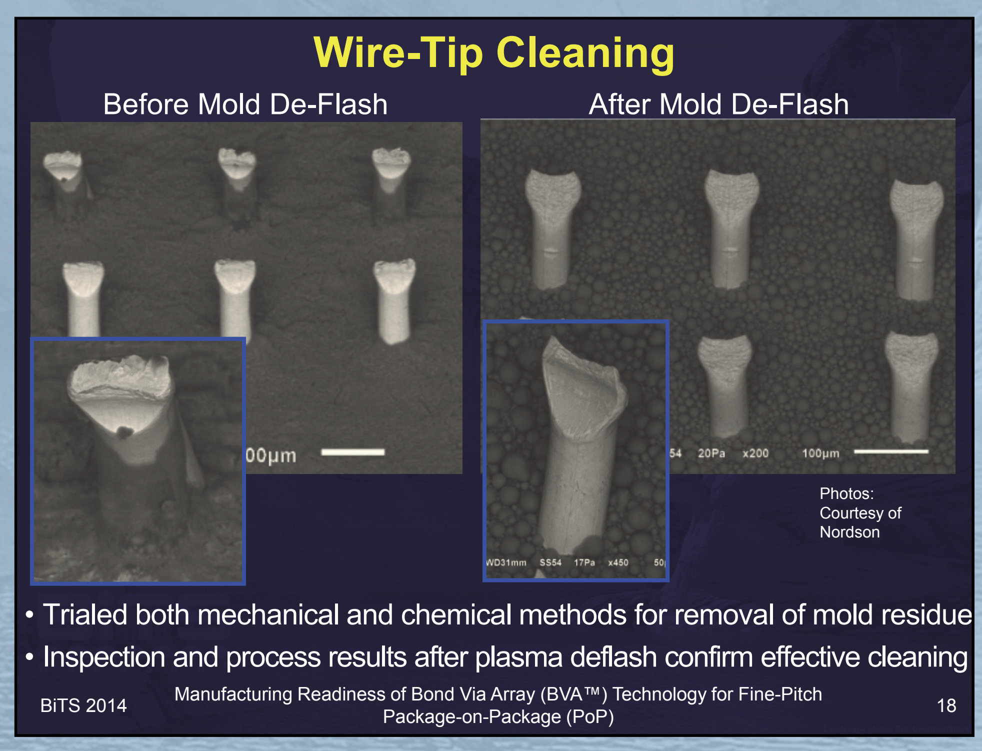
Wire-Tip Cleaning
Before Mold De-Flash
After Mold De-Flash
Photos: Courtesy of Nordson
• Trialed both mechanical and chemical methods for removal of mold residue
• Inspection and process results after plasma deflash confirm effective cleaning
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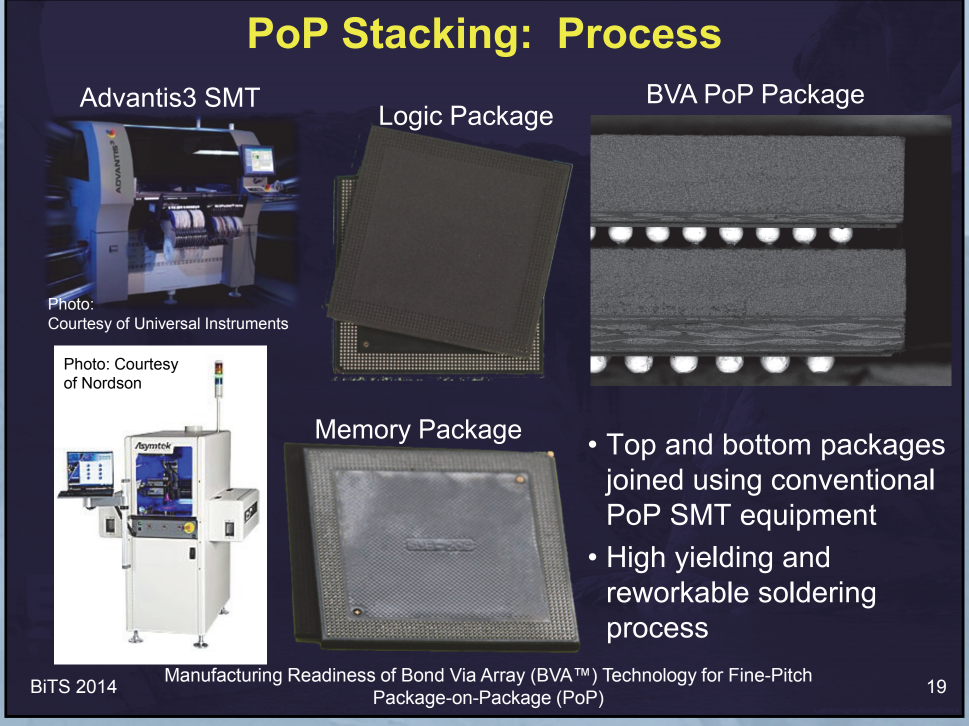
PoP Stacking: Process
Advantis3 SMT
Photo:
Courtesy of Universal Instruments
Logic Package
BVA PoP Package
Photo: Courtesy
of Nordson
Memory Package
• Top and bottom packages joined using conventional PoP SMT equipment
• High yielding and reworkable soldering process
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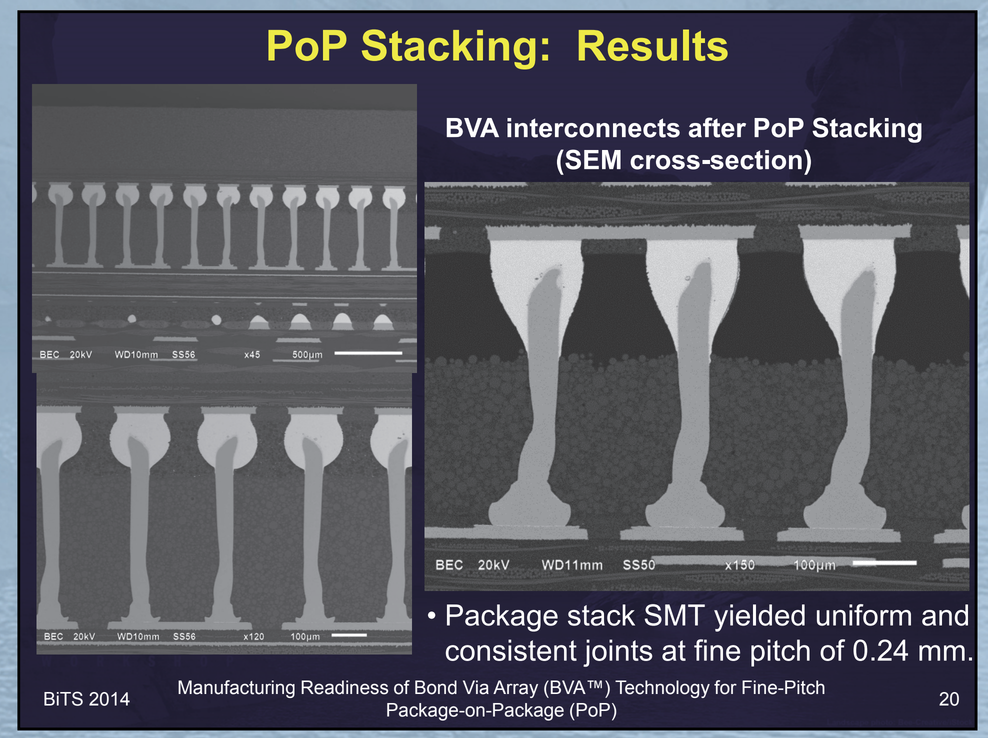
PoP Stacking: Results
BVA interconnects after PoP Stacking
(SEM cross-section)
BEC 20kV WD10mm SS56 x45 500µm
BEC 20kV WD10mm SS56 x120 100µm
BEC 20kV WD11mm SS50 x150 100µm
• Package stack SMT yielded uniform and consistent joints at fine pitch of 0.24 mm.
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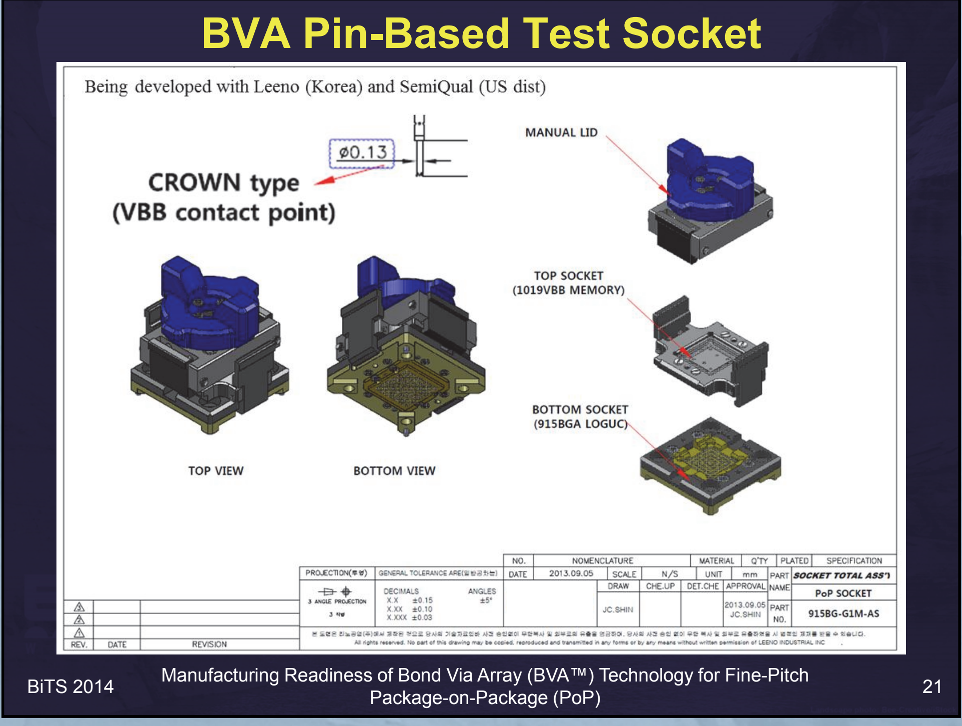
BVA Pin-Based Test Socket
Being developed with Leeno (Korea) and SemiQual (US dist)
Ø0.13
CROWN type
(VBB contact point)
MANUAL LID
TOP SOCKET
(1019VBB MEMORY)
BOTTOM SOCKET
(915BGA LOGUC)
TOP VIEW
BOTTOM VIEW
SOCKET TOTAL ASS'Y
PoP SOCKET
915BG-G1M-AS
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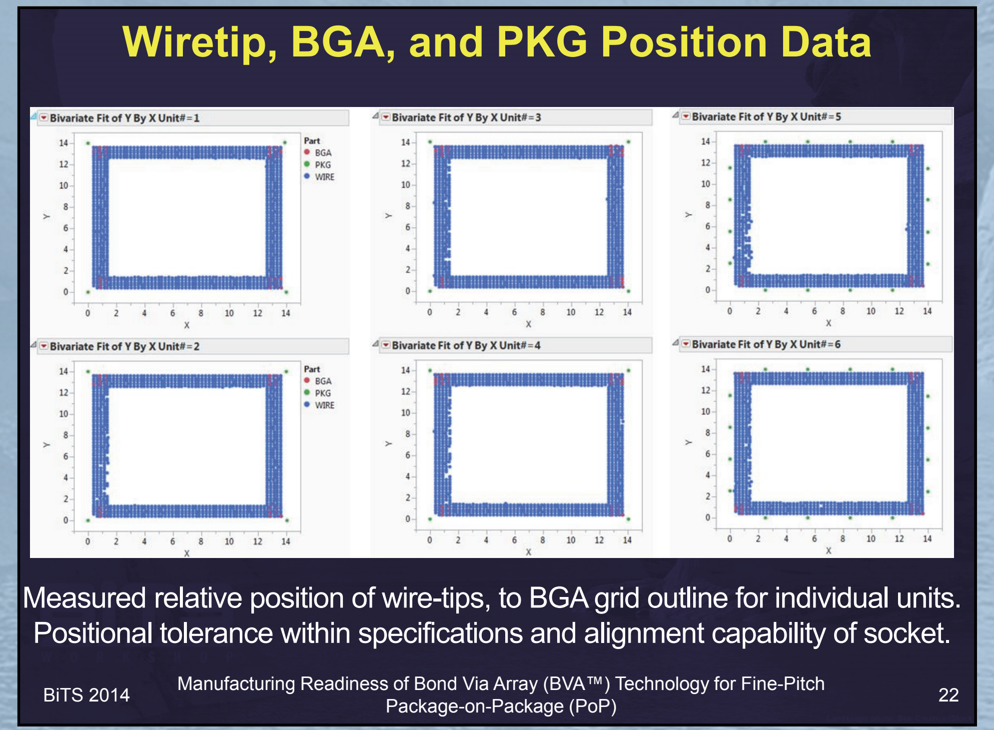
Wiretip, BGA, and PKG Position Data
Bivariate Fit of Y By X Unit#=1
Bivariate Fit of Y By X Unit#=3
Bivariate Fit of Y By X Unit#=5
Bivariate Fit of Y By X Unit#=2
Bivariate Fit of Y By X Unit#=4
Bivariate Fit of Y By X Unit#=6
Part
BGA
PKG
WIRE
Measured relative position of wire-tips, to BGA grid outline for individual units.
Positional tolerance within specifications and alignment capability of socket.
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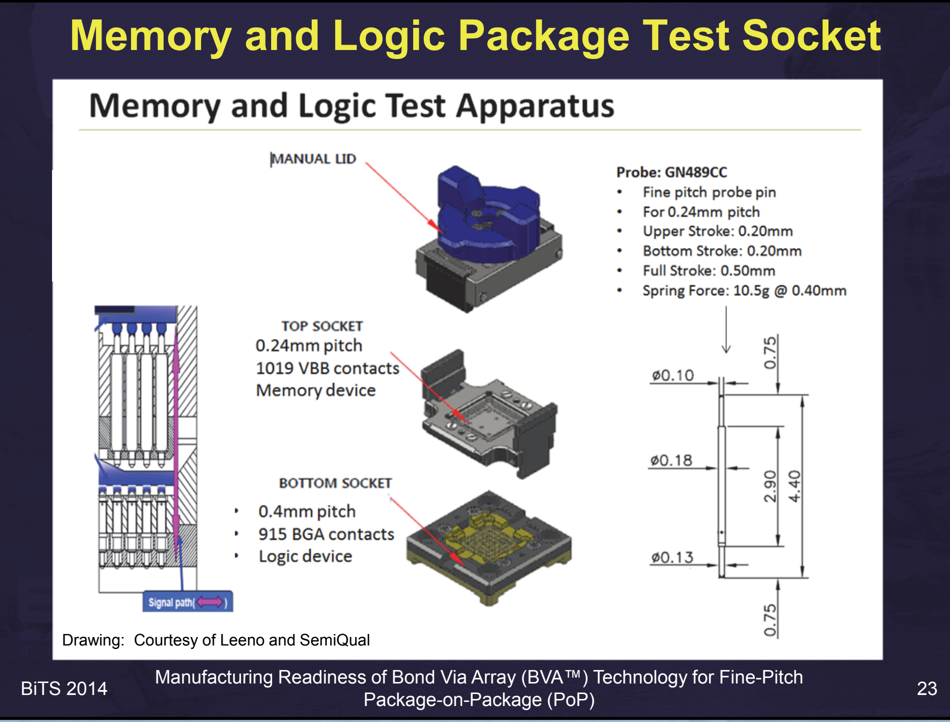
Memory and Logic Package Test Socket



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1020-IO BVA PoP Reliability Testing

Test	Standard	Test Condition	Sample	Results
MSL: Level3	IPC / JEDEC J-STD-020C	125°C for 24hrs; 30°C/60%RH for 192 hrs, 3X Pb-free reflow	22	Pass
Temperature Cycling (Board Level)	JESD22-A104D Condition G	-40°C to 125°C, 1000 cycles	45	Pass
High Temperature Storage	JESD22-A103D Condition B	150°C, 1000 hrs	22	Pass
Drop Testing	JESD22-B111	>30drops, 1500Gs, 0.5mSec of half sine pulse	20	Pass

- **1020-IO BVA PoP successfully passed all standard tests**

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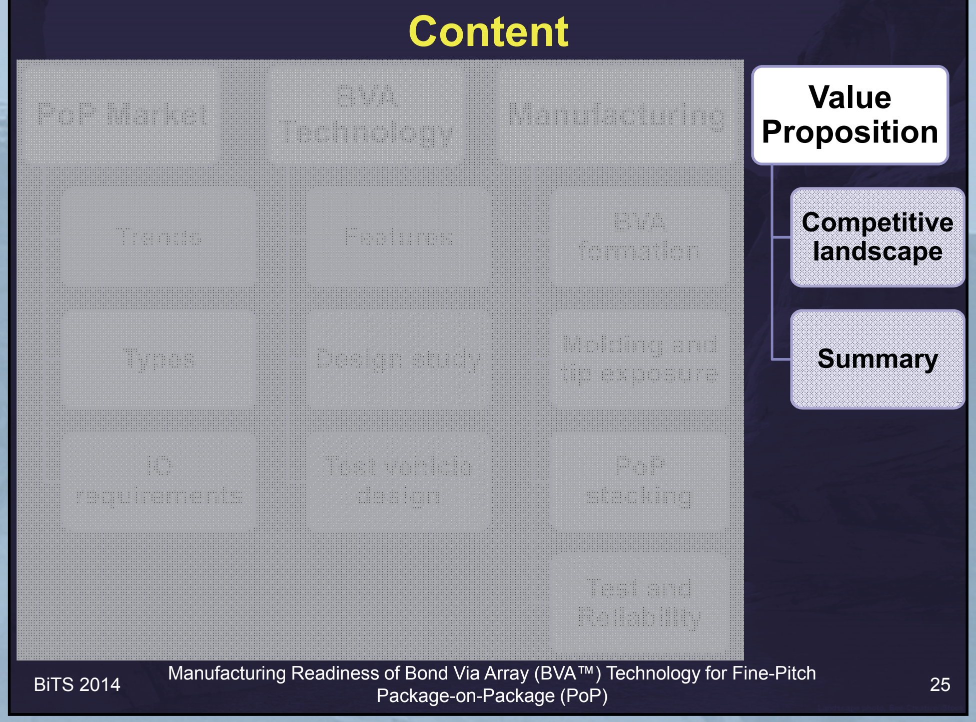
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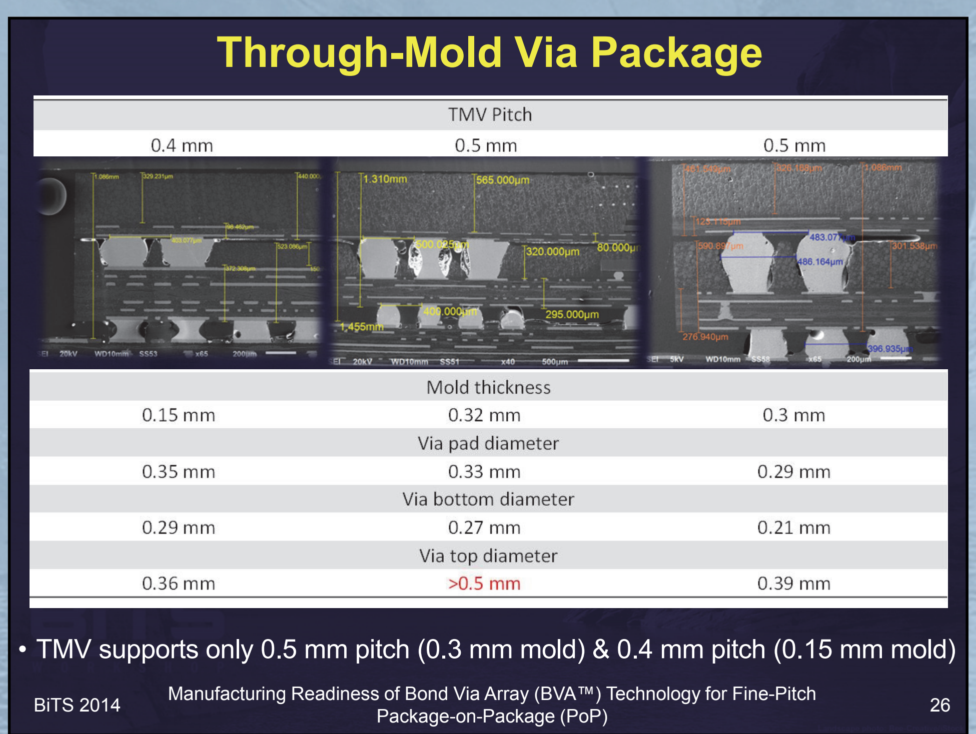
Through-Mold Via Package
TMV Pitch
0.4 mm
0.5 mm
0.5 mm
Mold thickness
0.15 mm
0.32 mm
0.3 mm
Via pad diameter
0.35 mm
0.33 mm
0.29 mm
Via bottom diameter
0.29 mm
0.27 mm
0.21 mm
Via top diameter
0.36 mm
>0.5 mm
0.39 mm
• TMV supports only 0.5 mm pitch (0.3 mm mold) & 0.4 mm pitch (0.15 mm mold)
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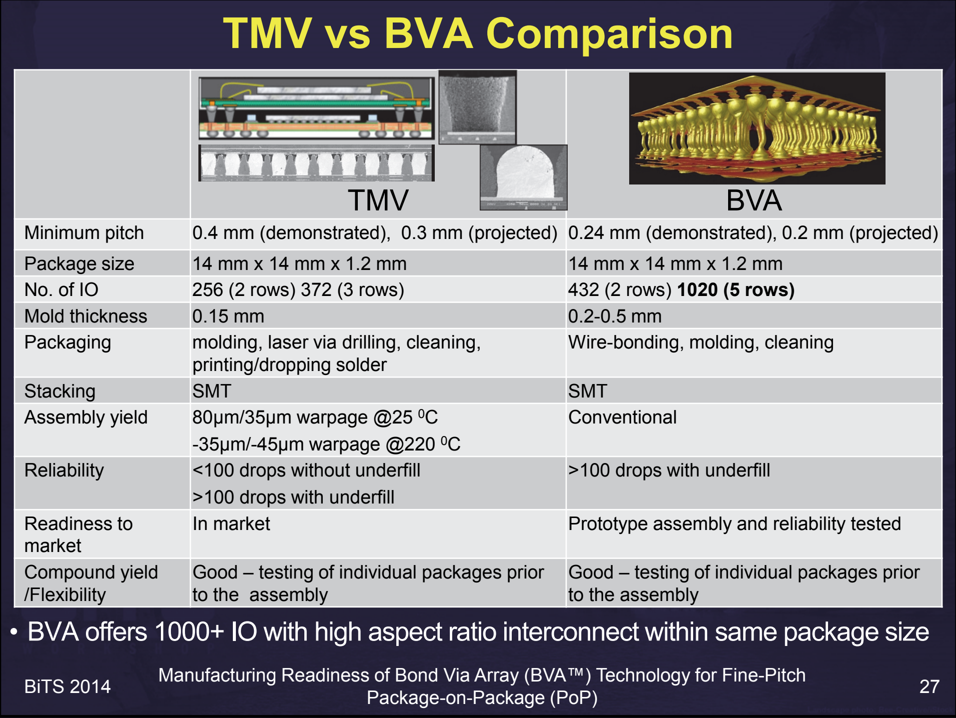

	TMV	BVA
Minimum pitch	0.4 mm (demonstrated), 0.3 mm (projected)	0.24 mm (demonstrated), 0.2 mm (projected)
Package size	14 mm x 14 mm x 1.2 mm	14 mm x 14 mm x 1.2 mm
No. of IO	256 (2 rows) 372 (3 rows)	432 (2 rows) **1020 (5 rows)**
Mold thickness	0.15 mm	0.2-0.5 mm
Packaging	molding, laser via drilling, cleaning, printing/dropping solder	Wire-bonding, molding, cleaning
Stacking	SMT	SMT
Assembly yield	80µm/35µm warpage @25 ^{0}C -35µm/-45µm warpage @220 ^{0}C	Conventional
Reliability	<100 drops without underfill >100 drops with underfill	>100 drops with underfill
Readiness to market	In market	Prototype assembly and reliability tested
Compound yield /Flexibility	Good – testing of individual packages prior to the assembly	Good – testing of individual packages prior to the assembly

- BVA offers 1000+ IO with high aspect ratio interconnect within same package size