THE MARKET IS OPEN

The BiTS Workshop just wouldn't be the BiTS Workshop without at least one presentation on the test and burn-in marketplace. In this year's three presentations, first we'll hear about the technical and market forces that are shaping the future of test and burn-in, particularly the challenges of industry cycles with the never ending quest for reduced costs. Next up will be our own Fred Taber, with his fourth annual Socket Report on the size of the market, whether its shrinking or growing, and companies that are leading the charge. This session's final paper hones in on a market technology trend with one innovative high-density package-on-package (PoP) solution requiring test hardware to accommodate fine pitch wire-tip interconnects. Socket and test hardware development and verification studies are underway to take this technology to high volume manufacturing.

The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets
John West—VLSI Research, Inc.

Socket Marketplace Report
Fred Taber—Taber Consulting

Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)
Rajesh Katkar, Rey Co, Wael Zohni—Invensas Corporation

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Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

Rajesh Katkar*, Rey Co, Wael Zohni
Invensas

2014 BiTS Workshop
March 9 - 12, 2014

Content

PoP Market
- Trends
- Types
- IO requirements

BVA Technology
- Features
- Design study
- Test vehicle design

Manufacturing
- BVA formation
- Molding and tip exposure
- PoP stacking
- Test and Reliability

Value Proposition
- Competitive landscape
- Summary
PoP Market

- Trends
- Types
- IO requirements

PoP Broadly Used in Mobile

Apple iPhone 4 Smartphone
Apple iPad
Sony Cybershot Digital Still Camera
Nokia CS Feature Phone

Source: UBM TechInsights (www.teardown.com)
**Processor-Memory Stacking Solutions**

<table>
<thead>
<tr>
<th>BGA</th>
<th>TMV</th>
<th>BVA</th>
<th>TSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>![BGA Image]</td>
<td>![TMV Image]</td>
<td>![BVA Image]</td>
<td>![TSV Image]</td>
</tr>
</tbody>
</table>

- **Pitch (mm):**
  - BGA: 0.5-0.65
  - TMV: 0.4-0.5
  - BVA: 0.2-0.4
  - TSV: 0.05-0.2

- **IO:**
  - BGA: 200-300
  - TMV: 300-500
  - BVA: 500-1500
  - TSV: 1000+

- BVA offers the advantages of TSV while utilizing existing packaging materials.

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**BVA PoP: Wide-IO Support without TSV**

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Mobile DRAM</td>
<td>LPDDR</td>
<td>LPDDR2</td>
<td>LPDDR3 Emerging</td>
<td>Wide IO</td>
<td>Wide IO</td>
<td></td>
</tr>
<tr>
<td>Packaging</td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>PoP</td>
<td>BVA PoP</td>
<td>TSV</td>
</tr>
<tr>
<td>Mobile processor to memory interconnect</td>
<td>168</td>
<td>168</td>
<td>240</td>
<td>240</td>
<td>IO ranging from 200 to 1000+</td>
<td>1200</td>
</tr>
<tr>
<td>Clock Speed (MHz)</td>
<td>400</td>
<td>533</td>
<td>800</td>
<td>High IO offers high bandwidth at low speed</td>
<td>200</td>
<td></td>
</tr>
<tr>
<td>Power</td>
<td>2X</td>
<td>1X</td>
<td>0.8X</td>
<td>Enables intermediate power reductions</td>
<td>0.5X</td>
<td></td>
</tr>
<tr>
<td># of Channels</td>
<td>Single</td>
<td>Single</td>
<td>Dual</td>
<td>Dual</td>
<td>Quad+</td>
<td>Quad+</td>
</tr>
<tr>
<td>Bandwidth (GB/s)</td>
<td>1.6</td>
<td>4.2</td>
<td>8.5</td>
<td>12.8</td>
<td>≥25.6</td>
<td>≥25.6</td>
</tr>
</tbody>
</table>

- Wide IO provides order of magnitude increase in IO
- Wide IO implementation with TSV is not expected soon
- Bond Via Array (BVA) can offer wide IO using current infrastructure
BiTS 2014 Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

Content

- BVA Technology
- Features
- Design study
- Test vehicle design

BVA PoP Features

- Stand-off issue eliminated: Wire-bond based memory-logic interconnect
- 1000+ wide IO: 0.2 mm pitch capability
- High performance at low-cost: Conventional PoP materials, equipment and process

Top View

Memory-Logic Interface

Side View

Multi-Chip Wide IO DRAM

Multi-Core CPU/GPU

Bond Via Array (BVA)
Test Vehicle Design – 432 IO

- Reliability test vehicle with 432 memory-logic interconnects at 0.24mm x 0.24mm

Test Vehicle Design – 1020 IO

- 1020 memory-logic interconnects at 0.24 mm x 0.24 mm pitch providing wide IO PoP implementation.
Test Vehicle Design – Substrates

Logic Substrate Top View

Memory Substrate Bottom View

- Logic substrate has flip-chip pads at the center and wire-bond pads at periphery
- Memory substrate has solder pads only along the periphery

Content

Manufacturing

- BVA formation
- Molding and tip exposure
- PoP stacking
- Test and Reliability

BiTS 2014 Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)
BVA PoP Process Flow

- Conventional industry equipment and processes are used for BVA assembly.

BVA PoP Assembly Highlights

- **BVA Formation:** Wire-tip positional tolerance
- **Molding and tip exposure:** Clean wire tips
- **PoP Stacking:** High yield
Session 4

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Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

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**BVA Formation: Process**

- Co-developed vertical wirebond process
- Robust process using conventional ICONN
- Verified volume production feasibility
- High positional accuracy and yield

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**Molding and Wire-Tip Exposure**

- Critical process parameters verified in cooperation with Yamada mold
- Established production process that ensures uniform and clean wire tips

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Photo: Courtesy of Kulicke & Soffa

Photo: Courtesy of APIC Yamada Corp.
Illustration: Molding with Wire-Tip

BVA™: Bond Via Array™ Film Assisted Molding

- Trialed both mechanical and chemical methods for removal of mold residue
- Inspection and process results after plasma deflash confirm effective cleaning

Wire-Tip Cleaning

Before Mold De-Flash

After Mold De-Flash

Photos: Courtesy of Nordson

Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)
PoP Stacking: Process

- Top and bottom packages joined using conventional PoP SMT equipment
- High yielding and reworkable soldering process

PoP Stacking: Results

- Package stack SMT yielded uniform and consistent joints at fine pitch of 0.24 mm.
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**Session 4**

**BVA Pin-Based Test Socket**

Being developed with Leeno (Korea) and SemiQual (US dist)

**Wiretip, BGA, and PKG Position Data**

Measured relative position of wire-tips, to BGA grid outline for individual units. Positional tolerance within specifications and alignment capability of socket.
Memory and Logic Test Apparatus

Test Standard Test Condition Sample Results

MSL: Level 3 IPC / JEDEC J-STD-020C 125°C for 24 hrs; 30°C/60%RH for 192 hrs, 3x Pb-free reflow 22 Pass

Temperature Cycling (Board Level) JESD22-A104D Condition G -40°C to 125°C, 1000 cycles 45 Pass

High Temperature Storage JESD22-A103D Condition B 150°C, 1000 hrs 22 Pass

Drop Testing JESD22-B111 > 30 drops, 1500 Gs, 0.5 mSec of half sine pulse 20 Pass

• 1020-IO BVA PoP successfully passed all standard tests
### Through-Mold Via Package

<table>
<thead>
<tr>
<th>TMV Pitch</th>
<th>0.4 mm</th>
<th>0.5 mm</th>
<th>0.5 mm</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Mold thickness</th>
<th>Via pad diameter</th>
<th>Via bottom diameter</th>
<th>Via top diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.15 mm</td>
<td>0.32 mm</td>
<td>0.29 mm</td>
<td>&gt;0.5 mm</td>
</tr>
<tr>
<td>0.35 mm</td>
<td>0.33 mm</td>
<td>0.21 mm</td>
<td></td>
</tr>
<tr>
<td>0.29 mm</td>
<td>0.27 mm</td>
<td>0.21 mm</td>
<td></td>
</tr>
<tr>
<td>0.36 mm</td>
<td>&gt;0.5 mm</td>
<td></td>
<td></td>
</tr>
</tbody>
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- TMV supports only 0.5 mm pitch (0.3 mm mold) & 0.4 mm pitch (0.15 mm mold)
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Session 4

TMV vs BVA Comparison

<table>
<thead>
<tr>
<th></th>
<th>TMV</th>
<th>BVA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum pitch</td>
<td>0.4 mm (demonstrated), 0.3 mm (projected)</td>
<td>0.24 mm (demonstrated), 0.2 mm (projected)</td>
</tr>
<tr>
<td>Package size</td>
<td>14 mm x 14 mm x 1.2 mm</td>
<td>14 mm x 14 mm x 1.2 mm</td>
</tr>
<tr>
<td>No. of I/O</td>
<td>256 (2 rows) 372 (3 rows)</td>
<td>432 (2 rows) 1020 (5 rows)</td>
</tr>
<tr>
<td>Mold thickness</td>
<td>0.15 mm</td>
<td>0.2-0.5 mm</td>
</tr>
<tr>
<td>Packaging</td>
<td>molding, laser via drilling, cleaning,</td>
<td>Wire-bonding, molding, cleaning</td>
</tr>
<tr>
<td></td>
<td>printing/dropping solder</td>
<td></td>
</tr>
<tr>
<td>Stacking</td>
<td>SMT</td>
<td>SMT</td>
</tr>
<tr>
<td>Assembly yield</td>
<td>80µm/35µm warpage @ 25 °C</td>
<td>Conventional</td>
</tr>
<tr>
<td></td>
<td>-35µm/-45µm warpage @ 220 °C</td>
<td></td>
</tr>
<tr>
<td>Reliability</td>
<td>&lt;100 drops without underfill</td>
<td>&gt;100 drops with underfill</td>
</tr>
<tr>
<td></td>
<td>&gt;100 drops with underfill</td>
<td></td>
</tr>
<tr>
<td>Readiness to market</td>
<td>In market</td>
<td>Prototype assembly and reliability tested</td>
</tr>
<tr>
<td>Compound yield/Flexibility</td>
<td>Good – testing of individual packages prior to the assembly</td>
<td>Good – testing of individual packages prior to the assembly</td>
</tr>
</tbody>
</table>

• BVA offers 1000+ IO with high aspect ratio interconnect within same package size

Summary

Technology

A wire-bond based interconnect technology offering 1000+ interconnects

BVA PoP with 1020 IO logic-memory interface successfully assembled at 0.24 mm pitch and passed reliability tests

Value

More than twice the number of IO in the same package size compared to competing solutions

Utilizes existing infrastructure and is cost competitive

BVA PoP realizes wide IO interface in conventional packaging, offering high performance at low power and cost.