

Tuesday 3/11/14 11:00am

THE MARKET IS OPEN

The BiTS Workshop just wouldn't be the BiTS Workshop without at least one presentation on the test and burn-in marketplace. In this year's three presentations, first we'll hear about the technical and market forces that are shaping the future of test and burn-in, particularly the challenges of industry cycles with the never ending quest for reduced costs. Next up will be our own Fred Taber, with his fourth annual Socket Report on the size of the market, whether its shrinking or growing, and companies that are leading the charge. This session's final paper hones in on a market technology trend with one innovative high-density package-on-package (PoP) solution requiring test hardware to accommodate fine pitch wire-tip interconnects. Socket and test hardware development and verification studies are underway to take this technology to high volume manufacturing.

This Paper

The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets

John West—VLSI Research, Inc.

Socket Marketplace Report

Fred Taber—Taber Consulting

Manufacturing Readiness of Bond Via Array (BVA™) Technology for Fine-Pitch Package-on-Package (PoP)

Rajesh Katkar, Rey Co, Wael Zohni—Invensas Corporation

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FIFTEENTH ANNUAL
2014

Burn-in & Test Strategies Workshop™

Session 4

The Market is Open

The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets

John West
VLSI Research, Inc.



2014 BiTS Workshop
March 9 - 12, 2014

VLSIresearch

Overview

- **Introduction**
- **Semiconductors**
- **Cost per Device Tested**
- **Competitive Factors**
- **Summary**



BiTS 2014

The Technical and Market Forces Shaping the Future of Test and Burn-In Sockets

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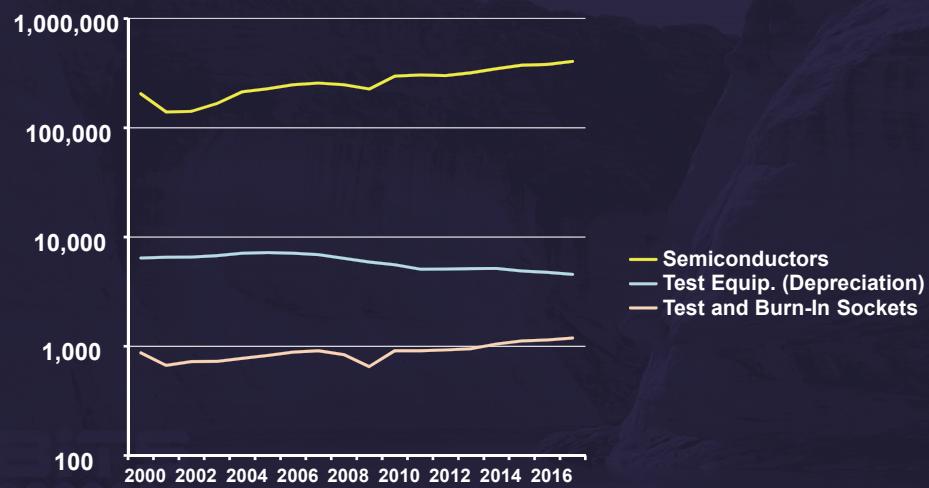
Paper #1
1

2014 BiTS Workshop ~ March 9 - 12, 2014

Some Perspective... 2013 Sales, \$Bn

- Semiconductors 318.5
- Test Equipment 3.3
- Test & Burn-In Sockets 1.0

Value for Money? Sales in \$Bn



Semiconductors

- Long-term growth assured
 - Revenues
 - Units
- Device Types
- Package Types/Technologies
- Cost Benefit of Shrinking is Slowing
 - May even be going up!

Semiconductors

VLSI's Spot Market Chip Price Performance Index

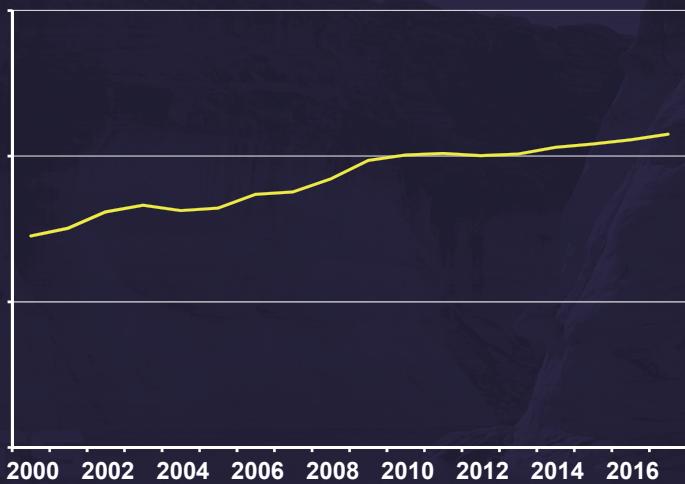


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Costs per Device Tested

- **ATE**
 - down 33% last 5 years
- **Test Handlers**
 - down 25% last 5 years
- **Test and Burn-In Sockets**
 - down 10% last 5 years

Pins Per Device... Still Going Up



Test and Burn-In Socket Cost per Device Tested, Cents

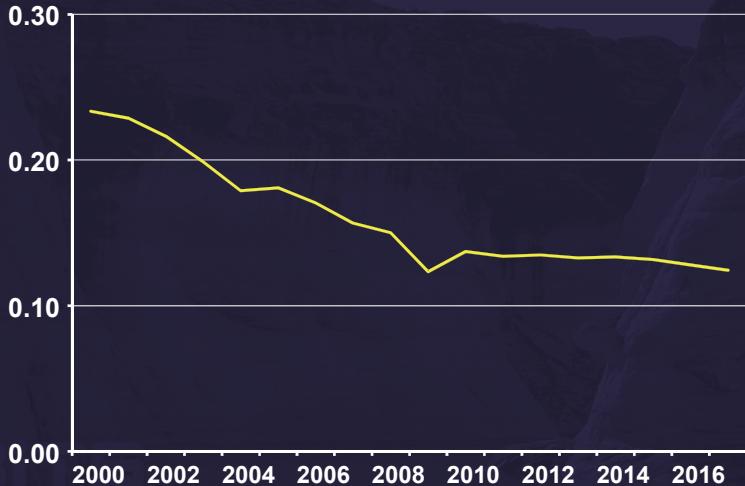


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Industry-Wide Cost Reduction Roadmap

Does not necessarily mean lower profits...

- New Technologies = New Opportunities
- Competitive rivalry leads to innovation
- Increased complexity
 - Higher barriers to entry
 - Consolidation

Summary

	2013	2014	2017	CAGR 12-17
Test Sockets, \$M	511	554	654	5.1%
<i>Annual Growth %</i>	<i>1%</i>	<i>8%</i>		
Burn-In Sockets, \$M	439	478	533	5.0%
<i>Annual Growth, %</i>	<i>6%</i>	<i>9%</i>		
Semiconductors, \$Bn	318	347	405	6.2%
<i>Annual Growth, %</i>	<i>6%</i>	<i>9%</i>		

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