

Monday 3/10/14 10:30am

A CLEAN START

There's no doubt about it, clean contacts in contactors and sockets work a lot better than dirty ones. So what better place to start looking at burn-in and test strategies than with a close look at contamination control and cleaning processes to improve yields, test time and re-test reduction? This session begins with three hypotheses of the causes for contact contamination, Along with guidance on procedural changes for improved performance. The next presentation offers a solution to the havoc high temperature burn-in can wreak on devices under test (DUTs) with a specialized coating process to prevent solder contamination of contacts and deformation of the solder bumps on the DUT. The final two presentations examine online cleaning processes. The first focuses on a characterization tool that determines the effectiveness of online cleaning, while the second is directed at an automatic cleaning solution for a bowl fed handler used with a RF contactor. Hey, it's a dirty job, but somebody's got to do it.

Contamination Mechanisms of Contact Probes

Jon Diller, Kevin DeFord—Smiths Connectors | IDI

Special Coating Cleans-Up a Mess

Paul Ruo—Aries Electronics, Inc.

Erik Orwoll—Contact Coatings, LLC

This Paper

Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

Jerry J. Broz, Ph.D., Soheil Khavandi, Bret Humphrey—International Test Solutions

Yield and Test Time Improvement via Automated Online Cleaning

Brent Edington—TriQuint

COPYRIGHT NOTICE

The paper(s) in this publication comprise the Proceedings of the 2014 BiTS Workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2014 BiTS Workshop. This version of the papers may differ from the version that was distributed in hardcopy & softcopy form at the 2014 BiTS Workshop. The inclusion of the papers in this publication does not constitute an endorsement by BiTS Workshop, LLC or the workshop's sponsors.

There is NO copyright protection claimed on the presentation content by BiTS Workshop, LLC. (Occasionally a Tutorial and/or TechTalk may be copyrighted by the author). However, each presentation is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

The BiTS logo and 'Burn-in & Test Strategies Workshop' are trademarks of BiTS Workshop, LLC. All rights reserved.

Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

Jerry Broz, Ph.D., Soheil Khavandi, Bret Humphrey
International Test Solutions, Inc.



2014 BiTS Workshop
March 9 - 12, 2014



Overview

- Introduction
- Motivation / Approach
- Methodology
- Implementation / Characterization
- Summary
- Conclusions



Introduction – What we already know !

- Semiconductor packages carry various debris and other contaminants that affect electrical contact integrity.
- Contamination is found on contact surfaces, around the pins, along guide plates, and across the socket bed.
- Contactors must physically and reliably touch the I/O's of the DUT for test programs to be properly executed.
- Unstable contact resistance (CRES) is the biggest factor for yield fallout, opens/ shorts, and re-screen problems.

Introduction – What we already know !

- Contact reliability is controlled through socket cleaning.
- Socket maintenance is critical to control CRES, maximize contactor electrical performance, and extend lifetimes
- Off-line cleaning (idle state with potentially long downtime)
 - Pins in sockets and sockets in load-boards are replaced at added cost
 - Socket lifetime can be reduced due to cleaning related damage
 - Excessive cleaning can reduce test throughput without yield benefits
- On-line cleaning (consistent CRES control and low downtime)
 - Socket and load boards remain docked (no idle state needed)
 - Debris and adherent materials are removed from socket in-situ
 - Consistent cleaning to maintain high FPY yields and without downtime

Cleaning in Package Test Parallels Wafer Sort

Manual Test by operators

Wafer Sort



Prober is in idle state

Minimal Intervention



Yield control
Minimal downtime

KEY DRIVERS

High Costs of Test
High \$\$\$ Tooling

OEE Improvement
High \$\$\$ Devices
High Device Volumes

1970

2000

2007

Today

Manual Clean by operators

Package Test



Handler is in idle state

Reduced Intervention



ACC Function

Minimized Intervention



Delta Design, Advantest,
MultiTest, Seiko-Epson, SRM

BiTS 2014

Unique Methodologies for Investigating On-line Cleaning Process Parameters and
Recipe Optimization

5

Socket Auto Clean Reduces Downtime



Test Cell

Targeted first pass yield (FPY)

Actual first pass yield

↑ Yield recovery after cleaning execution

..... Yield loss threshold requiring cleaning

Yield

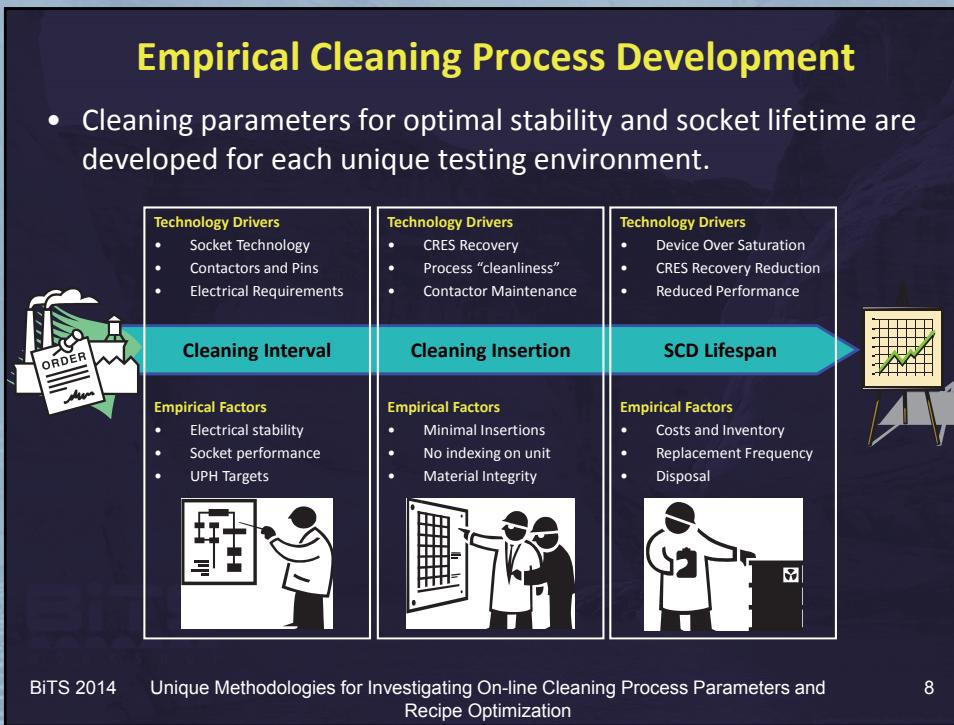
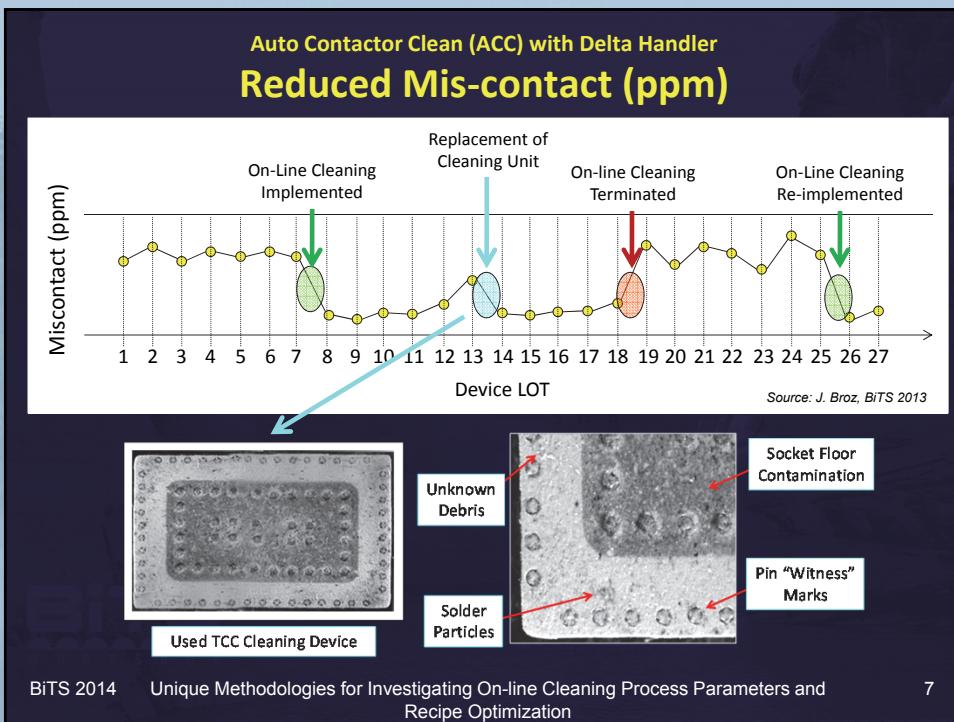
Time

BiTS 2014

Unique Methodologies for Investigating On-line Cleaning Process Parameters and
Recipe Optimization

G. Gschwendtberger, SEMICON Europa 2008

6



Motivation

- Assessing combinations of key parameters requires substantial resource allocation.
- Production package test floors are typically manpower, time, and resource limited.
- Basic testing and optimizations in a high volume package test environment is often not feasible.
- A methodology is needed to for cleaning process development under controlled conditions.
- Initial cleaning processes could be developed and implemented for each device family.

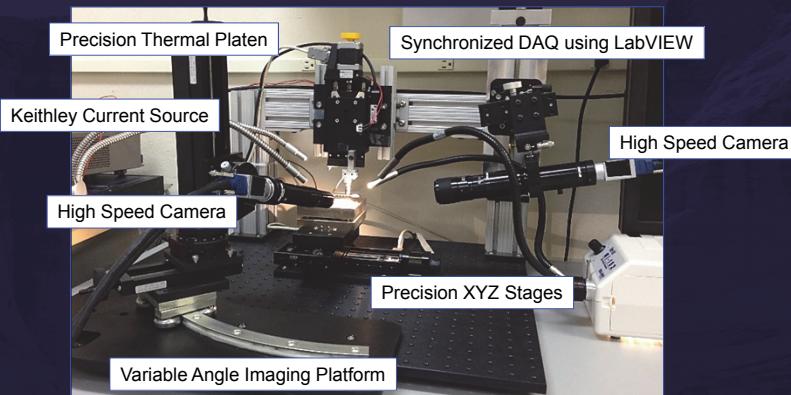
Approach

- Existing process development methods have shortcomings
 - Resources to assess material(s) performance are limited.
 - Demanding UPH requirements prohibit iterative characterizations.
 - “Optimized” cleaning processes for the HVM environment can occur “on the fly”.
- Initial cleaning recipe assessment should be possible using some combination of test-die and contactor technologies
 - Off-line development should be applicable to actual products.
 - High number of touchdowns utilizing very “little real estate”.
 - Test capabilities to facilitate investigation of cleaning materials.

Objectives

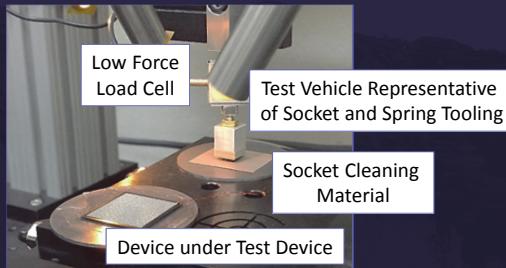
- Develop off-line analytical tool and standardized test methods to effectively ...
 - Characterize / quantify key cleaning material performance metrics
 - Visualize contactor and cleaning material interactions
 - Optimize cleaning process using representative devices and pins
- Controlled conditions for “cleaning recipe starting point”
 - Probe force vs. z-Overtravel vs. CRES with high speed imaging
 - Repeated insertions and stepping to quantify probe-tip wear
 - Cleaning process development capabilities which include microstepping, z-speed control, insertions, etc.
 - Thermal capabilities across representative test temperature

Socket-Gen Characterization Tool



- Variable speed / acceleration z-stage
- Dual high speed cameras with for high resolution video imaging
- Synchronized load vs. overtravel vs. CRES acquisition vs. Video
- z-Stepping and XY-indexing for socket cleaning recipe development

Test Cell Details



Probe + Bump Visualization



Dual Camera Visualization



Cleaning Execution



BiTS 2014

Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

13

“Socket Gen” Case Studies

- Mechanical Behavior of Materials Testing
 - Pin-to-Material Interaction Characterizations
 - Key Parameter for Cleaning Efficiency Assessment
- Controlled Cleaning Process Development
 - Micro-stepping on device I/Os (CRES vs. Touchdowns)
 - Basic cleaning recipe parameter determination
 - Cleaning process validation

BiTS 2014

Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

14

"Socket Gen" Case Studies

- Mechanical Behavior of Materials Testing
 - Pin-to-Material Interaction Characterizations
 - Key Parameter for Cleaning Efficiency Assessment
- Controlled Cleaning Process Development
 - Micro-stepping on-device I/Os (CRES vs. Touchdowns)
 - Basic cleaning recipe parameter determination
 - Cleaning process validation

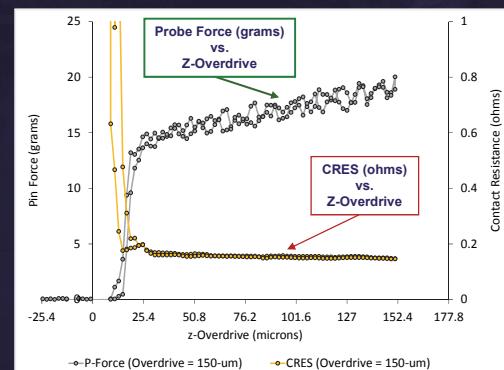
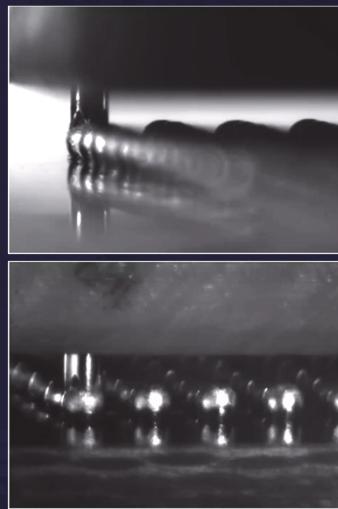
BiTS WORKSHOP

BiTS 2014 Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

15

Mechanical Behavior of Materials

- Probe-on-Ball Force vs. CRES vs. Overdrive Curves



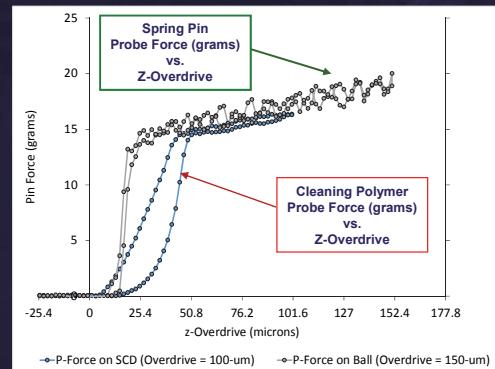
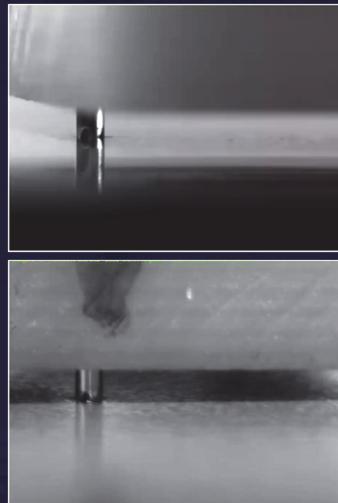
BiTS 2014 Unique Methodologies for Investigating On-line Cleaning Process Parameters and Recipe Optimization

16

Paper #3
8

Mechanical Behavior of Materials

- Probe-on-Polymer Force vs. Overdrive Curves



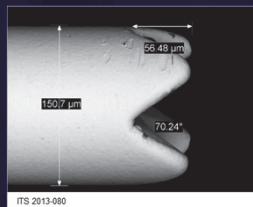
Performance Characterization

- Objectives
 - Characterize SCD polymer abrasiveness
 - Investigate effects of pin insertion speed (ACC vs. Manual)
 - Assess polymer material and pin contactor geometry interactions
 - Provide insights for a cleaning process matched to application
- Setup Parameters
 - Target p-Force = 30-grams for each pin
 - 50 × insertions at same location (model SCD lifetime)
 - Index to new location (model SCD replacement cycle)
 - Inspection at 0K and 5K clean insertions (model wear due to clean)
 - CL_Freq = 250 TD and CL_TDs = 3 per cycle → 400K DUTs Tested

Methods / Materials

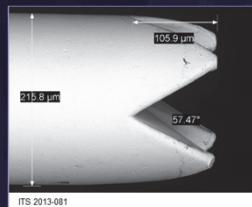
- ITS SCD Polymer Materials
 - TCC H-Abrasive (manual insertion)
 - TCC Standard (online ACC cleaning)

Small Pitch (Plated)



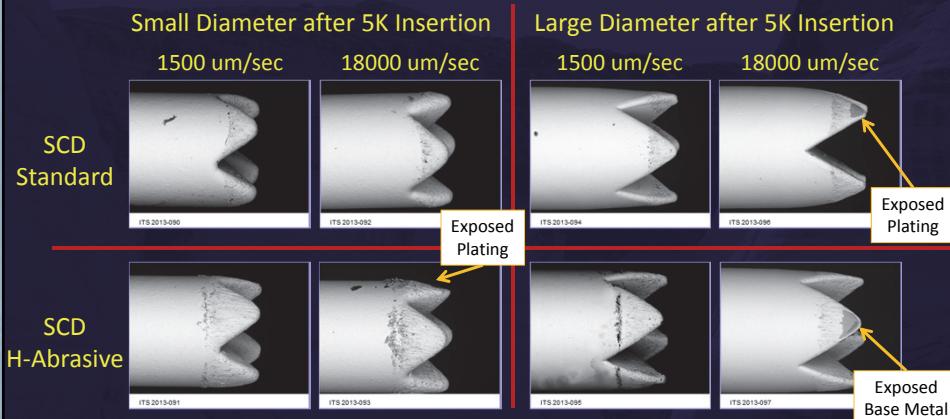
- Pin Diameter = 150um
- Tine Length = ~55 to 58um
- Tine Angle = ~70 to 75-degree

Large Pitch (Plated)



- Pin Diameter = 215um
- Tine Length = ~105 to 108um
- Tine Angle = ~55 to 60-degree

Results – Wear Effects Due to Cleaning

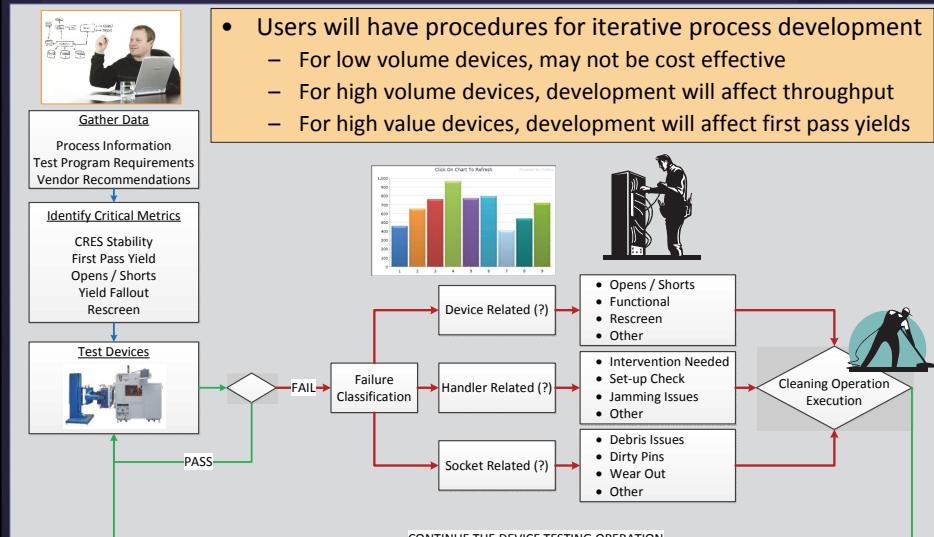


- In all cases, H-Abrasive had a greater cleaning efficiency than SCD Standard.
- For ACC speed, both materials showed tip wear and plating removal.
- Insertion speed is a key parameter for attaining high cleaning efficiency.

“Socket Gen” Case Studies

- Mechanical Behavior of Materials Testing
 - Pin-to-Material Interaction Characterizations
 - Key Parameter for Cleaning Efficiency Assessment
- Controlled Cleaning Process Development
 - Micro-stepping on device I/Os (CRES vs. Touchdowns)
 - Basic cleaning recipe parameter determination
 - Cleaning process validation

End-User “Cleaning Process” Development

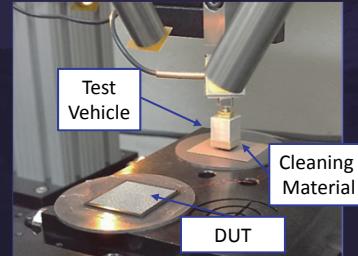


"Socket Gen" Multi-Functional Overview

- Precision XYZ Movement for 3D surface profiling for DUT and cleaning zone, and z-Overdrive consistency
- Bump XY location map for micro-stepping according to device netlist to maximize utilization of available I/Os
 - Shorted dummy devices to maximize touchdowns (XY map required)
 - Touchdowns on all I/Os with periodic CRES (XY map and netlist required)
 - Touchdowns on only VCC and/or VSS Planes (XY map and netlist required)
- Synchronized data collection of p-Force vs. touchdown vs. CRES with controlled forcing current and current application duration
- Functions for materials assessment, controlled cleaning frequency, insertion count, location on SCD, z-Overdrive, and dwell time

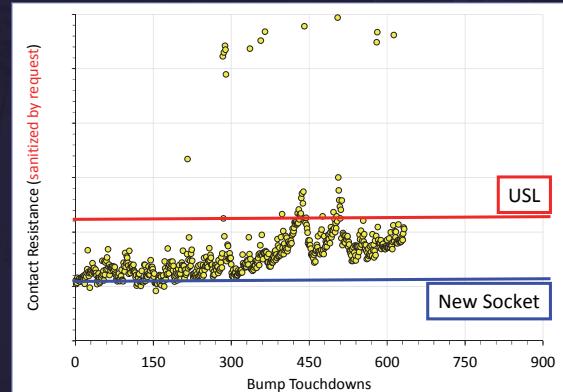
Bumped Package Testing

- Materials
 - BGA package with over 2000 bumps
 - Crown spring pin installed in test vehicle
 - 3 x SCD cleaning materials were tested – TCC Std, TCC H, and MPX Foam
- Setup Parameters
 - Pin force = 20 to 25-grams at full overdrive
 - Forcing current = 100-mA for 100-msec
 - 4-point CRES across shorted bumps
- Test Sequence
 - No-Clean Baseline identifies "When to Clean?"
 - Cleaning recipe assessed according to baseline
 - Cleaning recipe can be iteratively refined



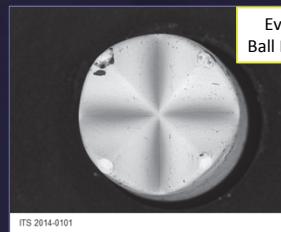
Bumped Package Test Sequence

- No-Clean Baseline to determine "When to Clean ?"

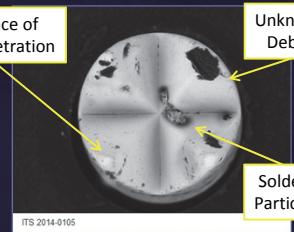


Insertions per Cycle Determination

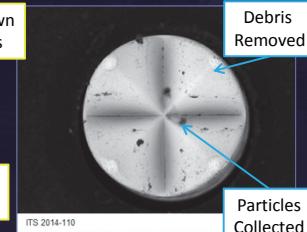
As Received



After 150 Bump TDs
Tip Debris / Accumulation



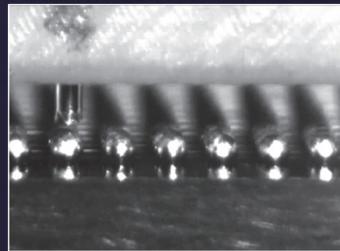
After SCD Clean Cycle
using 8 insertions



- CRES was within specification limits; BUT, after only 150 bump TDS, solder debris and process residuals were already accumulating
- Number of insertions per cycle will depend on the dirtiness of the pin and socket (i.e., debris, contaminations, residuals, etc.)
- Field data has shown 3 to 8 insertions (which do occur in same location) are generally sufficient for cleaning

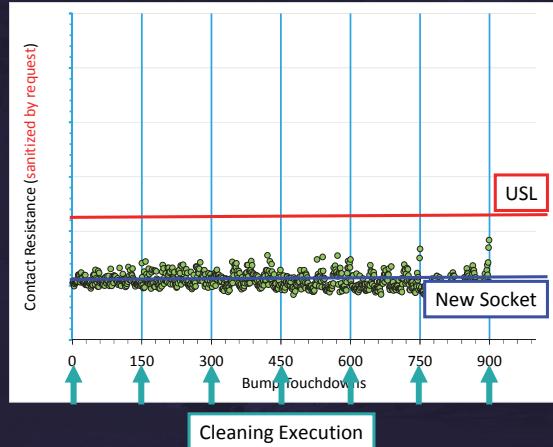
Auto Cleaning for Improved CRES Stability

- ACC cleaning performed after 150-bump touchdowns

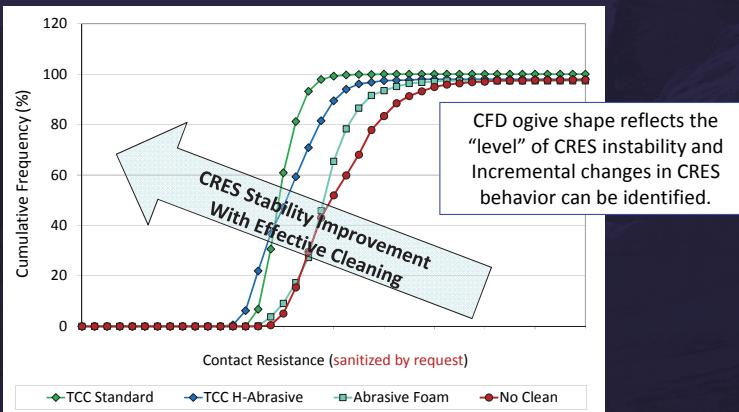


Cleaning Recipe

- CL_Freq = 150-DUT
- CL_Insertions = 8 per cycle
- Total SCD Insertions = 100



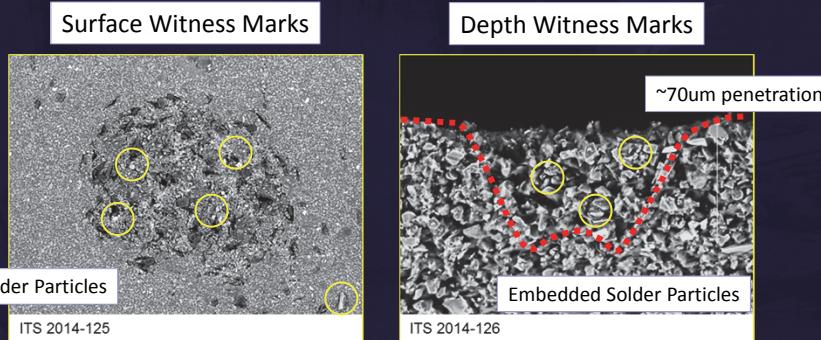
Iterative Testing for Process Improvement



- All materials tested provided some level of process improvement
- Tacky polymer materials for debris collection were most effective for CRES stability
- Abrasive foam showed small improvement; however, the small improvement was at an extremely high tooling cost for 6 to 10X greater pin wear rate.

Debris Collection

- Debris collection is critical for attaining maximum cleaning performance
- Tacky polymer materials effectively remove surface from surface as well as from within the interior of the crown contactor
- Solder and other particles are held on the surface as well as embedded into the cleaning material during penetration



Summary / Conclusions

- Non-optimized cleaning processes compromise test results, reduce tooling life, affect throughput and equipment up-time.
- Defining proper “cleaning recipes” is a crucial step to maintain CRES control; however, iterative testing can be difficult
- A unique bench-top system to assess cleaning efficiency with ACC can help guide ACC cleaning recipe” for HVM environments.
 - Visualization of cleaning material and probe interaction
 - Wear testing and probe tip shape visualization
 - Off-line cleaning process development

"When and How Much to Clean" Is Balancing Act !

- By utilizing an off-line approach, test-floor engineers can significantly reduce the amount of resources required to develop effective and efficient cleaning processes.

Too Little

- High O/S ratios
- Low First Pass Yield
- High Second Yield
- Multiple Rescreen
- Operator Assist
- Reduced OEE



Too Much

- Increased Test Time
- Reduced UPH
- Excessive Pin Wear
- Increase Tooling Costs
- Reduced Utilization
- Reduced OEE

Future Work

- Thermal (hot and cold) characterization
- High forcing current applications
- Application specific material and cleaning device development

Acknowledgements

- ITS WW Applications Team
- ITS Technical Partners ... THANKS !
 - End customers and technologists that must unfortunately remain “nameless”
- IEEE SW Test Workshop 2014
 - <http://www.swtest.org>
 - Abstract submission is open!
 - San Diego, CA, for June 8 to 11

