Keynote Speaker

Monday 3/10/14 9:00am
Kiva Ballroom

INTERCONNECTOLOGY - THE ROAD TO 3D

by
Simon McElrea
President
Invensas Corporation

*L**ast year's Talking Points talk show** introduced you to Interconnectology, a holistic approach to microelectronics manufacturing describing both technical interconnection, and supply chain partnership interconnection. This year's Keynote Speaker, Simon McElrea, President at Invensas, the Interconnectology Company, will explain why his company is spearheading this approach to manufacturing, and how it is more important than ever.*

ABSTRACT

Interconnectology is everything involved with getting "Silicon into Systems": a holistic approach describing both technical interconnection and supply chain partnership interconnection. Nowhere does this concept apply more than in the commercialization of 2.5D and 3D integration technologies. From design, to processes, and equipment and material development, to manufacturing and test, 2.5D interposer products and 3D ICs require collaboration across the value chain to achieve high yielding devices, optimum cost-of-ownership and rapid time-to-market: all critical elements for today's consumer-driven market. Further, the middle-end-of-line (MEOL) processes require engineering knowledge that spans front- and back-end processing through to packaging, assembly and test. Consumer trends that are bringing about the need for Interconnectology to be adopted as a concept industry wide will be discussed.

Interconnectology – The Road to 3D

Simon McElrea
Invensas Corporation

BiTS Burn-in & Test Strategies Workshop

2014 BiTS Workshop
March 9 - 12, 2014

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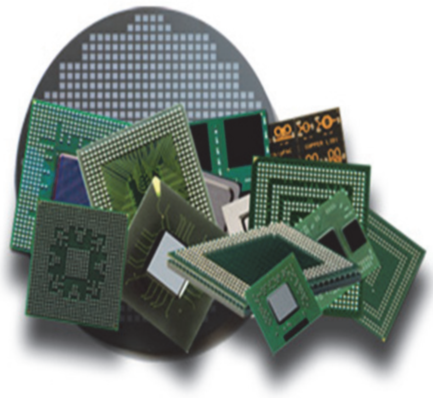
What Is Advanced/3D Packaging?



This Is... …But So Is This.

The level of Hardware Engineering now required to build the miniaturized & wearable devices of tomorrow, is Package Engineering (what Invensas calls Interconnectology).

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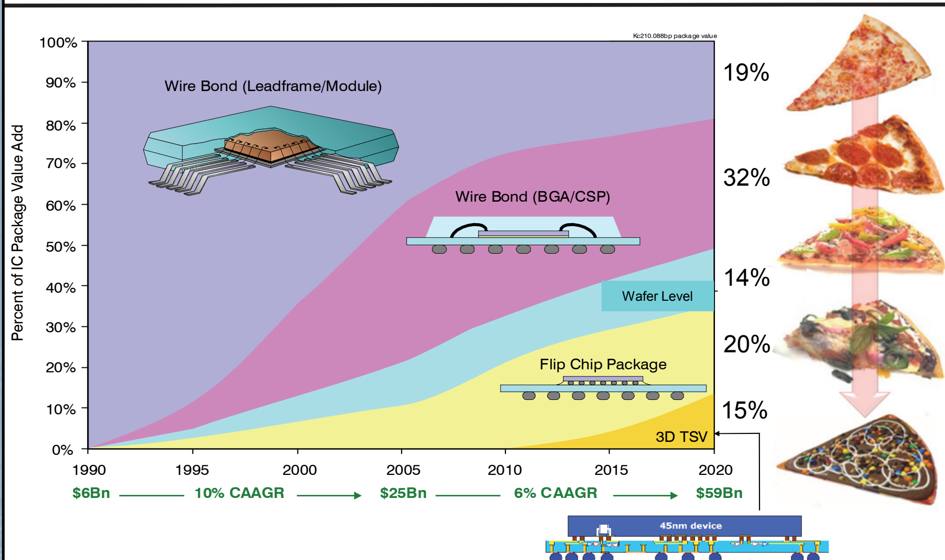
The Packaging Pizza Pie Chart (1990-2020)



PRISMARK, PIZZA HUT
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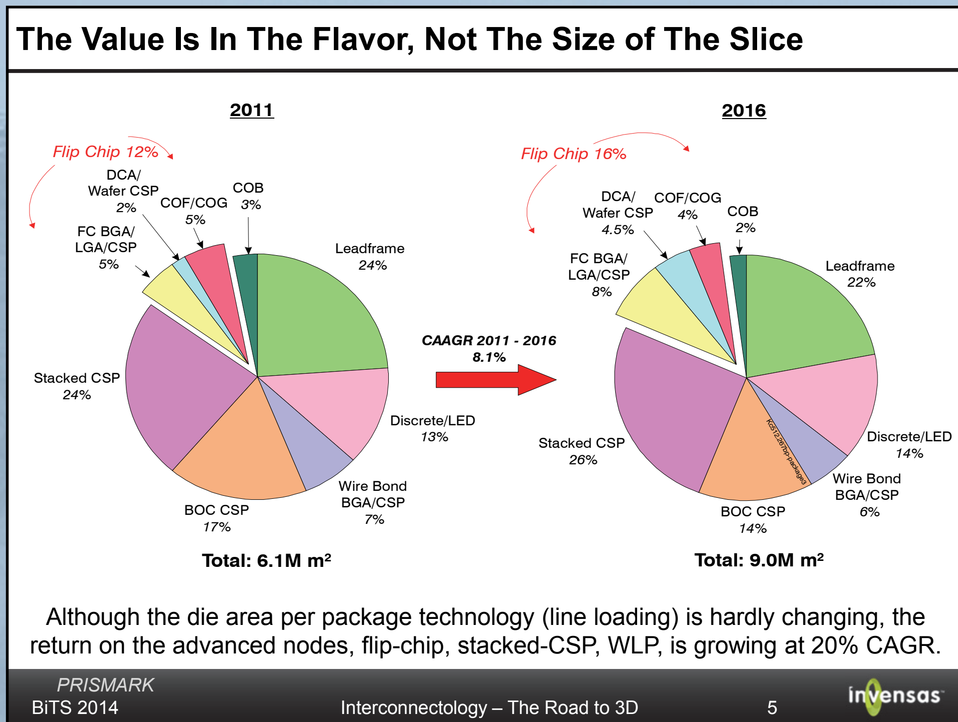
The Value Is In The Flavor, Not The Size of The Slice
2011
Flip Chip 12%
DCA/ Wafer CSP 2%
COF/COG 5%
COB 3%
FC BGA/ LGA/CSP 5%
Leadframe 24%
Stacked CSP 24%
Discrete/LED 13%
Wire Bond BGA/CSP 7%
BOC CSP 17%
Total: 6.1M m²
CAAGR 2011 - 2016 8.1%
2016
Flip Chip 16%
DCA/ Wafer CSP 4.5%
COF/COG 4%
COB 2%
FC BGA/ LGA/CSP 8%
Leadframe 22%
Stacked CSP 26%
Discrete/LED 14%
Wire Bond BGA/CSP 6%
BOC CSP 14%
Total: 9.0M m²
Although the die area per package technology (line loading) is hardly changing, the return on the advanced nodes, flip-chip, stacked-CSP, WLP, is growing at 20% CAGR.
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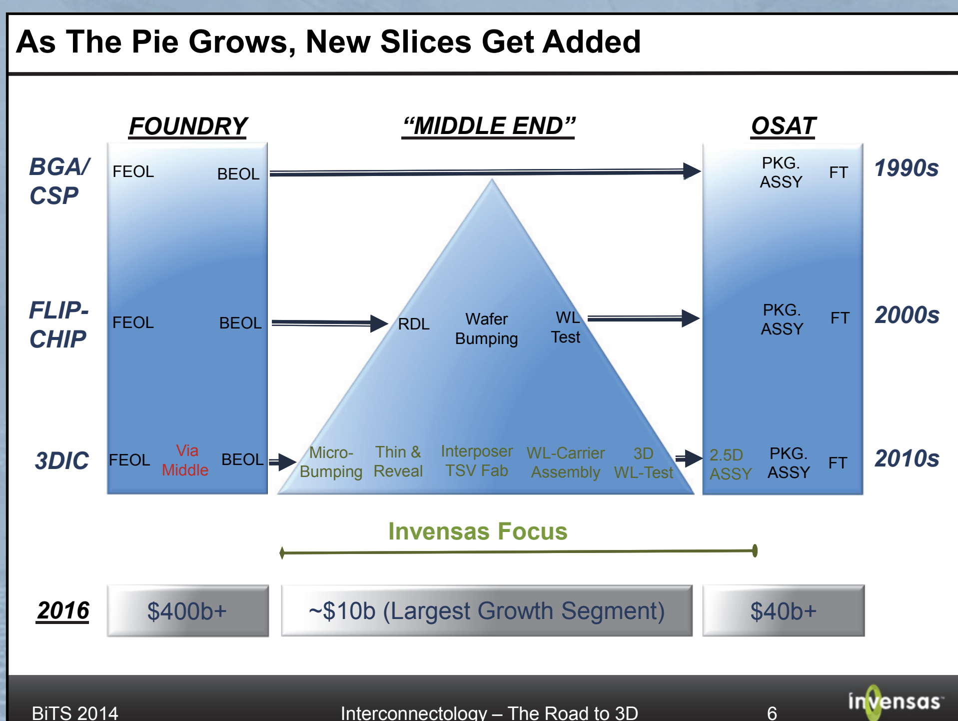
As The Pie Grows, New Slices Get Added
FOUNDRY
“MIDDLE END”
OSAT
BGA/ CSP
FEOL
BEOL
PKG. ASSY
FT
1990s
FLIP-CHIP
FEOL
BEOL
RDL
Wafer Bumping
WL Test
PKG. ASSY
FT
2000s
3DIC
FEOL
Via Middle
BEOL
Micro-Bumping
Thin & Reveal
Interposer TSV Fab
WL-Carrier Assembly
3D WL-Test
2.5D ASSY
PKG. ASSY
FT
2010s
Invensas Focus
2016
$400b+
~$10b (Largest Growth Segment)
$40b+
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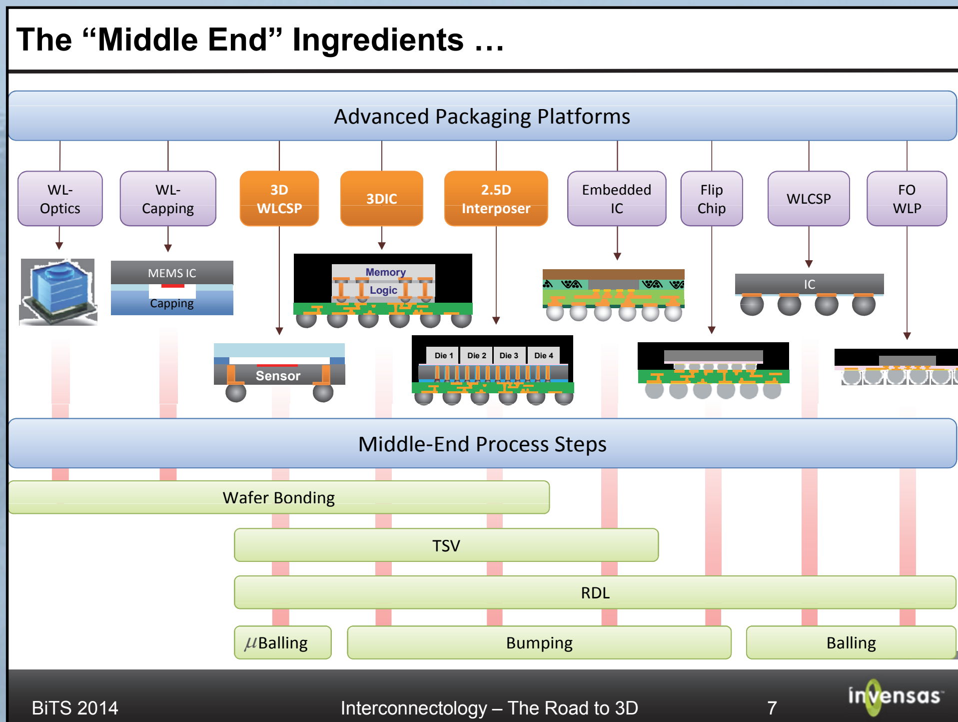
The "Middle End" Ingredients …
Advanced Packaging Platforms
WL-Optics
WL-Capping
3D WLCSP
3DIC
2.5D Interposer
Embedded IC
Flip Chip
WLCSP
FO WLP
MEMS IC
Capping
Memory
Logic
Sensor
Die 1
Die 2
Die 3
Die 4
IC
Middle-End Process Steps
Wafer Bonding
TSV
RDL
μBalling
Bumping
Balling
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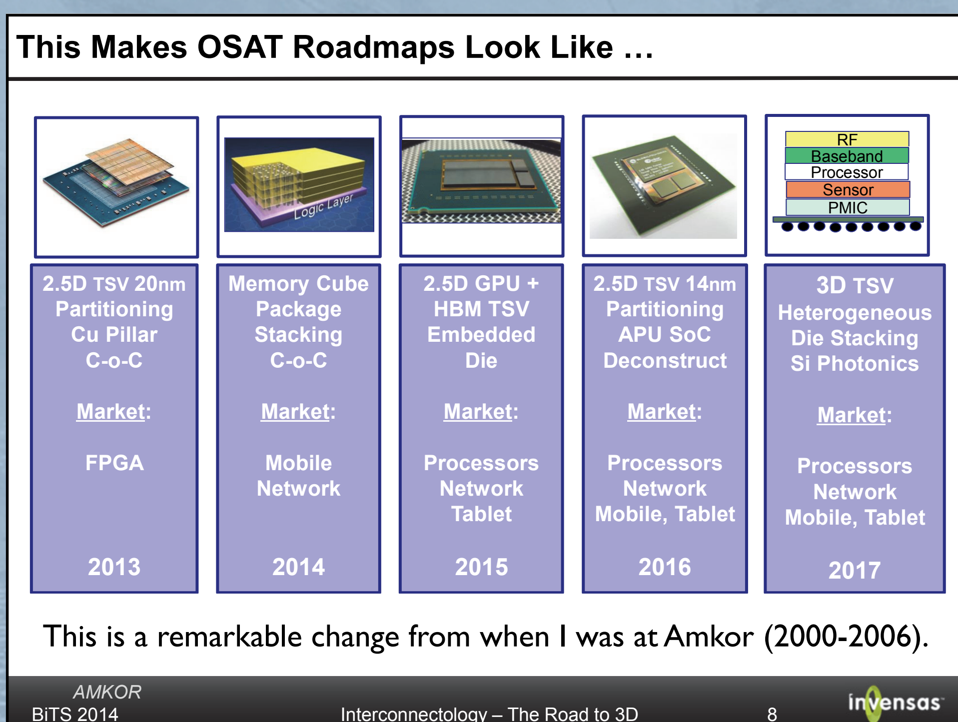
This Makes OSAT Roadmaps Look Like …
Logic Layer
RF
Baseband
Processor
Sensor
PMIC
2.5D TSV 20nm Partitioning Cu Pillar C-o-C
Market:
FPGA
2013
Memory Cube Package Stacking C-o-C
Market:
Mobile Network
2014
2.5D GPU + HBM TSV Embedded Die
Market:
Processors Network Tablet
2015
2.5D TSV 14nm Partitioning APU SoC Deconstruct
Market:
Processors Network Mobile, Tablet
2016
3D TSV Heterogeneous Die Stacking Si Photonics
Market:
Processors Network Mobile, Tablet
2017
This is a remarkable change from when I was at Amkor (2000-2006).
AMKOR
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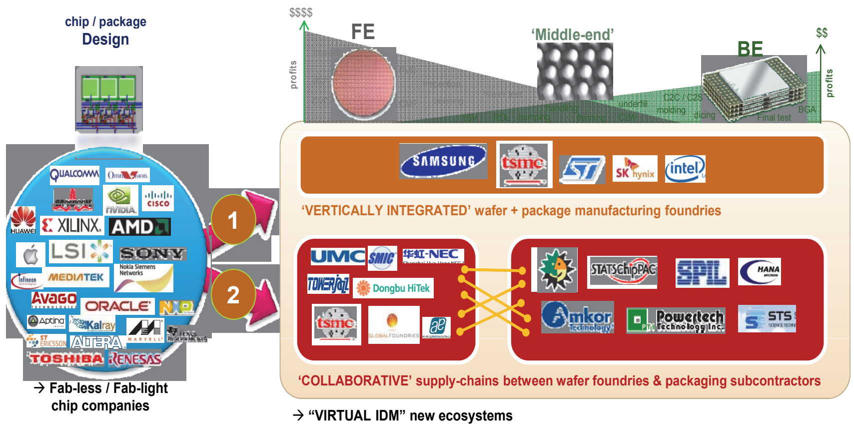
And It Makes Supply Chain Roadmaps Look Like …



YIKES!

YOLE
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And That's The Key …

"MIDDLE END"

The adoption curve depends on which players the supply chain (market) permits to own the new value-added elements.

History says: it's the model that provides the greatest sourcing flexibility to the end product owners.

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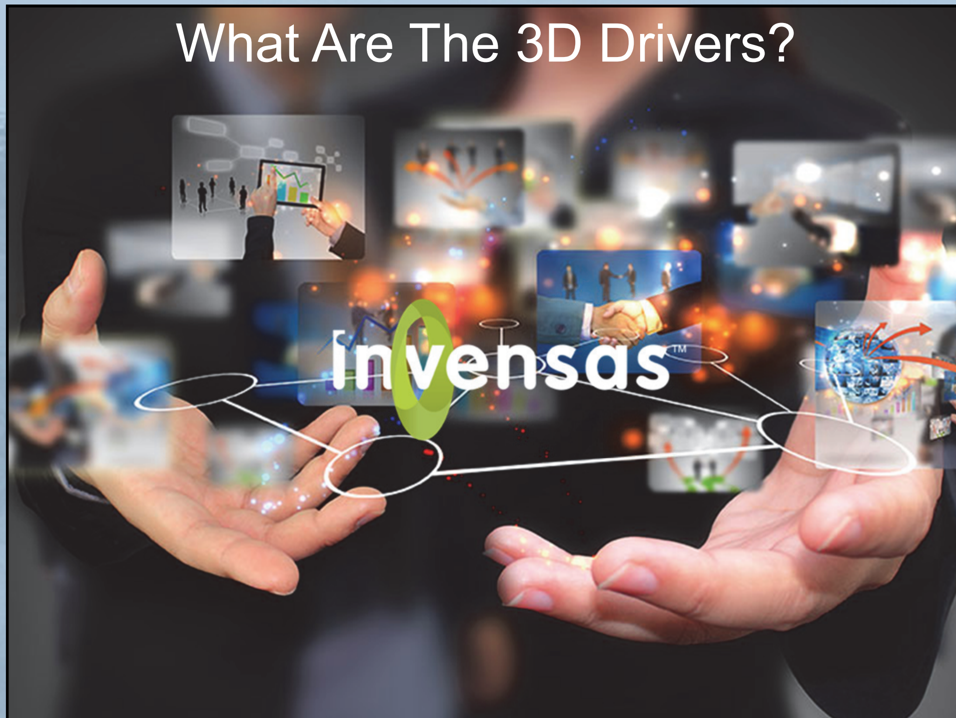
What Are The 3D Drivers?
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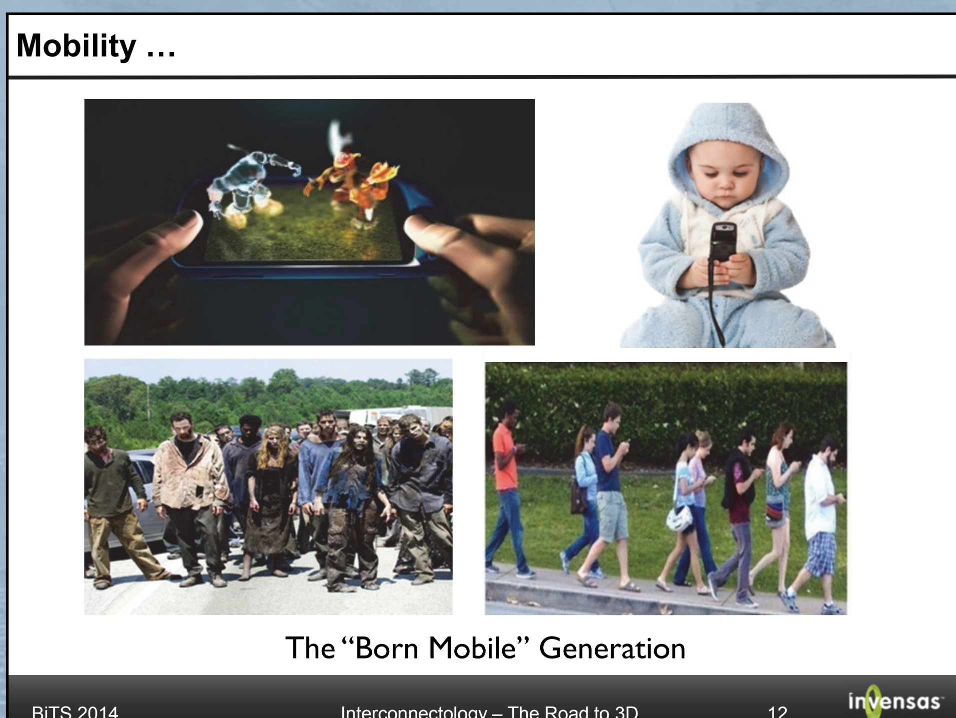
Mobility …
The "Born Mobile" Generation
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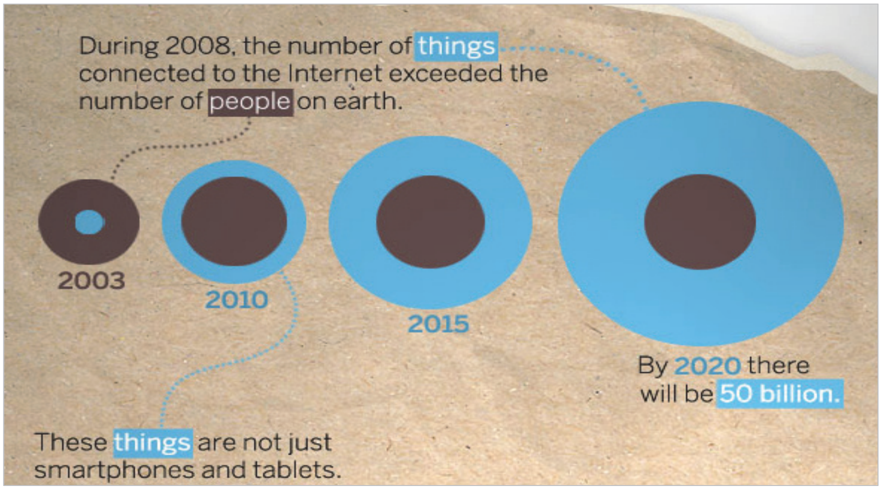
… and The Internet of Every Thing …



IDC

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How Many "Things"?

- 10^7 – Internet infrastructure – servers, networking…
- 10^8 - Cars; appliances
- 10^9 - PCs; smartphones; tablets; watches; TVs; people; clocks; radios
- 10^{10} – Headsets; peripherals; lights and switches; anything with a battery
- 10^{11} – Tags, tickets
- 10^{12} – Pills

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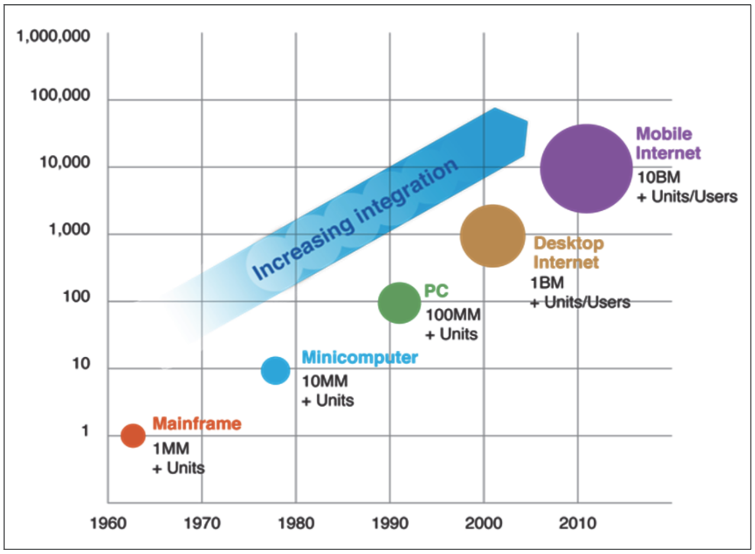
Yes, Its Exponential My Dear Watson



DR. MORRIS CHANG
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Speaking of Watson …

"By the end of this decade, the equivalent of Watson will fit in our pocket." – Dr. John Kelly

IBM
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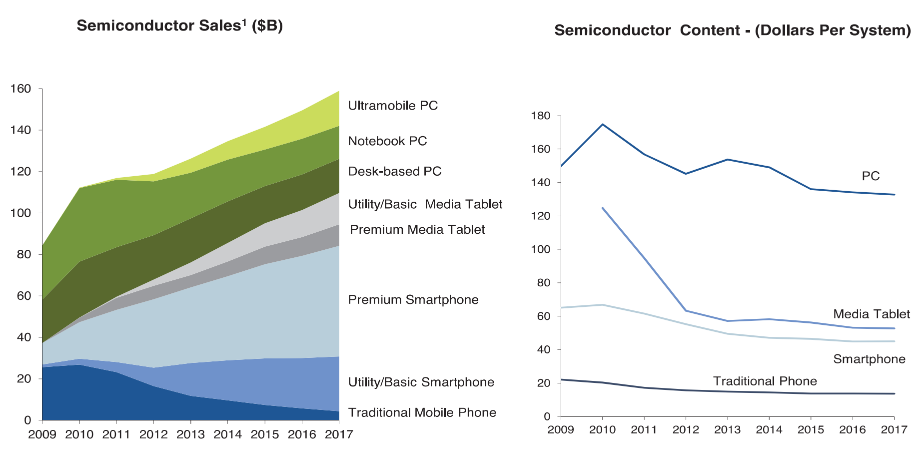
The New Normal: Lower Semiconductor Content/System



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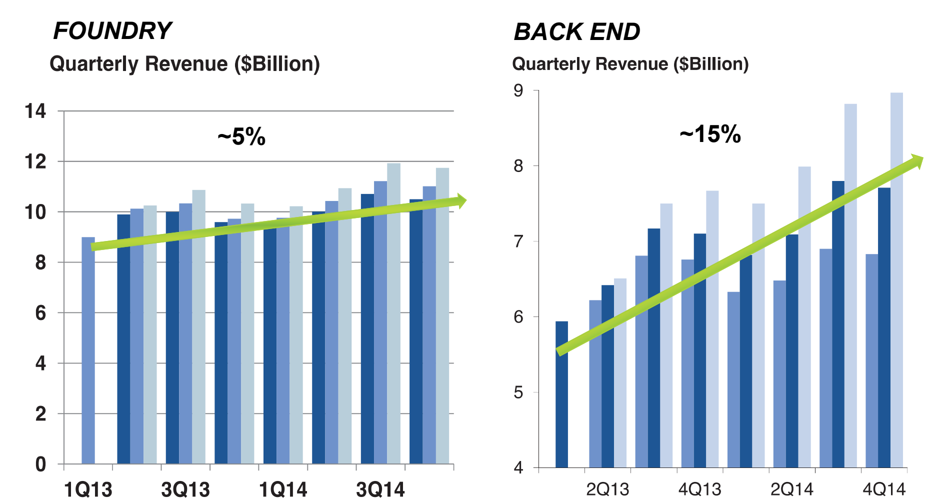
Front End vs. Back End Growth



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Your Back End Is Bigger Than You Think …
… And Your Middle End is Huge
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The Killer App That Created Advanced Packaging?
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The Mobile Phone, Of Course ...

The Mobile Phone Drove The Creation of the Stacked-Chip CSP Package, System-in-Package, Package-on-Package, the Wafer-Level & Fan-Out Wafer Level Package, along with a host of CMOS Image & Touch Sensor Packages, MEMS Sensor Packages, and 2.5/3DIC Solutions.

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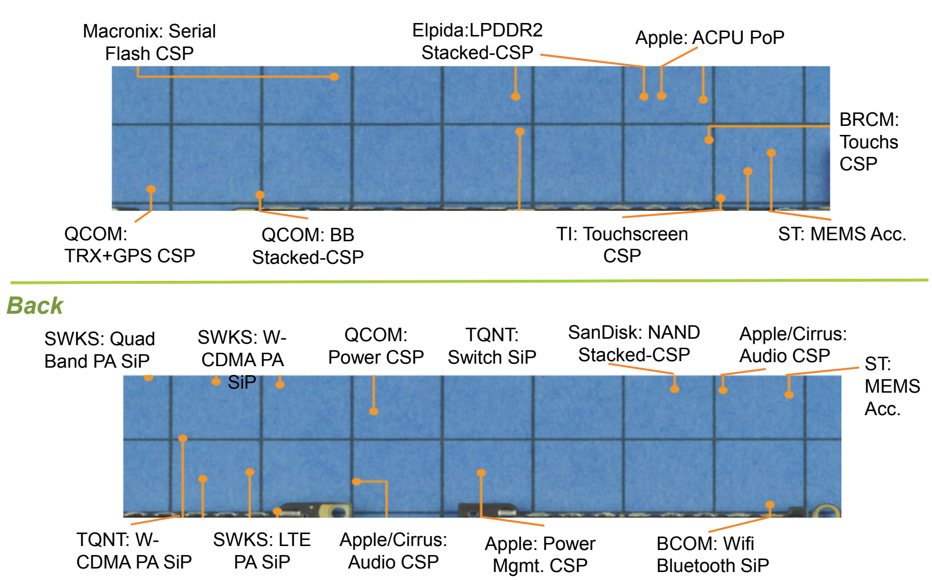
Advanced 3D Packaging Now Dominates The BOM



APPLE iPHONE 5s

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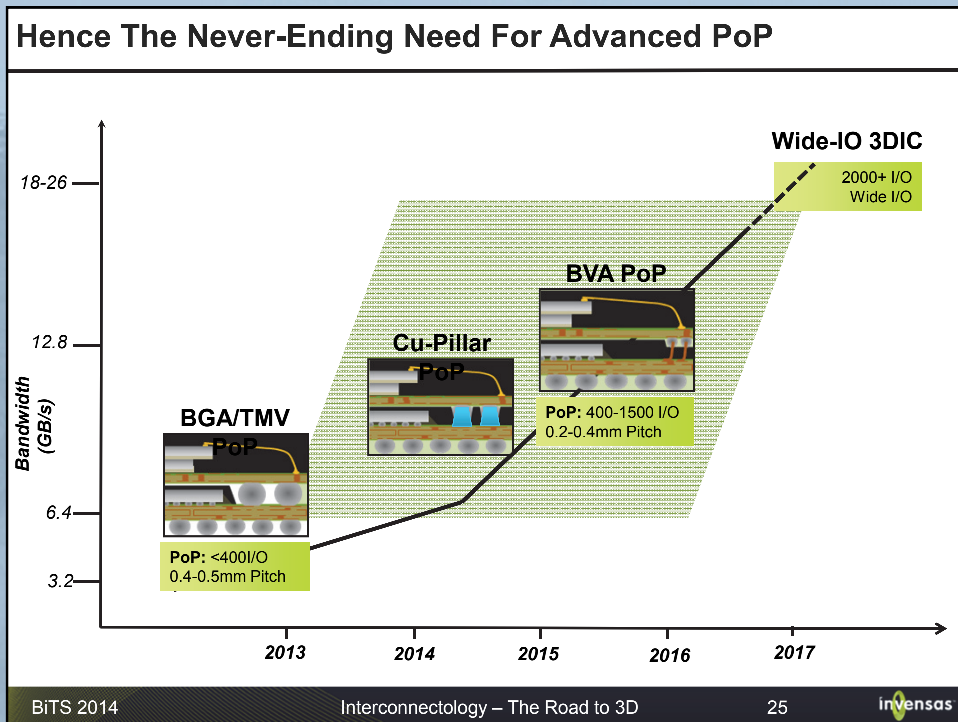
BOM Breakdown (By $)

Description	Package Type	Piece Cost	Cum. BOM Cost	Cum BOM %	Pin Count	Package Brand
Dual-Core Applications Processor	BGA-POP	$33.200	$33.200	21%	1564	Apple
Multimode Baseband Processor w/ Memory	BGA Stacked 2	$22.810	$56.010	36%	383	Qualcomm
Multichip Memory - 32 GB MLC iNAND Flash, Memory Controller	BGA Stacked 5	$17.620	$73.630	48%	60	SanDisk
Multichip Memory - 1 GB Mobile DDR2 SDRAM	BGA-POP-2	$5.220	$78.850	51%	272	Elpida
8 MP BSI CMOS Image Sensor	COB	$4.850	$83.700	54%	65	Sony
WiFi 802.11a/b/g/n / Bluetooth / FM Radio Module	MCP - 5 Chips	$4.610	$88.310	57%	52	Murata
GSM / W-CDMA / LTE RxD Transceiver + GPS	BGA	$3.910	$92.220	60%	196	Qualcomm
Stereo Audio CODEC	BGA	$3.150	$95.370	62%	140	Apple
3-Axis MEMS Gyroscope	MCP - 2 Chips	$2.980	$98.350	63%	16	STMicroelectronics
Power Management	BGA	$2.650	$101.000	65%	276	Apple
W-CDMA Band I & LTE Band IV Power Amplifier	MCP - 3 Chips	$1.920	$102.920	66%	31	Avago
W-CDMA Bands II & V Power Amplifier	MCP - 2 Chips	$1.530	$104.450	67%	31	Skyworks
1.2 MP CMOS Image Sensor	COB	$1.480	$105.930	68%	16	Sony
Diversity Rx Antenna Switch w/ SAW Filters	MCP - 2 Chips	$1.430	$107.360	69%	24	Murata
3-Axis MEMS Accelerometer	MCP - 2 Chips	$1.400	$108.760	70%	16	STMicroelectronics
Touchscreen Line Driver ?	Flip Chip, Solder	$1.380	$110.140	71%	99	TI
TFT-LCD Display Driver	Flip Chip, Adhesive	$1.250	$111.390	72%	1113	Renesas SP Drivers
Camera: Auto Focus	Module	$1.250	$112.640	73%	2	
Power Management	Flip Chip, Solder	$1.190	$113.830	73%	106	Qualcomm
Touchscreen Controller	Flip Chip, Solder	$0.980	$114.810	74%	56	Broadcom
W-CDMA Band VIII Power Amplifier	QFN	$0.880	$115.690	75%	14	TriQuint
RF Antenna Switch	QFN	$0.880	$116.570	75%	20	Murata
Audio Amplifier	Flip Chip, Solder	$0.600	$117.170	76%	42	Apple
Port: Lightning	Connector	$0.500	$117.670	76%	10	
Quad-Band GSM Power Amplifier	MCP - 2 Chips	$0.440	$118.110	76%	14	Skyworks
GPS Front-End Module	DFN	$0.320	$120.190	78%	12	Skyworks
Display Port Multiplexer ?	Flip Chip, Solder	$0.320	$120.510	78%	36	NXP Semiconductor
		TOTAL $	154.94			

3D Packaging (Package on Package & Stacked Die CSP) accounts for over 2/3 of the packaged-IC BOM cost (~$80).

Why The PoP Love Affair?

- **Each device is packaged separately**
  - Mature technology and infrastructure
- **Each component is tested and burned-in separately at the package level**
  - Mature technology and infrastructure
- **No margin stacking**
  - Each component is sourced separately by OEM or EMS provider
- **Joining technology widely available**
  - Utilizes standard SMT process and existing manufacturing platform
- **Joining process is very high yielding**
- **Relatively clear ownership of defect liability**
  - Failure analysis methods are mature


Hence The Never-Ending Need For Advanced PoP
Bandwidth (GB/s)
18-26
12.8
6.4
3.2
2013
2014
2015
2016
2017
BGA/TMV PoP
PoP: <400I/O
0.4-0.5mm Pitch
Cu-Pillar PoP
BVA PoP
PoP: 400-1500 I/O
0.2-0.4mm Pitch
Wide-IO 3DIC
2000+ I/O
Wide I/O
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But Why 3DIC?
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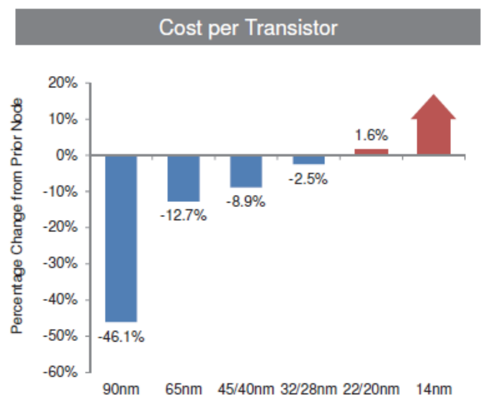
Why 3D?: It's Mostly About Cost



- For the First Time Ever, Wafer Price Increases Eliminating Scaling Benefits at 22/20nm
- Substantial Process R&D
- Increased Equipment Costs
- Lithography Now 50% of Wafer Costs

Moore's Law is a Law of Economics.

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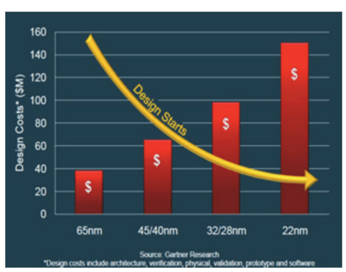
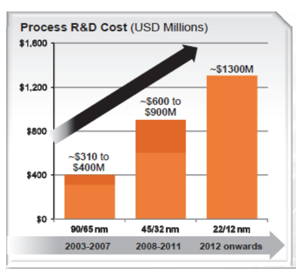
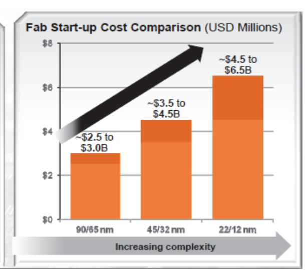
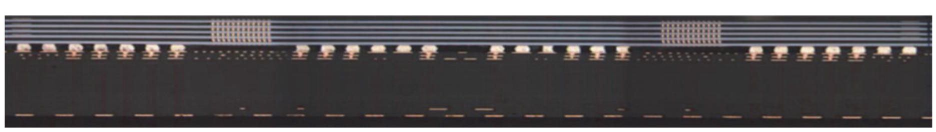
But It's Also About Cost … Cost of Scaling









The cost per fab, R&D cost per node, and design cost per device, grow beyond a tipping point below 20nm. 3DIC design architecture allows technologies to be built "at the right node" and then stacked, which is much more cost-effective overall, and not exclusive to 2-3 players.

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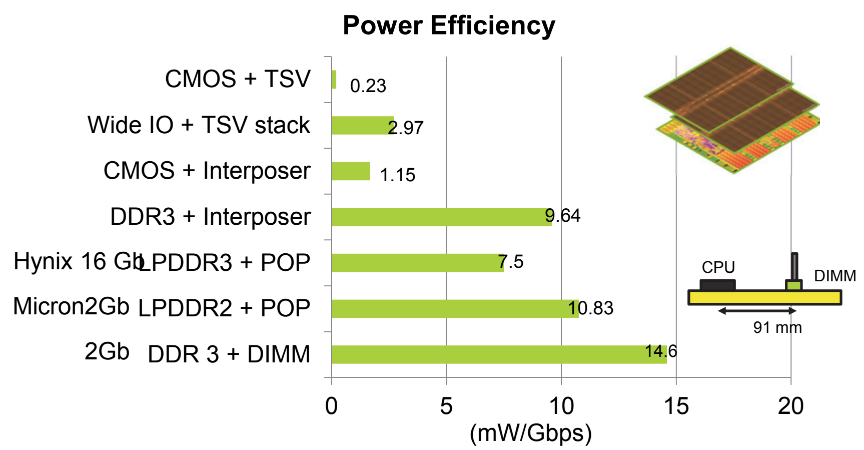
Its Also About Power



Orders Of Magnitude Power Savings (Mobile Battery Life or Data Center Cost) Are Possible in 3DIC

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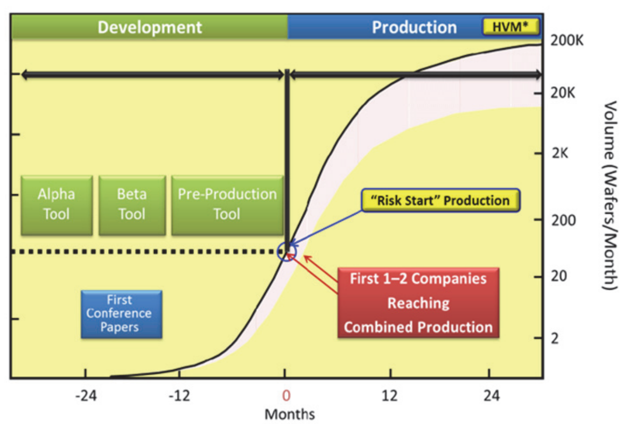
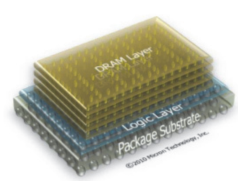
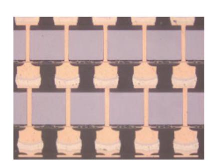
So Are We There Yet?







Fewer leading IDM companies requires adaption of definition to allow one IDM company or a foundry representing many fabless companies to lead a technology production ramp timing

By ITRS' definition, We Are There! Between the FPGA, Memory Cube, Wide-IO and Interposer-based products we are at this inflection point!

ITRS
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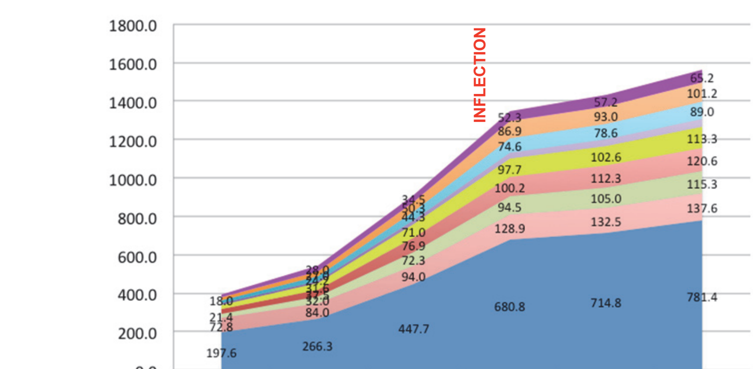
So We Said The Supply Chain Was The Key Indicator …



	2012	2013	2014	2015	2016	2017
Wet Clean (TSV)	13.2	28.0	34.5	52.3	57.2	65.2
CVD	18.0	27.0	50.3	86.9	93.0	101.2
CMP	15.1	24.2	44.3	74.6	78.6	89.0
Dry Strip (TSV)	7.0	12.0	20.3	31.2	34.0	38.9
Dry Etch (TSV)	22.0	31.6	71.0	97.7	102.6	113.3
Sputtering (TSV)	25.4	37.5	76.9	100.2	112.3	120.6
ECD (TSV)	21.4	32.0	72.3	94.5	105.0	115.3
Die And Wafer Bonders	72.8	84.0	94.0	128.9	132.5	137.6
Wafer Level Package Tools	197.6	266.3	447.7	680.8	714.8	781.4

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3DIC Equipment Suppliers Surveyed

Process Step	Leading Equipment Providers
Wafer Thinning/Stress Reduction	Disco, TOK, Accretech, Lam
Via Patterning (Lithography/Stepper)	EVG, SUSS, ASML, Nikon, Canon, Ultratech, Tamarack, Anvik
Via Etch (DRIE/Bosch)	SPTS, Applied, Lam, Hitachi High Tech, ULVAC
Laser Drill	ESI, Hitachi, Mitsubishi
Stripping/Cleaning	Applied, Novellus, Lam, Applied, TEL
Via Fill Barrier/Seed Layers (Deposition/Coating/CVD)	Oerlikon, Novellus, NEXX/TEL, Applied, SPTS, EVG, Hitachi High Tech, EEJA
Via Fill Plating	Applied, NEXX/TEL, SPTS, Ebara, Novellus, EEJA
Stripping/UBM Etch	Semitool, Lam
CMP	Applied, Novellus, Ebara, Accretech
Carrier Bonding	EVG, SUSS, TOK, AML
Wafer Thin to Expose Vias	Disco, TOK, Accretech
RDL	SUSS, Ultratech, Novellus, EVG, Novellus, NEXX/TEL
Dicing	**ESI, Alcatel, Accretech, Disco**
Carrier Debonding	**EVG, SUSS, TOK, ASML**
Die to Wafer Bonding	**Datacon/BESI, Palomar, K&S, PanasonicFA, EVG, ASML, Finetech, Hesse & Knipps, PacTech, Hitachi High Tech, SUSS**

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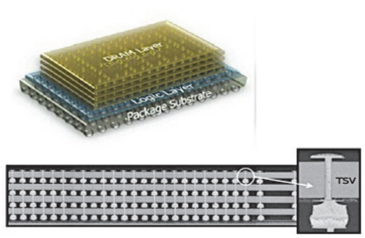
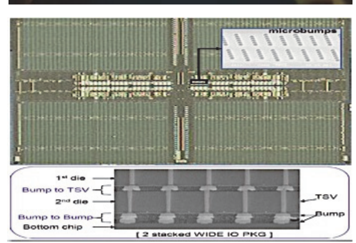
And There Are Now Two Main HVM Market Drivers …



New Enterprise/Storage Standard
1024bit wide, 20x Bandwidth, 20% Power Use, 40/50um pitch TSV.



New Mobile DRAM Standard
512bit wide, 1200 I/O per chip, 40/50um pitch TSV& μBumps.

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The 3DIC Market is Of Course Much Broader Than That …

3D TSV Applications

Imaging
- WLP CIS
- BSI CIS
- 3D integrated CIS
- Wafer level auto-focus

MEMS & Sensors
- Gyros
- Acceleros
- Pressure sensors
- Si-micro
- FBAR filters
- Oscillators
- μProbes
- μFluidic / IJ
- μValves
- Fingerprint sensors
- IR-bolometer
- Opto *(laser, VCSEL)*
- Micro-mirrors

HB-LED
- Mobile μ-Flash
- Automotive
- Projection engine
- General Lighting

RF, Power, Analog & Mixed Signal
- PA
- MOSFET
- IGBT
- IPD
- DC-DC converters

Stacked memories
- Stacked DRAM
- StackedNAND Flash
- StackedNOR / PCRAM

Logic 3D-SiP/SoC
- **3D SiP**: Wide IO BB; CPU / GPU; FPGA; High. Perf ASICs
- **3D SoC**: Baseband / DSP; MCU / Processors; Touchscreen controller; Low-end ASICs; PMIC

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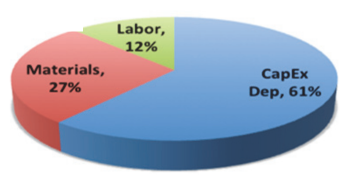
But Who Pays? The IDM, Foundry, Fabless or OSAT?

- TSV processing requires equipment sets traditionally seen in the wafer fab. These include lithography, etch and clean and deposition processes.
  - Cost of these tools range from $1.5 to more than $8 million/system.
  - Wafer grinding tools for via exposure needed for via first and middle processes.
- Additional tools include high-cost, low throughput wafer bonders.
  - (ASP +$6m, TP 20 wafers/hour)
  - Challenge of wafer bonding extremely thin 450mm wafers beyond the 2017 timeframe.
- Cap-Ex requirements will segment the SATS companies and reduce competition in this market.



- Or Will It Be Apple, Google, Microsoft, Amazon, Facebook, etc.? …

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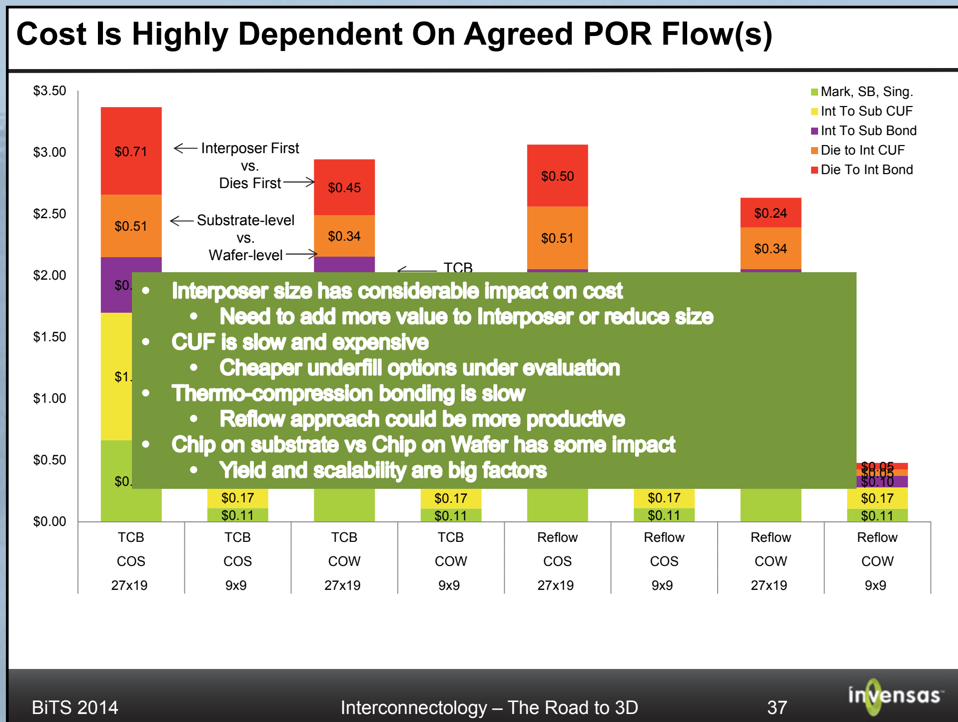
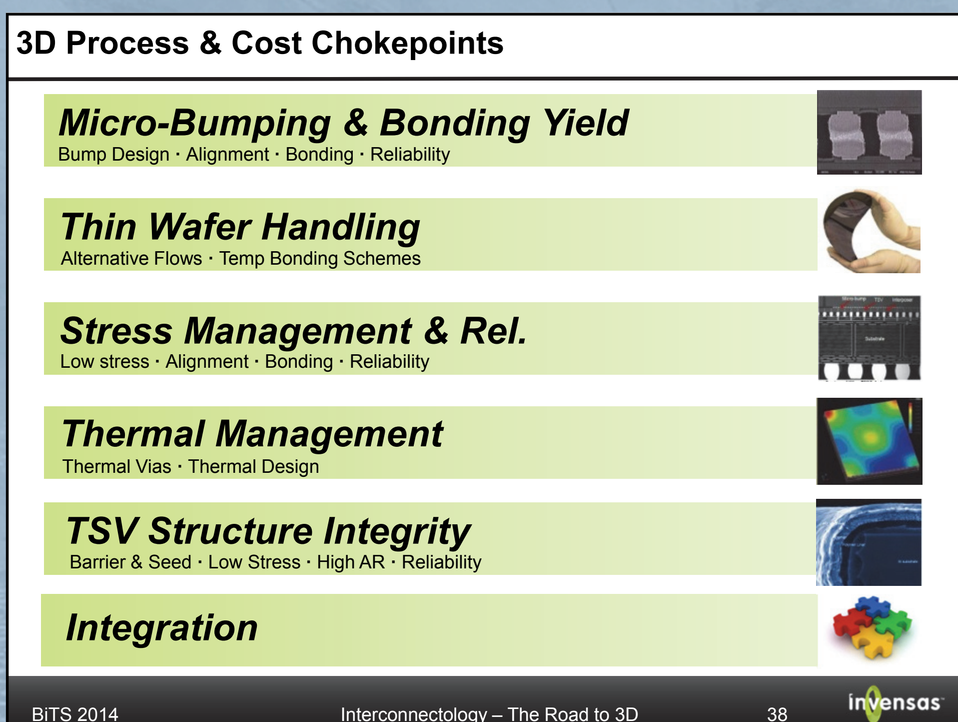
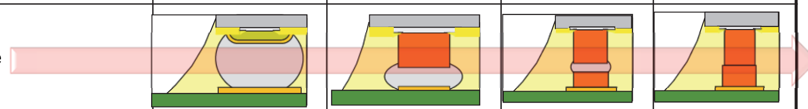
Keynote Address





Copper Transition: It's Always About Copper …

Bonding Method	C4 FC (Contolled Collapse Chip Connect)	C2 FC (Chip Connect)	TC/LR (Local Reflow) FC	TC FC
Bond Structure				
Major Bump Pitch Range at Application	> 130 um	140 um ~ 60 um	80 um ~ 20 um	< 30 um
Bonding Method	Conventional Reflow	Reflow with Cu pillar	Thermal Compression with Cu pillar	Thermal Compression
Bump Metallurgy	Solder (SnAg or SnAgCu)	Cu + Solder (SnAg or Sn)	Cu + Solder (SnAg or Sn) Cap	- Cu - Metal/Metal
Bump Collapse	Yes	No	No	No
Underfill Method	- Capillary - No flow	- Capillary - No flow - Wafer Level	- No flow - Wafer Level	- No flow - Wafer Level

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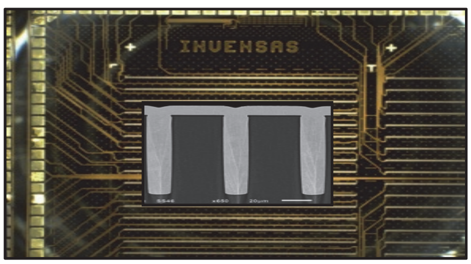
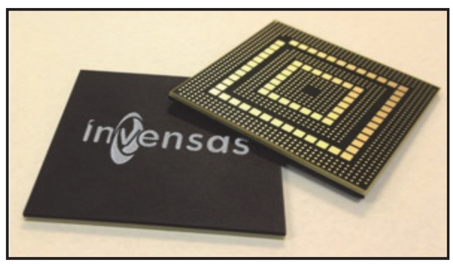
Invensas: Fun With 3D





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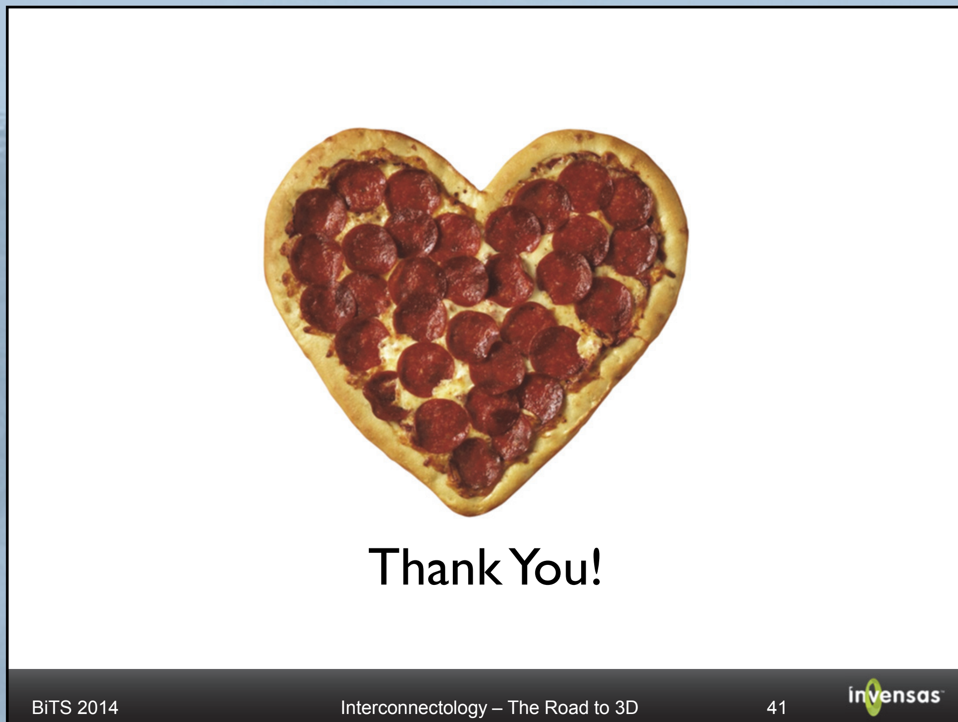
Thank You!
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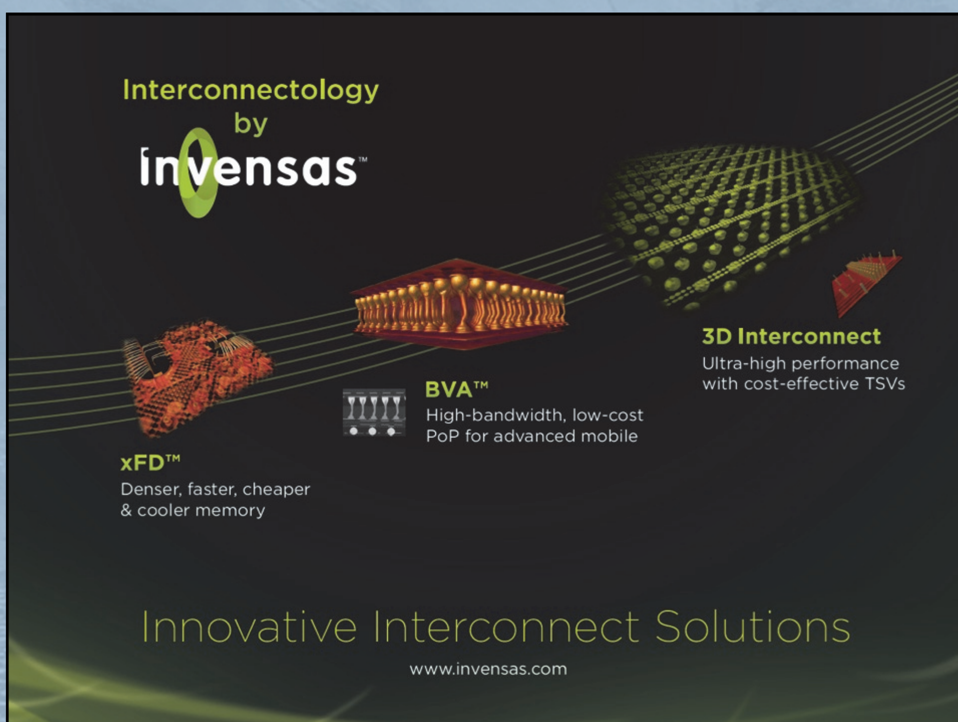
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