Distinguished Speaker

Sunday 3/9/14 8:30pm
Kiva Ballroom

PACKAGING AND INTERCONNECT TRENDS: QFN, WLCSP, FINE PITCH AND MODULAR/3D SOLUTIONS

by

Brandon Prior
Senior Consultant
Prismark Partners

***Brandon Prior, Senior Consultant at Prismark Partners**, returns to the BiTS Workshop with an overview of the global packaging market, focusing on emerging and fast growth package solutions. Be prepared for a glimpse of some cool product teardowns he'll use to illustrate his talk.*

ABSTRACT

This overview of the global packaging market will focus on emerging and fast growth package solutions. In his presentation Mr. Prior will review where package miniaturization and modularization has taken us so far, and where it will lead in the next 5 years. Teardowns of high density boards and packages will be used to illustrate key points.

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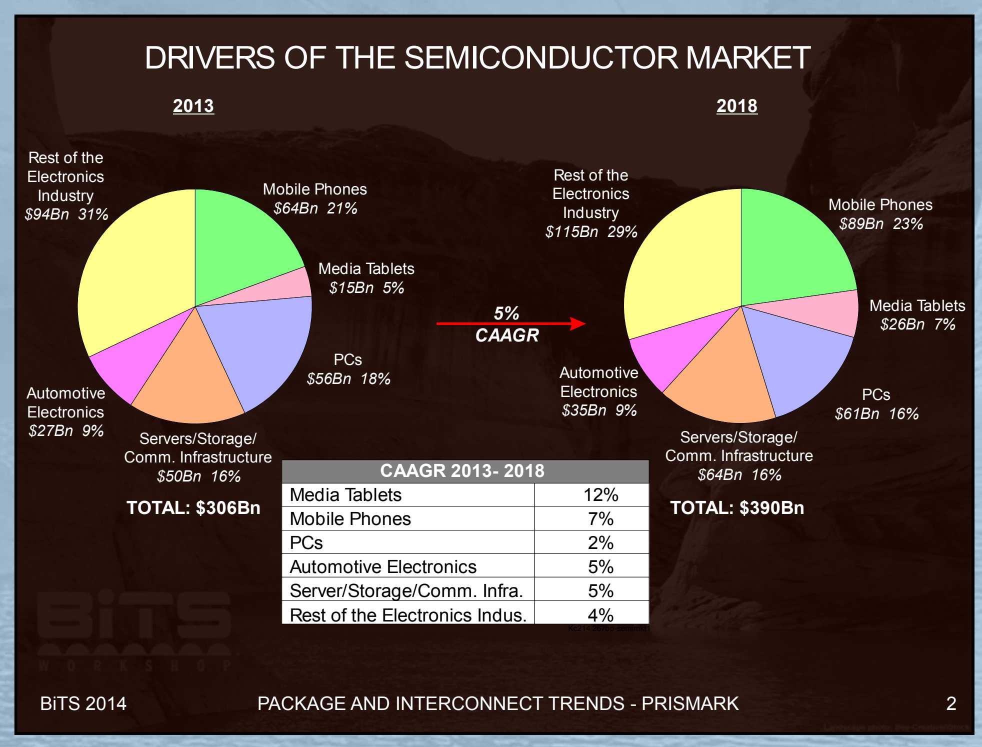
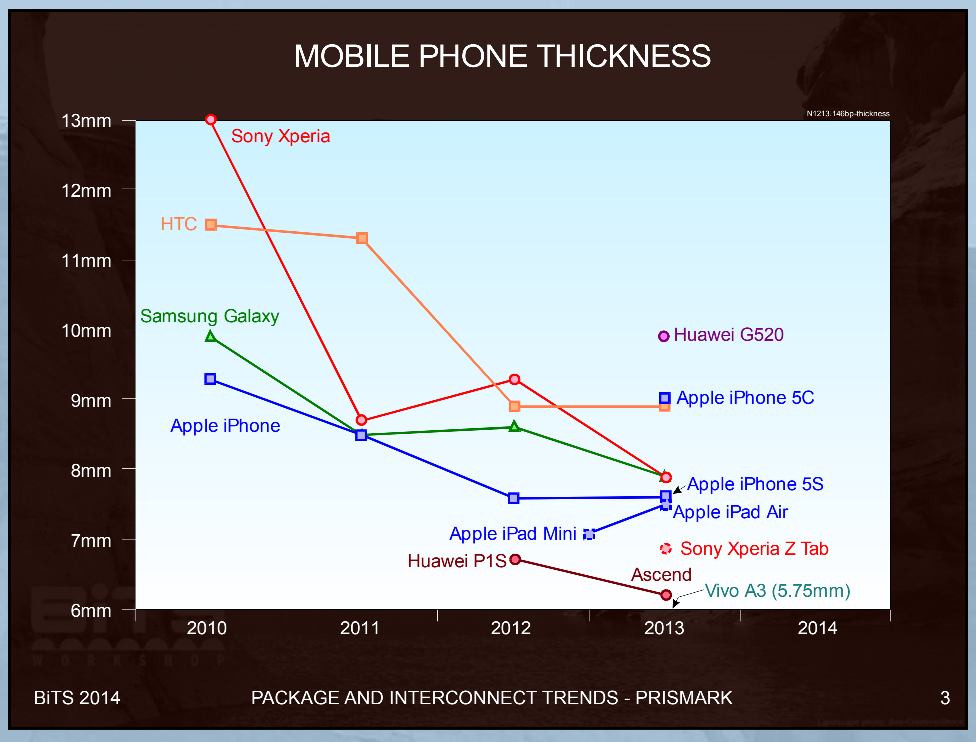
PACKAGE AND INTERCONNECT TRENDS

Brandon Prior
Prismark Partners LLC

2014 BiTS Workshop
March 9 - 12, 2014



CAAGR 2013- 2018	
Media Tablets	12%
Mobile Phones	7%
PCs	2%
Automotive Electronics	5%
Server/Storage/Comm. Infra.	5%
Rest of the Electronics Indus.	4%



MOBILE PHONE THICKNESS
13mm
12mm
11mm
10mm
9mm
8mm
7mm
6mm
2010
2011
2012
2013
2014
Sony Xperia
HTC
Samsung Galaxy
Apple iPhone
Huawei G520
Apple iPhone 5C
Apple iPhone 5S
Apple iPad Air
Apple iPad Mini
Sony Xperia Z Tab
Huawei P1S
Ascend
Vivo A3 (5.75mm)
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APPLE iPhone 5S SMARTPHONE
1013.4/407bp
1. Apple A7 1.3GHz Dual-Core Processor/Memory PoP (FCCSP)
2. SK Hynix 16GB NAND (WBCSP)
3. Dialog Power Manager (FCCSP)
4. Qualcomm MDM9615M Baseband Processor (FCCSP)
5. Qualcomm PM8018 Power Manager (WLCSP)
6. Qualcomm WTR1605L RF Transceiver (WLCSP)
7. Murata Filter+ Switch Module
8. Murata Filter Module
9. Skyworks SKY77810 Dual-Band PA+ Duplexer Module
10. Avago A792503 Dual-Band PA+ Duplexer Module
11. Skyworks SKY77572 Dual-Band PA+ Switch Module
12. TriQuint TQF6414 Dual-Band PA+ Duplexer Module
13. RFMD RF3763 Dual PA+ Duplexer Module
14. Skyworks SKY77496 Band PA+ Duplexer Module
15. Murata WLAN/BT Module (BCM4334) (WLCSP)
16. Skyworks GPS FEM
17. Cirrus Logic Audio Codec (WLCSP)
18. Cirrus Logic Audio Amplifier (WLCSP)
19. Broadcom Touch Controller (WLCSP)
20. TI Touch Controller (WLCSP)
21. Apple M7 Processor (by NXP) (WLCSP)
22. ST MEMS Gyroscope
23. Bosch MEMS Accelerometer
24. AKM MEMS Compass (WLCSP)
• 10 Layer PCB with 50µm L/S
– 0.4mm pitch CSP with 1300 I/O
– 01005 passives
– Near 100% utilization of PCB space
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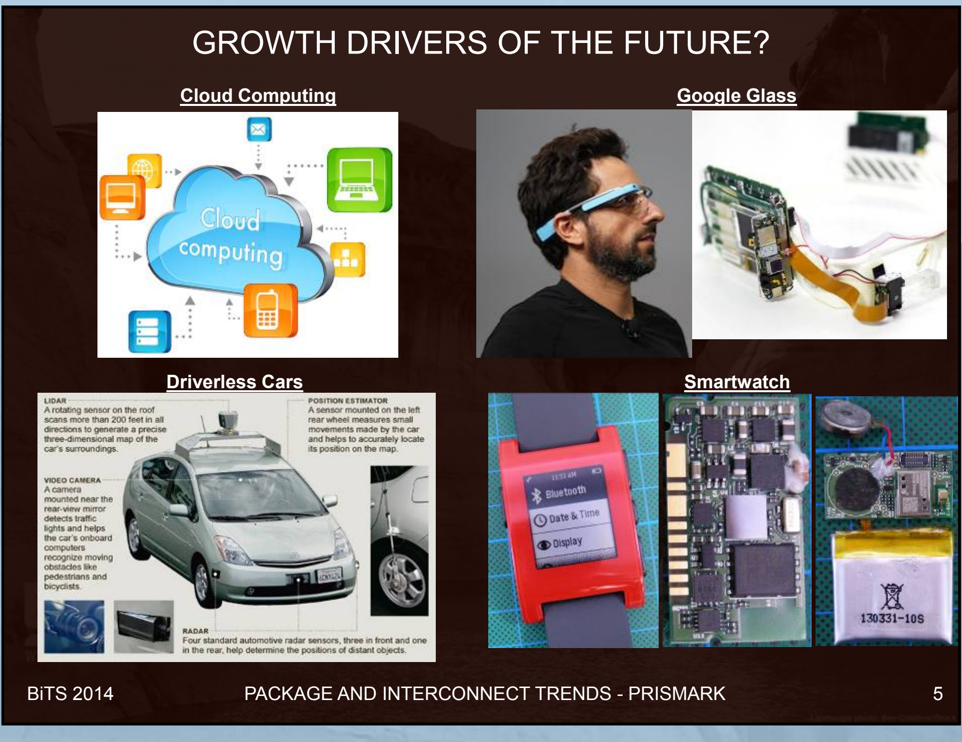
GROWTH DRIVERS OF THE FUTURE?
Cloud Computing
Cloud computing
Google Glass
Driverless Cars
Smartwatch
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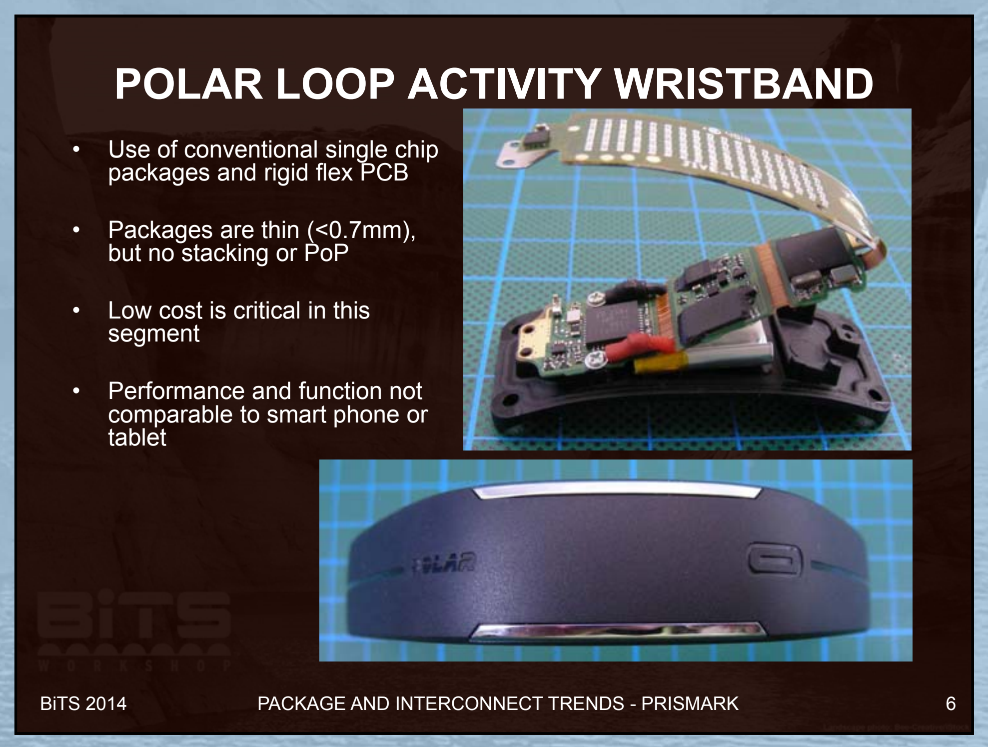
POLAR LOOP ACTIVITY WRISTBAND
• Use of conventional single chip packages and rigid flex PCB
• Packages are thin (<0.7mm), but no stacking or PoP
• Low cost is critical in this segment
• Performance and function not comparable to smart phone or tablet
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IC PACKAGE UNIT GROWTH

Package Type (Bn Units)	2011	% of Total	2013	2018	% of Total	CAAGR 2013-2018
Traditional Leadframe (SO, TSOP, QFP)	101	54%	102	108	40%	1.2%
QFN	21	11%	27	56	21%	16%
Wire Bond CSP (includes stacked & BOC/DRAM)	28	15%	27	29	11%	0.9%
Wire Bond BGA (> 19mm package size)	1.1	0.6%	0.9	0.8	0.3%	-2.3%
Wire Bond Bare Die (COB)	11	6%	12	16	6%	5.3%
Flip Chip CSP (includes DRAM)	1.5	0.8%	4.7	14	5%	25%
Flip Chip BGA/PGA/LGA (19mm Package Size)	1.1	0.6%	1.1	1.1	0.4%	0%
Wafer CSP	15	8%	19	35	13%	13%
COF/COG for Display Drivers	7.9	4%	8.6	11	4%	4.1%
TOTAL	**186.7**	**100%**	**202.4**	**269.8**	**100%**	**5.9%**

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PACKAGE SIZE REDUCTION AND SYSTEM IN PACKAGE (SiP)

- System Level Size Reduction
  - Mobile Consumer Electronics (Notebooks, Media Tablets, Smartphones, etc.) are representing an ever increasing portion of electronics value, and have been driving package roadmaps for the last fifteen years
  - Although system size is no longer decreasing dramatically, the area and volume allocated to PCB assembly is getting squeezed out in favor of larger battery, display, and overall thinner systems
- Package Size Reduction
  - Array Packages and Pitch reduction (0.5 → 0.4 → 0.3 → 0.25mm)
  - Wafer Level CSP – the "Package-less" Package
  - QFN – "leadless" packages using low cost leadframe and wirebond technology
- SiP Approaches
  - Adoption of stacked die and package stacking was first phase of 3D
  - 3D TSV and Silicon Interposers will be the "package" challenge over the coming decade

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QFN VS. WLCSP

- Both QFN and WLCSP package solutions have taken share from conventional SO packages – both offer
  - Smaller size
  - Lower cost
  - Better electrical performance
- QFN was initially successful across consumer/portable devices
  - Today, often displaced by WLCSP, modules, or move to CSP
  - QFN ramp now driven across all sectors as inspection/test concerns are solved
  - Multi-row QFN remains niche, but gaining traction
- WLCSP limitations remain
  - Die size and I/O limited
  - Fan out may open for more options
- QFN and WLCSP are often preferred packages by device suppliers due to low cost. Decision to use one over another is driven by cost and end-customer preference.
  – WLCSP is more cost effective for smaller die size and high I/O density. However, may be pitch limited
  – QFN looks more like standard package, and therefore has more traction as of 2013.

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TRANSITION TO 0.4mm PITCH PACKAGES

- Leadframe packages (TSOP, QFP) have used 0.4mm pitch for a long time
  - QFN, FBGA, and WLCSP packages in high volume production at 0.4mm and 0.35mm
  - Sub-0.4mm packages used in limited applications thus far
- All subcons and leading QFN users offering 0.4mm pitch designs
  - 0.35mm pitch availability from Carsem, Fairchild, NXP, and others
- Reliability/feasibility testing ongoing at OEMs and package assemblers
  - Wafer CSP at 0.3mm or below
  - CSP at 0.3 and 0.35mm for high leadcount devices
- Demand for sub-0.4mm pitch packages
  - Prismark forecast calls for > 28% of CSP/WLCSP to be 0.4mm or less pitch by 2018
  - Challenges remain PCB routing and assembly yield/process/ materials at 0.3mm pitch and below

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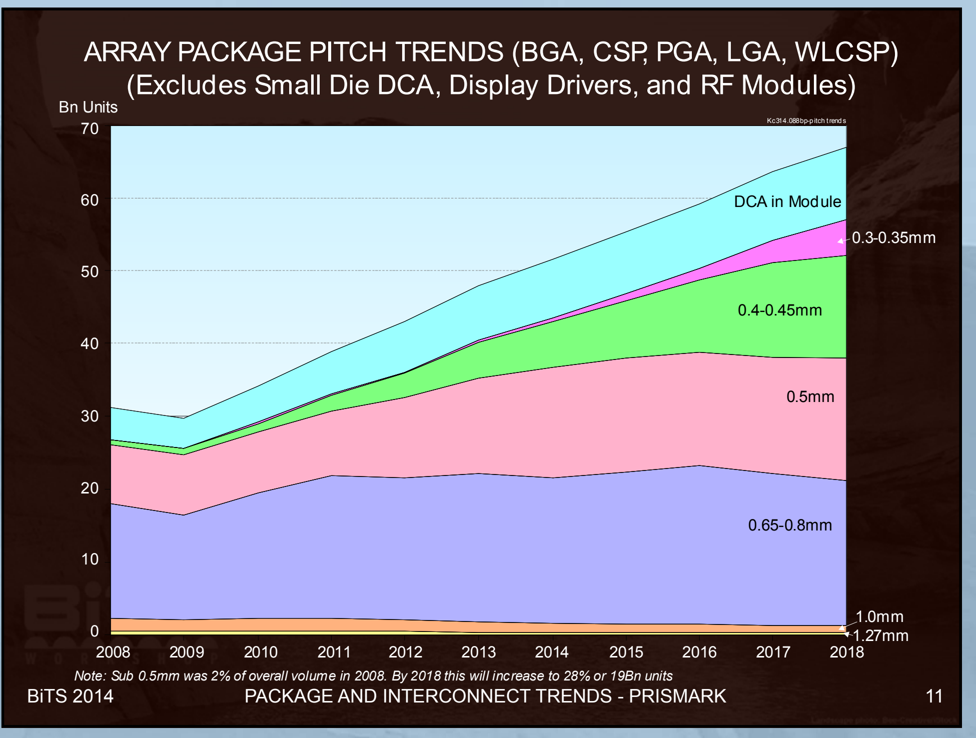

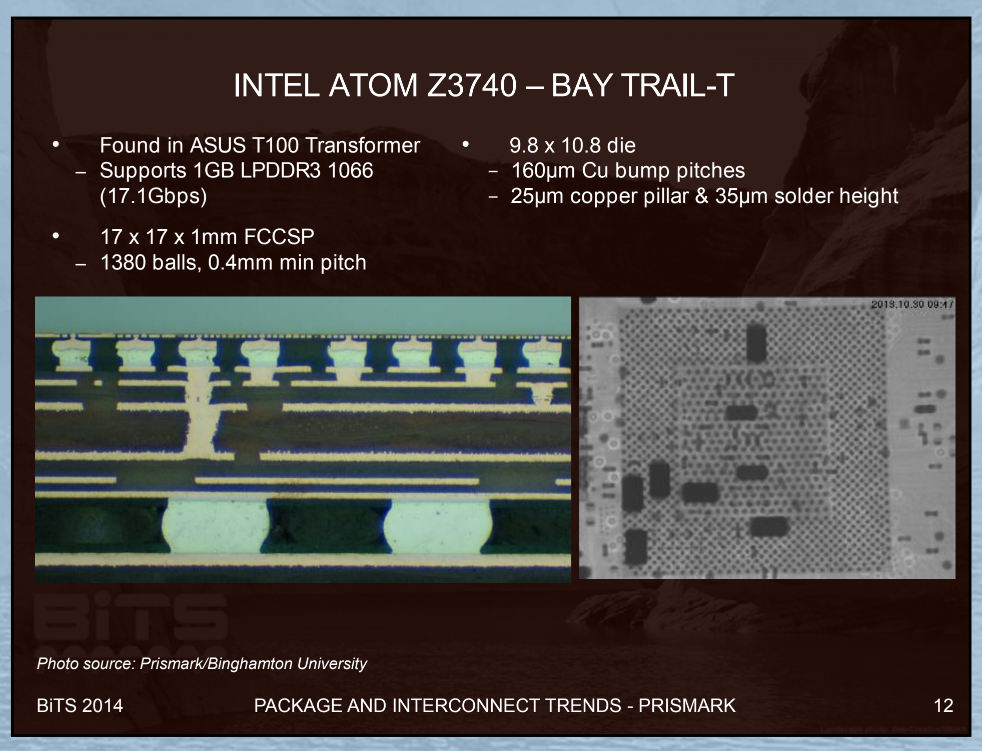

1013.6/193mvc
QUALCOMM SNAPDRAGON 800 MSM8974
• 15 x 15mm PoP, 1.45mm high
• Bottom Package - 1,005 balls, staggered rows, 0.6mm pitch
– Processor flip chip die, 100µm thick, 11 x 11mm
– About 3,600 bumps, 150µm pitch, 50µm height
– With PCB embedded capacitors
• Top Package - 216 balls in two peripheral rows, 0.5mm pitch
– Four memory die, wire bonded, 40µm thick, 9 x ?mm
– Die attach film between die
Photos source: Prismark/Binghamton University
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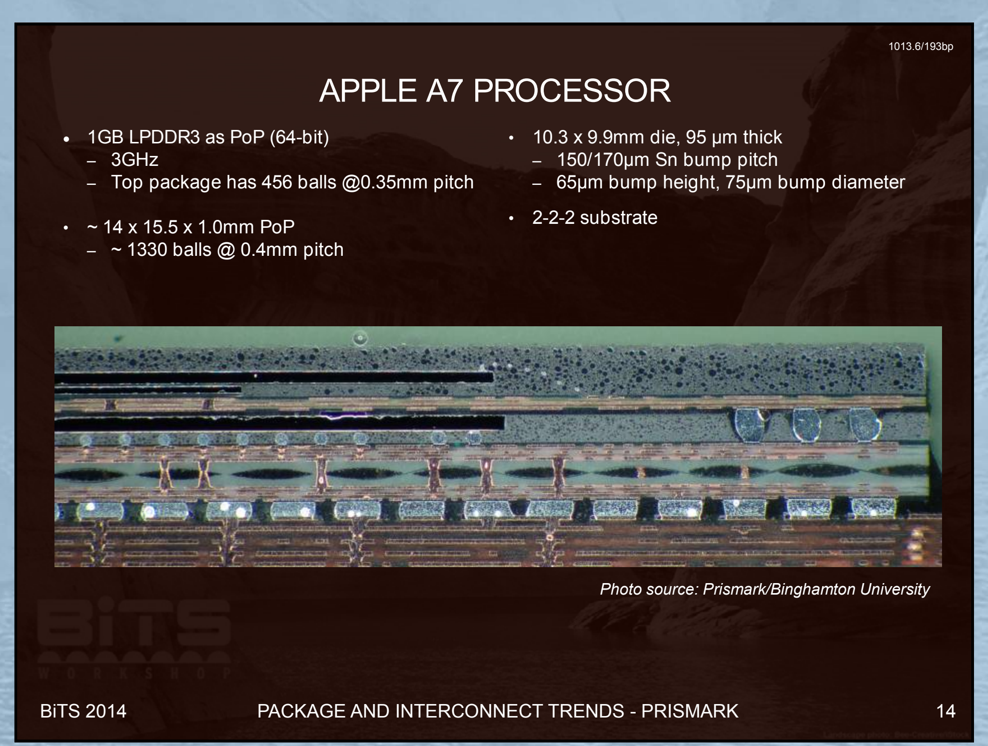
1013.6/193bp
APPLE A7 PROCESSOR
• 1GB LPDDR3 as PoP (64-bit)
– 3GHz
– Top package has 456 balls @0.35mm pitch
• ~ 14 x 15.5 x 1.0mm PoP
– ~ 1330 balls @ 0.4mm pitch
• 10.3 x 9.9mm die, 95 µm thick
– 150/170µm Sn bump pitch
– 65µm bump height, 75µm bump diameter
• 2-2-2 substrate
Photo source: Prismark/Binghamton University
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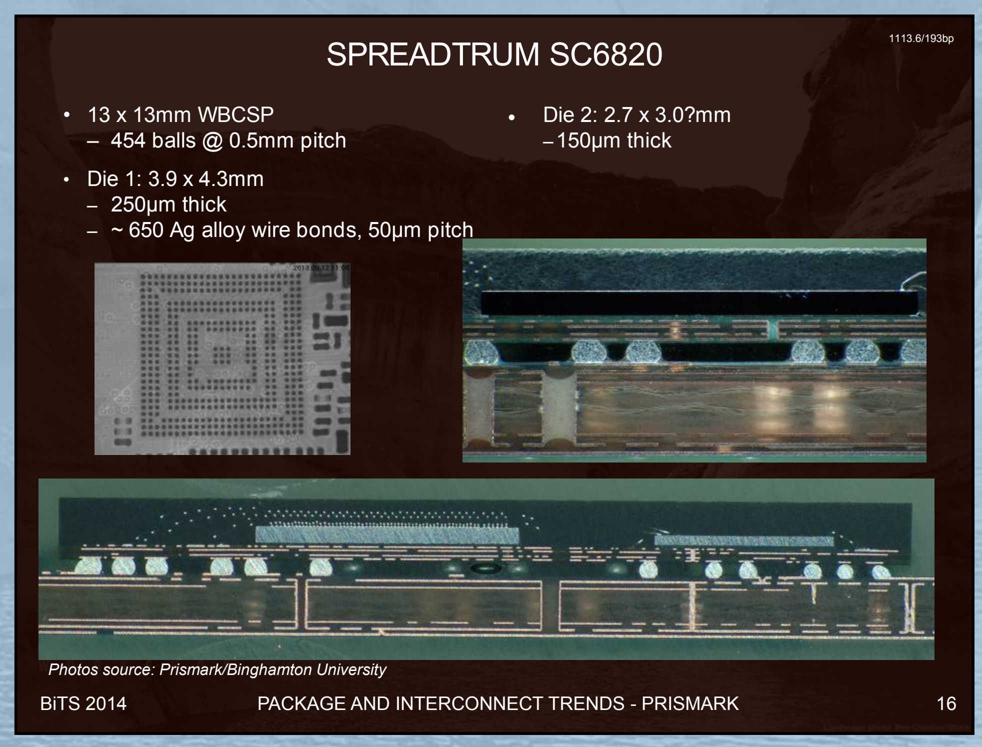

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1213.6/193bp

PHONE AND TABLET APPLICATION PROCESSOR ROADMAP

	2014	2014	2016	2016
Product name	High End	Low cost	High End	Low Cost
Process node	20/22	28/32	14/16	20/22 (some 14/16)
Die Size (mm)	8-11	7-9	8-12 (< 10 target)	7-10
Die thickness (µm)	75-100	100-150	65-80	75-200
Total Bumps (Est.)	3500	700-1500 (some wire bond)	4000	1000-2000
Bump Pitch (µm)	130-150	180	110-130	150/180
Package Size	11-17	10-18	12-16	12-14
Package I/O	950-1400	700	1100-1500	700-900
Package Pitch (mm)	0.4	0.5-0.65	0.35	0.4-0.65
Top PoP I/O	~ 300 (456 A7)	216	300-500	250+
Top PoP Pitch (mm)	0.4 / 0.35	0.5	0.3/0.35	0.4

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0214.1/105bp

SiP/MCP FORECAST

Product/Package Type Volume (Bn Units)	2013	2018 Forecast	Leading Suppliers/Players
Stacked Die In Package and Memory Card	8	11	ASE, SPIL, Amkor, STATS ChipPAC, Samsung, Micron, SKHynix, Toshiba, SanDisk
Stacked Package on Package – Bottom Package Only	0.8	1.3	Amkor, STATS ChipPAC, ASE, SPIL, Samsung, Apple, Qualcomm, Sony, Panasonic
PA Centric RF Module	4.3	6.3	RFMD, Skyworks, Anadigics, Renesas, TriQuint, Avago
Connectivity Module (Bluetooth/WLAN)	0.4	0.5	Murata, Taiyo Yuden, ACSIP, ALPS
Graphics/CPU or ASIC MCP	0.2	0.2	Intel, IBM, Fujitsu, Xlinx, Altera
Leadframe Module (Power/Other)	3	5	NXP, STMicro, TI, Freescale, Toshiba, Infineon, Renesas, IR, ON Semi
MEMS and Controller	5	8	ST, Analog, Bosch, Freescale, Knowles, SKHynix, InvenSense Denso
TOTAL	21.7	32.3	

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CONCLUSIONS

- Package size reduction is ongoing, but pitch limitations draw a logical path towards modular and 3D approaches
- A few clear trends are enabling miniaturization:
  - Fine Pitch Array Packages (0.5 → 0.4 → 0.35 → 0.3/0.25mm)
  - Stacked Die (Memory) and Package Stacks (Logic/Memory)
  - Wafer Level CSP
  - Reduced Z- height packages (0.3 to 0.6mm)
- 3D TSV and Silicon Interposer approaches are still in development, with high volumes products expected in next 3-5 years
  - Challenges emerge for die level test at pitches <50μm
  - Test before die to die or die to wafer assembly often required

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