AND, AT THE WAFER LEVEL

For many in the industry, performing final test at the wafer level is still a novel idea. While providing some much needed solutions, it also comes with its own set of challenges. The four papers in this session look at wafer-level test from a number of different perspectives. The first one discusses the mechanical and electrical differences between wafer-level probe and wafer-level test using spring pins, focusing on requirements for performing final test at the wafer-level. The second presentation provides a comparison between traditional probe test for an RF wafer level chip scale package (WLCSP) and a final test socket solution. TSV issues lead our third author to share technologies that can bridge between 3D stacking and the 3D IC without TSVs. Finally, we'll gain insight into what some consider the holy grail of burn-in and test – wafer-level burn-in (WLBI). Now that WLBI is possible, it's important to understand when it's appropriate to consider WLBI versus other burn-in alternatives.

Spring Probes and Probe Cards for Wafer-Level Test
Jim Brandes—Multitest

A Comparison of Probe Solutions for an RF WLCSP Product
James Migliaccio—RF Micro Devices

Bridging Between 3D and 3D TSV Stacking Technologies
Belgacem Haba, Ph.D.—Invensas

Wafer-Level Burn-in Decision Factors
Steve Steps—Aehr Test Systems

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Wafer-Level Burn-in Decision Factors

Steve Steps
Aehr Test Systems

2013 BiTS Workshop
March 3 - 6, 2013

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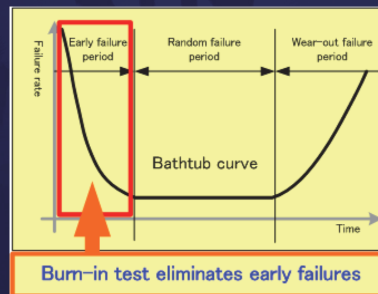
- Options for Burn-in
- Objective of analysis
- Scenario 1: Simple DRAM
- Scenario 2: Memory module
- Scenario 3: 3D stacked package
- Conclusions

Options for Burn-In

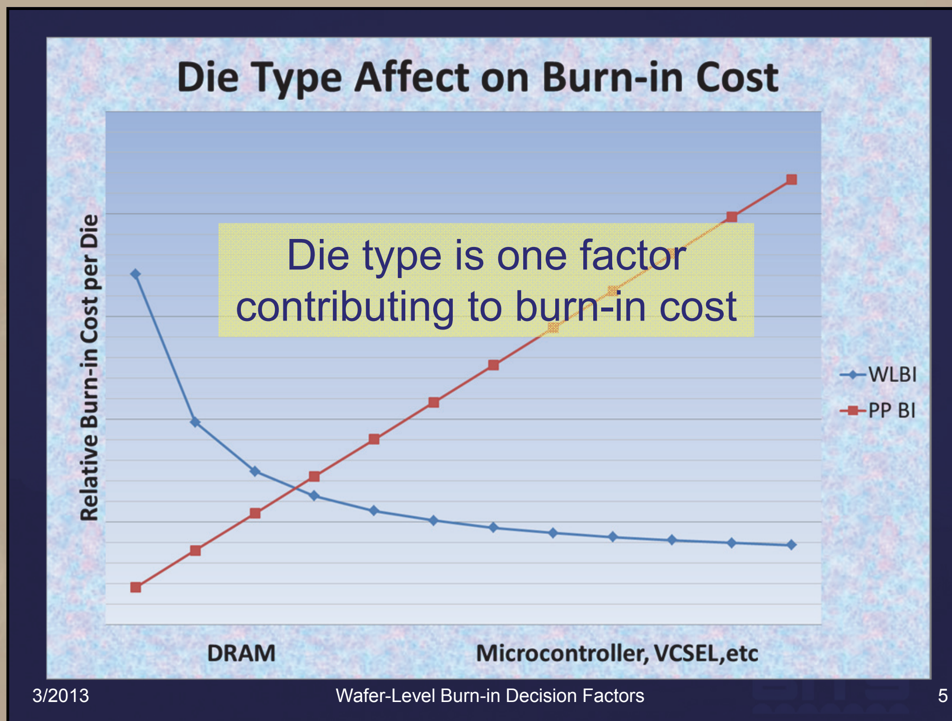
- No burn-in
- Wafer-Level burn-in (WLBI)
- Packaged part burn-in
- Module burn-in



Source: jec.co.jp

Burn-in Tradeoff Summary

- No burn-in
  - If die is more reliable than needed
- WLBI
  - High die count per wafer
  - Expensive packaging (burn-in before packaging)
  - Non-repairable module
- Packaged part burn-in
  - Large die with cheap, small package
- Module burn-in
  - High die count in repairable module
  - Relatively high module-level failures



Objective of Analysis

What factors determine which method of burn-in (if any) is most cost effective?

<u>Note:</u>

- Analysis only focuses on simple economic cost trade-offs and ignores the secondary effects of failures – which are typically significant
- All values (such as cost per die) should be used as relative measures, not absolute values
- "Your mileage may vary"

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Scenario 1: Simple DRAM

- Single, leading edge DRAM die
  - About $2 per die
  - About 750 die per wafer
- Single die per FBGA package
- Model cost versus benefit
  - Burn-in costs
  - Packaging cost savings
- Analysis ignores implications of failure; it only considers cost of replacing the failed die

Source: Digikey

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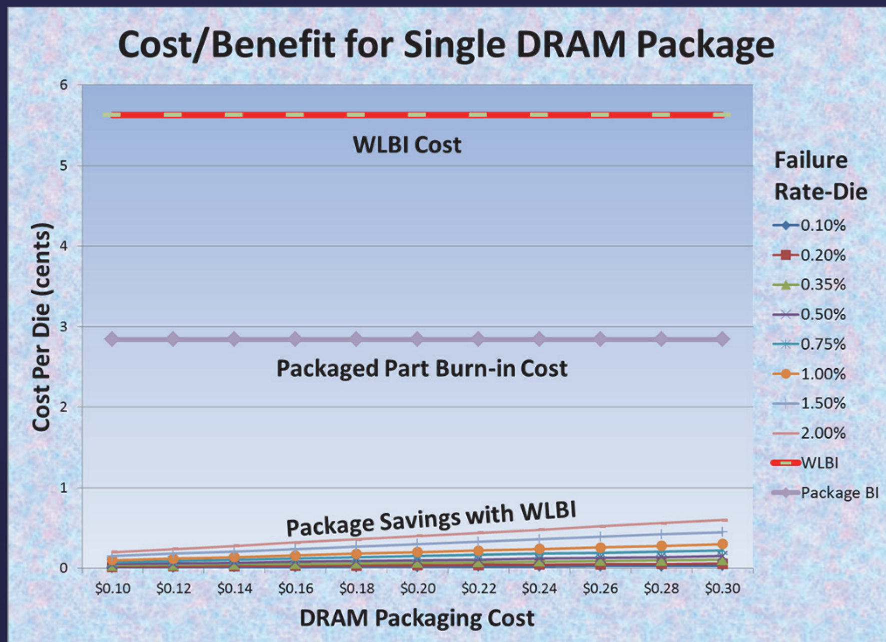

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Simple DRAM Conclusions

- Burn-in savings are quite small
  - Infant mortality die are thrown away anyway
  - Savings is only packaging costs
  - Burn-in costs are much higher than savings
- Burn-in not economically justified
  - but only if the effects of failures are ignored
  - Only considered replacement of device

Source: Digikey

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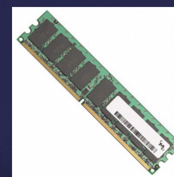
Scenario 2: Memory Module

- Assumptions:
  - $2 per memory die
  - Up to 18 die per package
- Model cost versus benefit of
  - Wafer-Level burn-in
  - Packaged Part burn-in
  - Module burn-in

Note: failure cost limited to replacement of module



Source: Digikey

Source: Amazon

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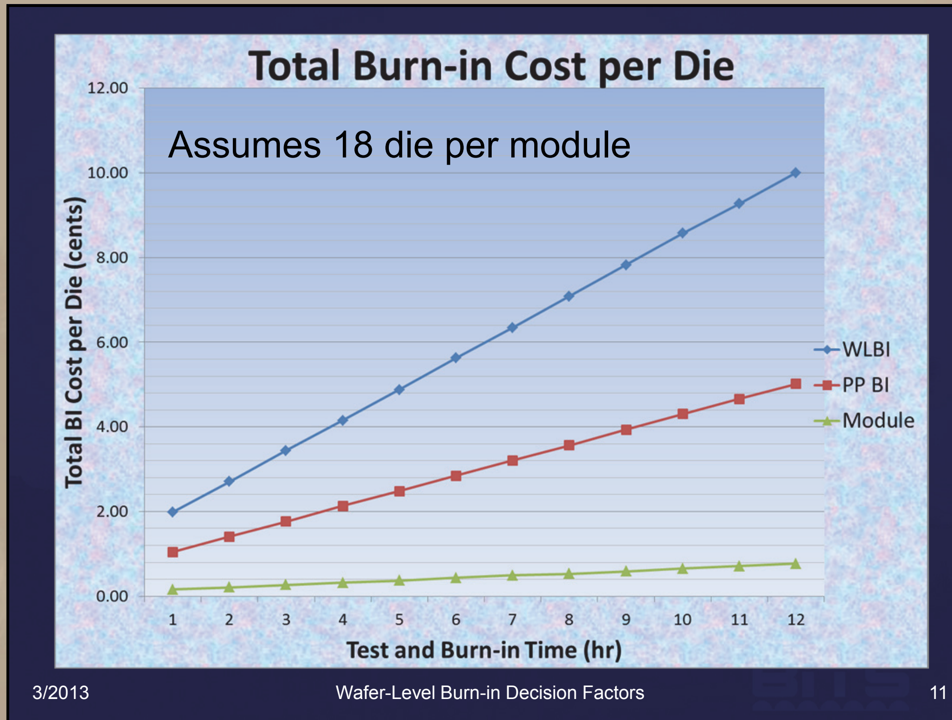
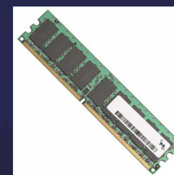


Preliminary Conclusion

- Burn-in costs
  - Highest: Wafer-Level burn-in
  - Mid: Packaged Part burn-in
  - Lowest: Module burn-in
- Is this the whole story?
- No, ignores the effects of failures
- Can module be repaired after burn-in?


Source: Digikey

Source: Amazon

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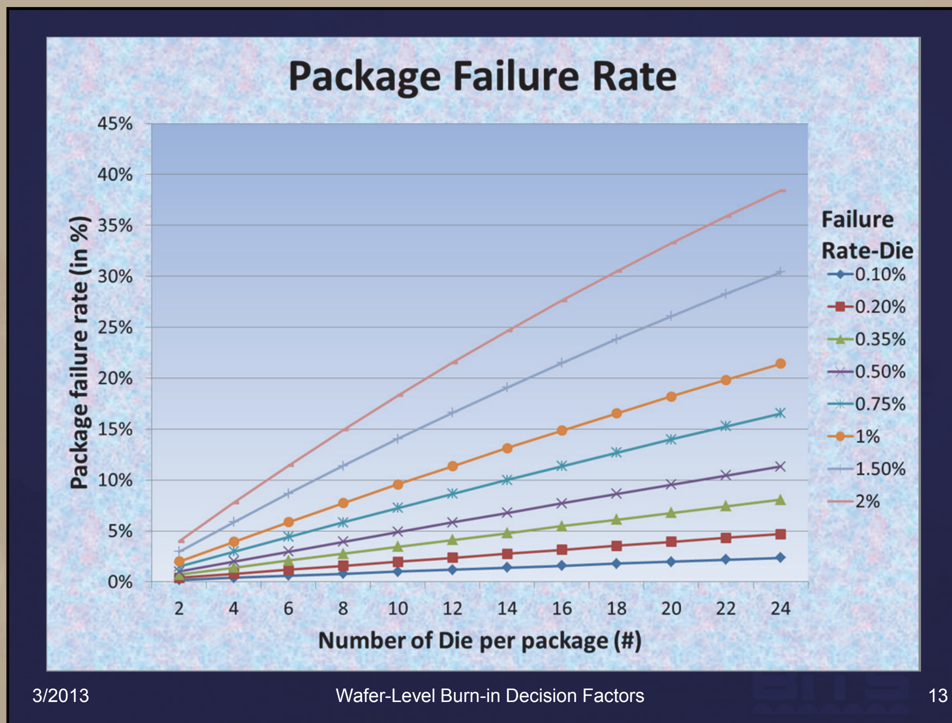
Package Failure Rate
Package failure rate (in %)
45%
40%
35%
30%
25%
20%
15%
10%
5%
0%
2
4
6
8
10
12
14
16
18
20
22
24
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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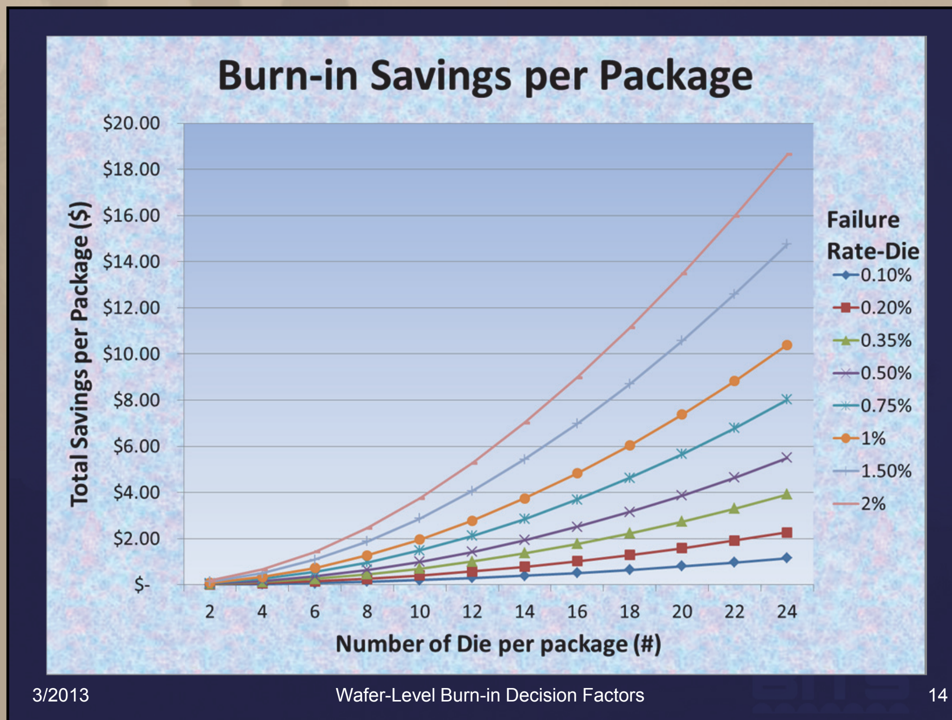
Burn-in Savings per Package
Total Savings per Package ($)
$20.00
$18.00
$16.00
$14.00
$12.00
$10.00
$8.00
$6.00
$4.00
$2.00
$-
2
4
6
8
10
12
14
16
18
20
22
24
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
3/2013
Wafer-Level Burn-in Decision Factors
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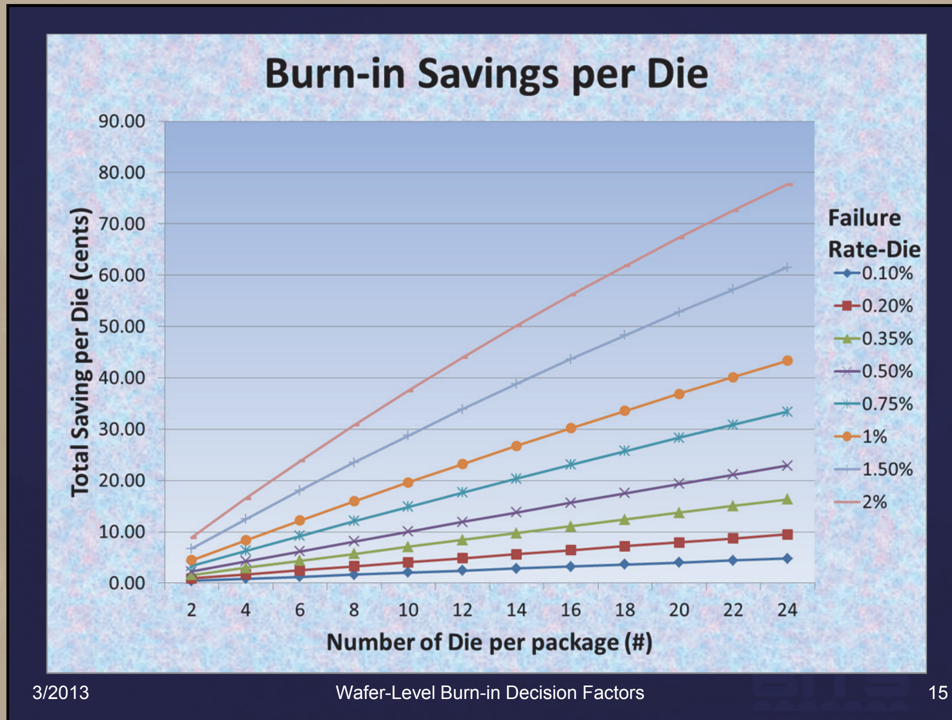
Burn-in Savings per Die
Total Saving per Die (cents)
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
2
4
6
8
10
12
14
16
18
20
22
24
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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Wafer-Level Burn-in Decision Factors
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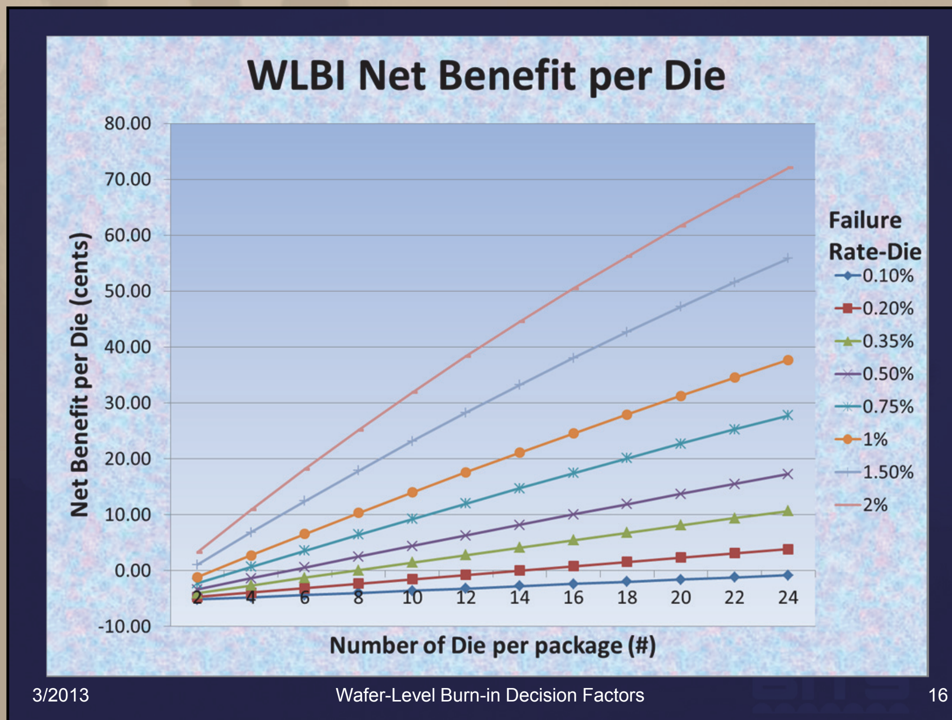
WLBI Net Benefit per Die
Net Benefit per Die (cents)
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
-10.00
2
4
6
8
10
12
14
16
18
20
22
24
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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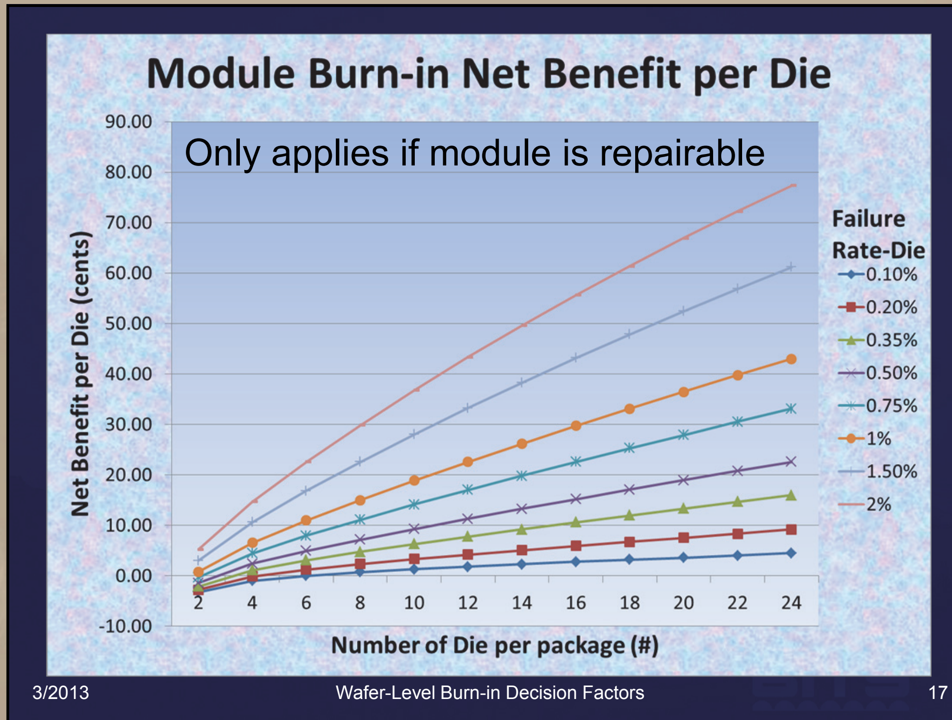

Memory Module Observations

- If failure rate improvement is low enough (<0.1%), then burn-in is not justifiable by module replacement cost savings alone
  - If die count is high and module is repairable, then Module-level burn-in might be cost justified
  - If the combination of number of die per module and failure rate is very low, then burn-in is not justified on module replacement cost savings alone
- If module is not repairable, and both die count and failure rate are not low, then wafer-level burn-in is very cost effective

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Scenario 3: 3D Stacked Package

- Stacked package with:
  - $20 microcontroller chip
  - 1 to 12 memory die @ $2 each
  - $5 packing cost
- Model cost per benefit varying:
  - Memory die count
  - Memory die failure rate

Note: only memory failures considered and cost of failure limited to replacement of package only

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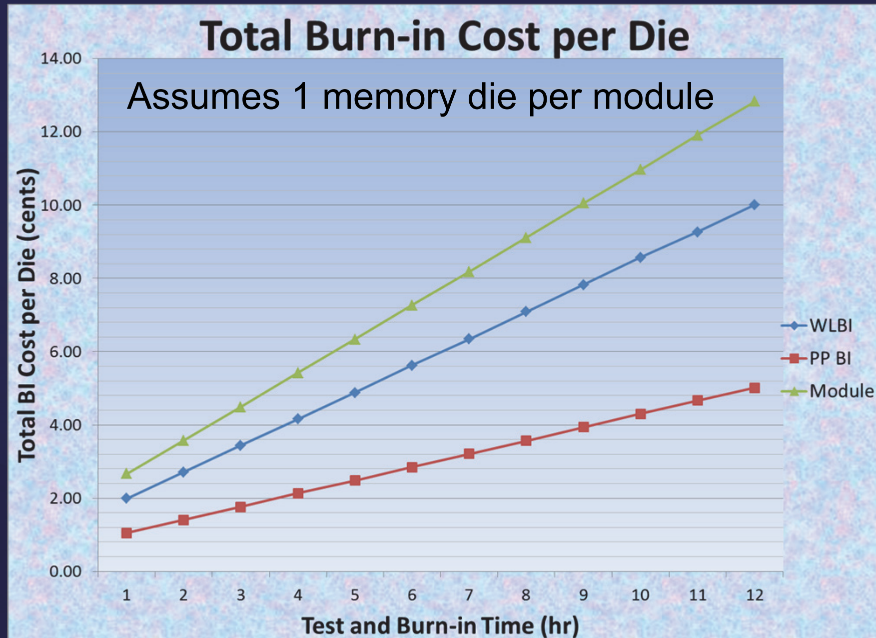

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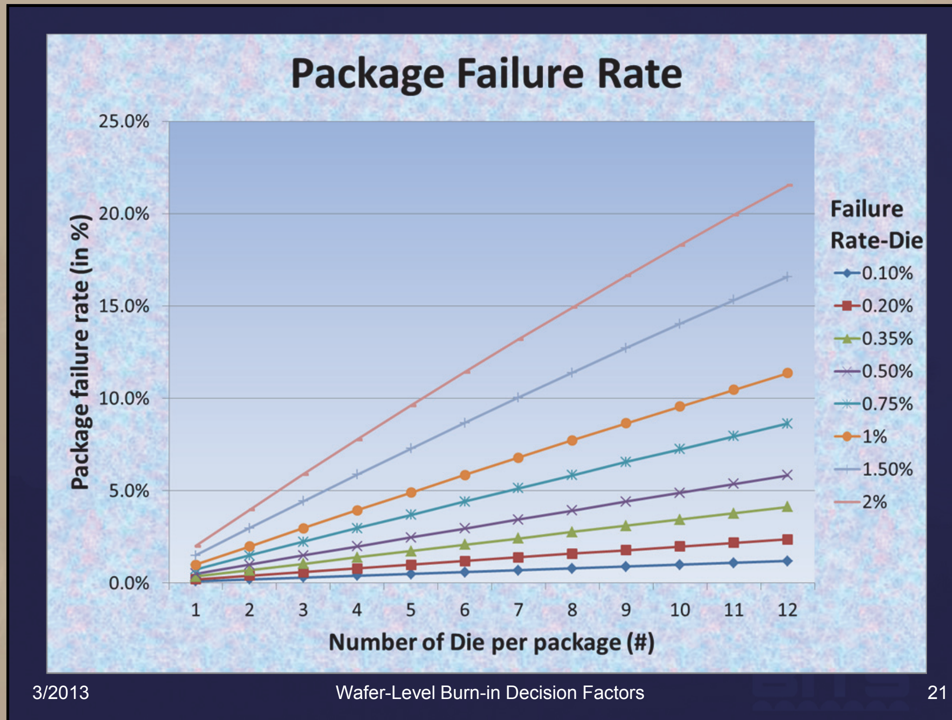
Package Failure Rate
Package failure rate (in %)
25.0%
20.0%
15.0%
10.0%
5.0%
0.0%
1
2
3
4
5
6
7
8
9
10
11
12
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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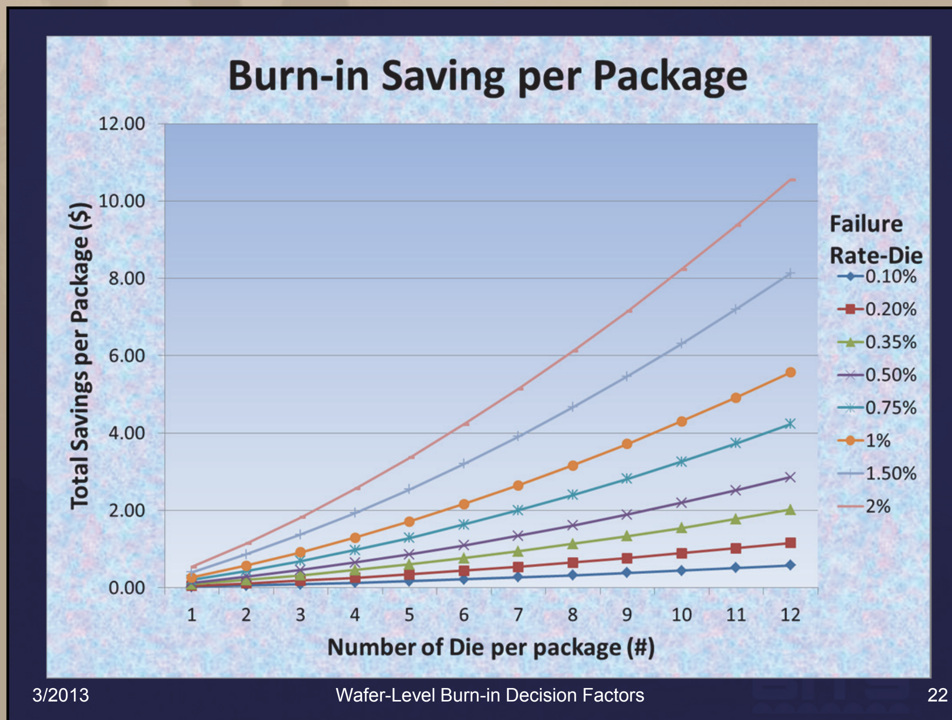
Burn-in Saving per Package
Total Savings per Package ($)
12.00
10.00
8.00
6.00
4.00
2.00
0.00
1
2
3
4
5
6
7
8
9
10
11
12
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
3/2013
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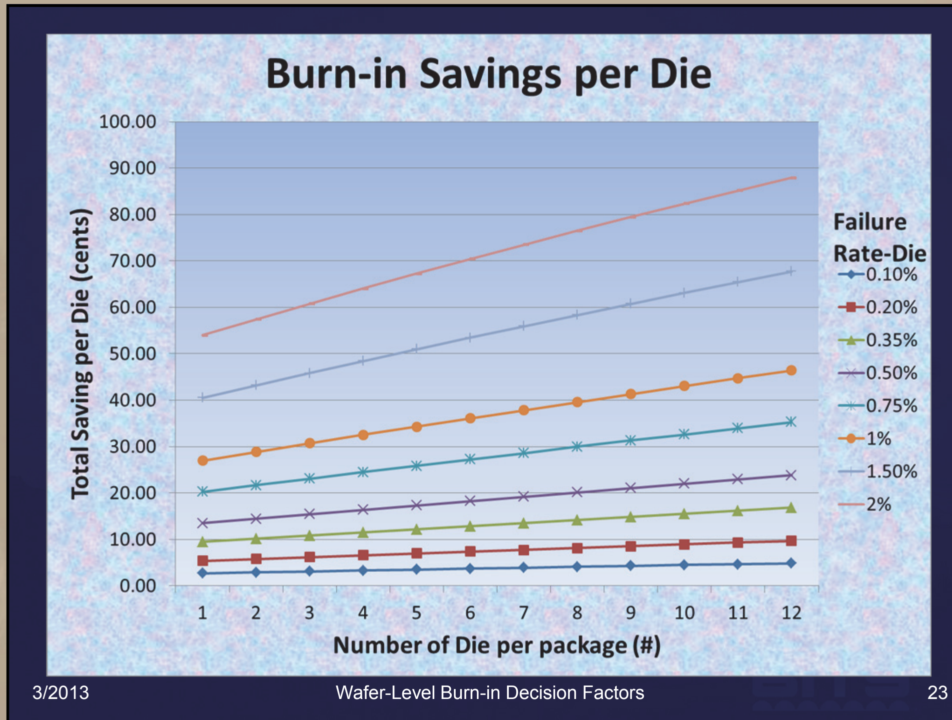
Burn-in Savings per Die
Total Saving per Die (cents)
100.00
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
1
2
3
4
5
6
7
8
9
10
11
12
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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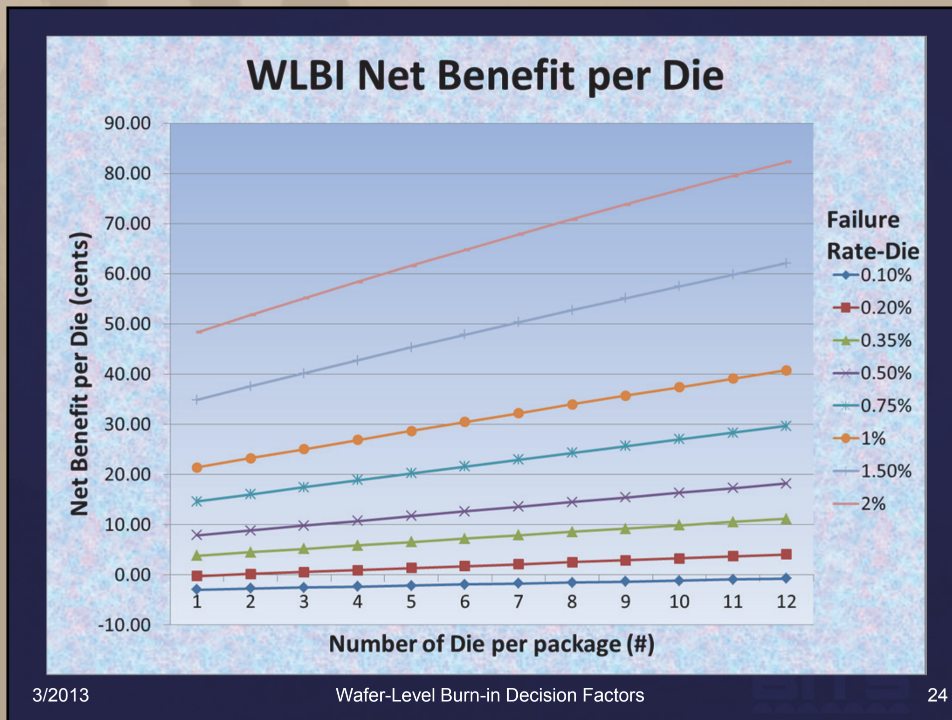
WLBI Net Benefit per Die
Net Benefit per Die (cents)
90.00
80.00
70.00
60.00
50.00
40.00
30.00
20.00
10.00
0.00
-10.00
1
2
3
4
5
6
7
8
9
10
11
12
Number of Die per package (#)
Failure Rate-Die
0.10%
0.20%
0.35%
0.50%
0.75%
1%
1.50%
2%
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24

3D Stack Observations

- If failure rate improvement is low enough (<0.1%) then burn-in is not justified by package replacement cost
- Burn-in decision is relatively independent of the number of memory die in the stack
  - Note this is very different from the memory module case
- Since the 3D stack is probably not repairable, wafer-level burn-in may be the only choice and is very cost effective

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Overall Conclusions (1)

- No burn-in might be appropriate choice if:
  - Die more reliable than needed
  - Limited implications of failure
- Package part burn-in might be cost effective if:
  - Large die (limited number of die per wafer)
  - Cheap, small package (high count per burn-in board)
- Module burn-in might be most cost effective if:
  - High die count in a repairable module
  - Relatively high module-level failures

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Overall Conclusions (2)

- Wafer-Level burn-in is likely the best choice if:
  - Die failure rate is not very low
  - High die count per wafer
  - Expensive packaging (burn-in before packaging)
  - Multiple die in a non-repairable end device
- All forms of burn-in are more justified if:
  - end application is sensitive to failures (such as automotive, medical, military, aerospace)
- WLBI can also be justified by:
  - Wafer information valuable (failure location on wafer, fab process monitoring, etc.)

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